

US00D768585S

(12) **United States Design Patent** (10) **Patent No.:** **US D768,585 S**  
**Moore et al.** (45) **Date of Patent:** **\*\* Oct. 11, 2016**

(54) **ELECTRONICS ENCLOSURE**  
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(\*\*) Term: **14 Years**

\* cited by examiner

(21) Appl. No.: **29/511,819**

*Primary Examiner* — Ian Simmons

(22) Filed: **Dec. 15, 2014**

*Assistant Examiner* — Harold Blackwell, II

(51) **LOC (10) Cl.** ..... **13-99**

(74) *Attorney, Agent, or Firm* — GE Global Patent  
Operation

(52) **U.S. Cl.**  
USPC ..... **D13/184**

(57) **CLAIM**

(58) **Field of Classification Search**  
USPC ..... 200/51.05; D13/101, 110, 118, 122,  
D13/123, 162, 197, 184, 199; 307/150–152,  
307/9.1; 361/600, 601, 622, 702, 703, 730,  
361/796, 809; 363/141, 142; 385/135;  
D14/188  
CPC ..... H05K 7/20854; Y10T 24/44983  
See application file for complete search history.

The ornamental design for an electronics enclosure, as  
shown and described.

**DESCRIPTION**

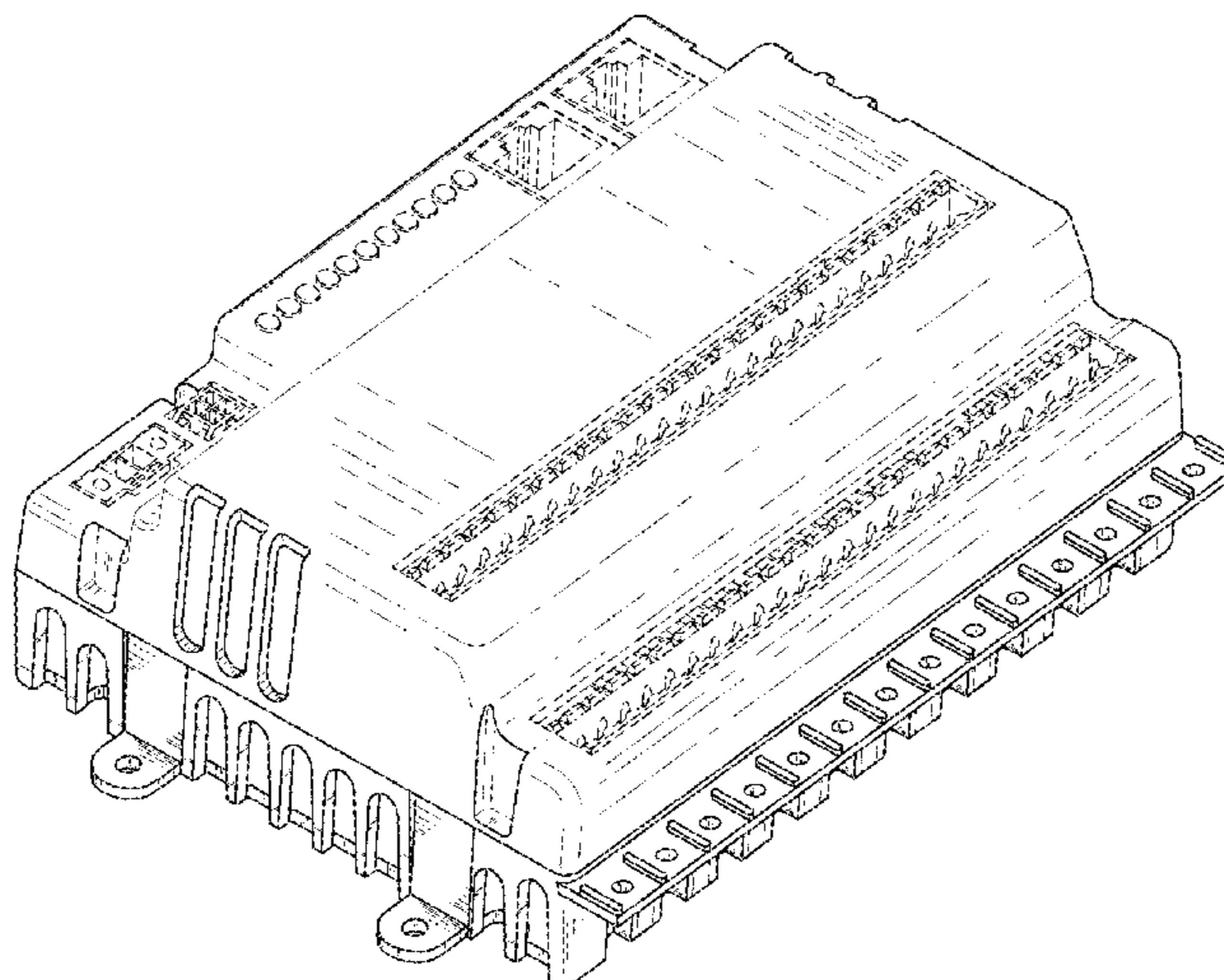
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FIG. 1 is a top, front, left perspective view of our design for  
an electronics enclosure;  
FIG. 2 is a top plan view of our design in FIG. 1;  
FIG. 3 is a bottom plan view of our design in FIG. 1;  
FIG. 4 is a front elevation view of our design in FIG. 1;  
FIG. 5 is a rear elevation view of our design in FIG. 1;  
FIG. 6 is a left side elevation view of our design in FIG. 1;  
and,  
FIG. 7 is a right side elevation view of our design in FIG. 1.  
In Figures 1-7, the broken lines are directed to environment,  
and are for illustrative purposes.  
The broken lines in the drawings illustrate portions of an  
electronics enclosure which form no part of the claimed  
design.

**1 Claim, 7 Drawing Sheets**



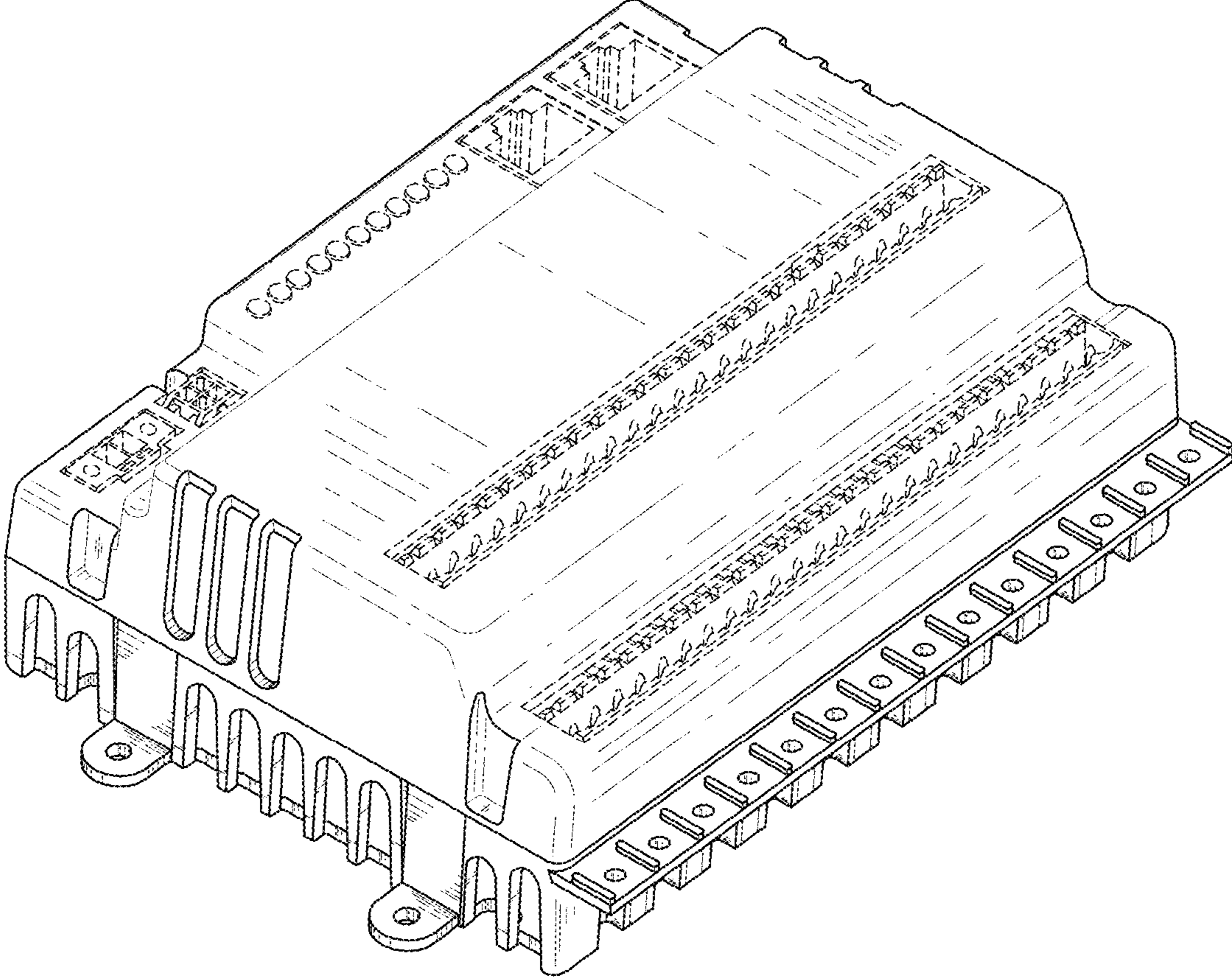


FIG. 1

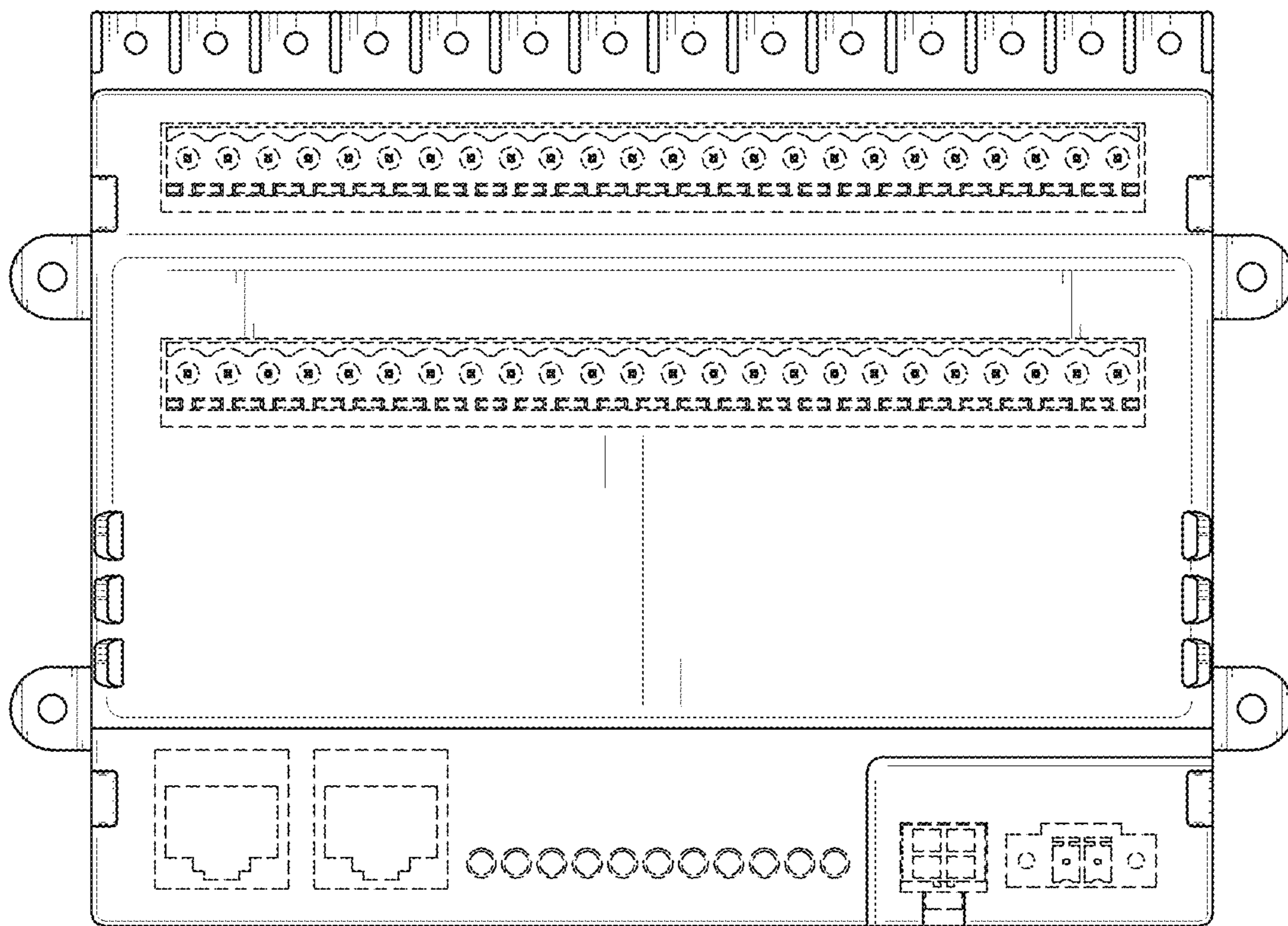


FIG. 2

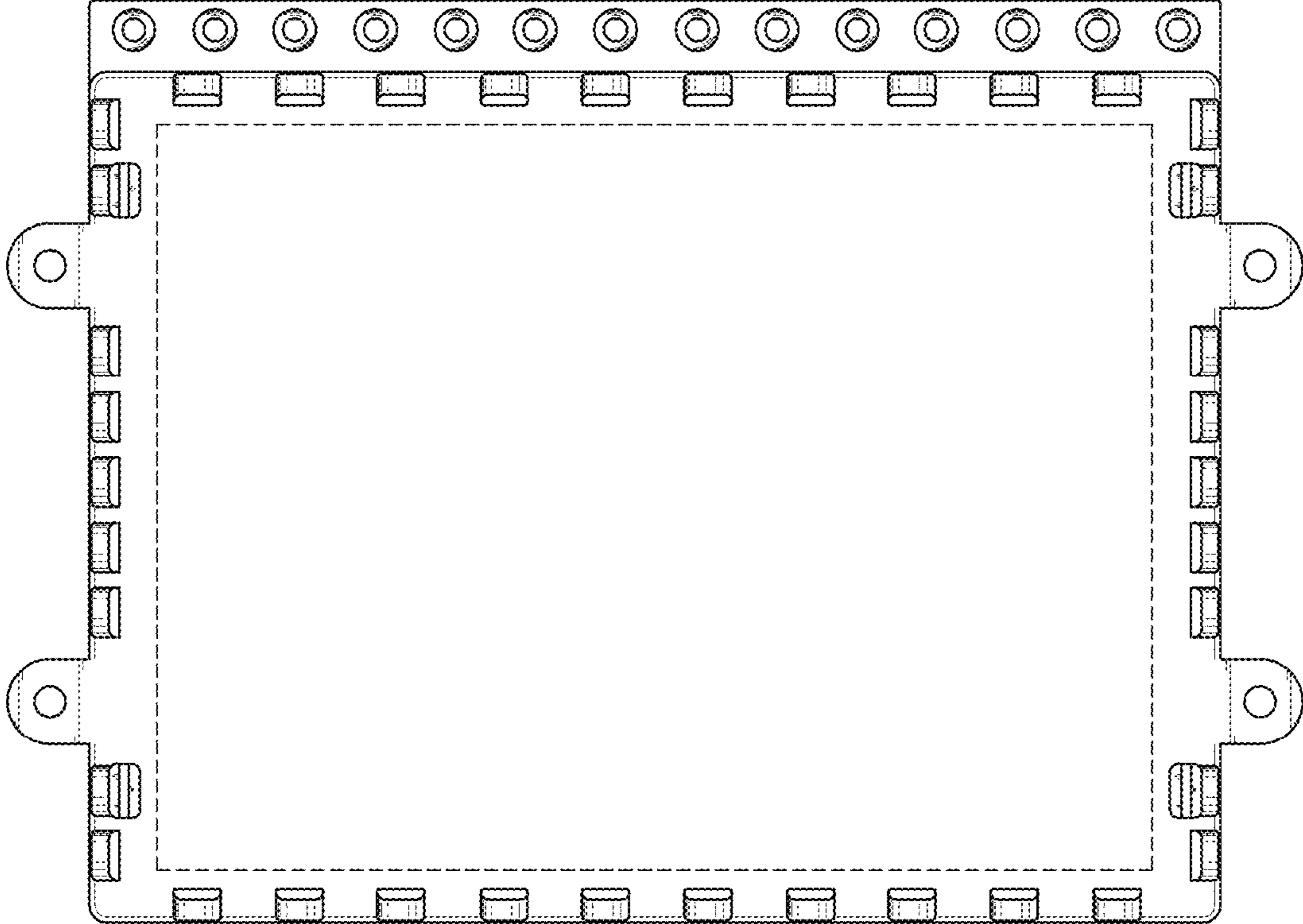


FIG. 3

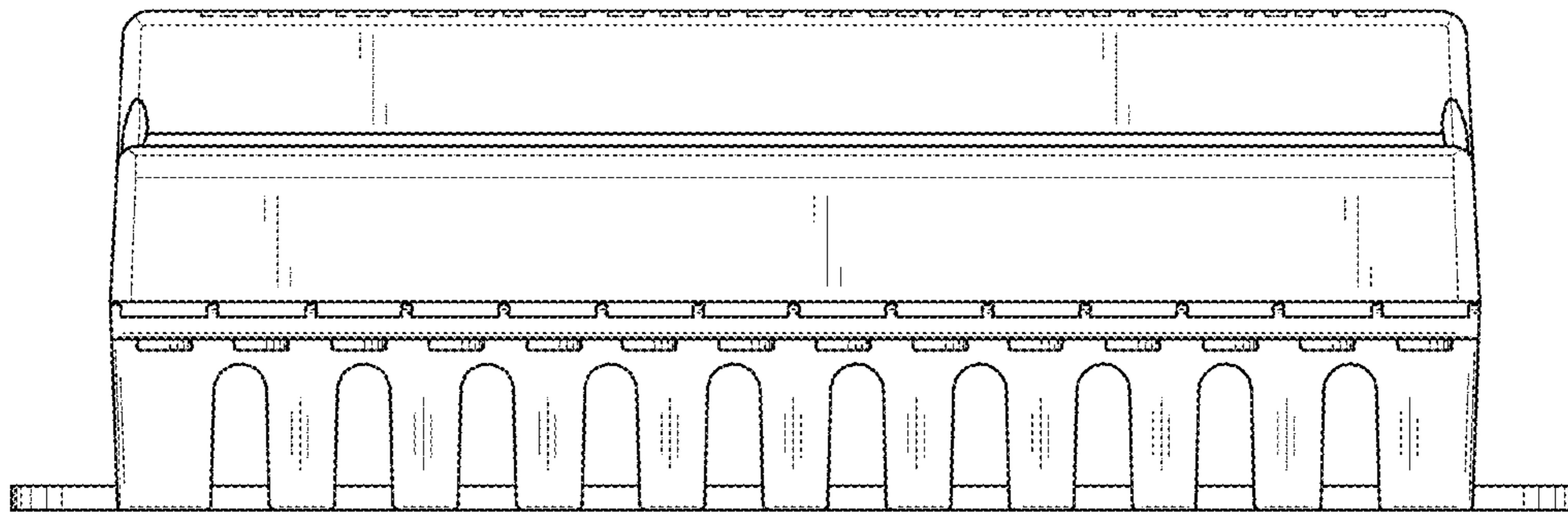


FIG. 4

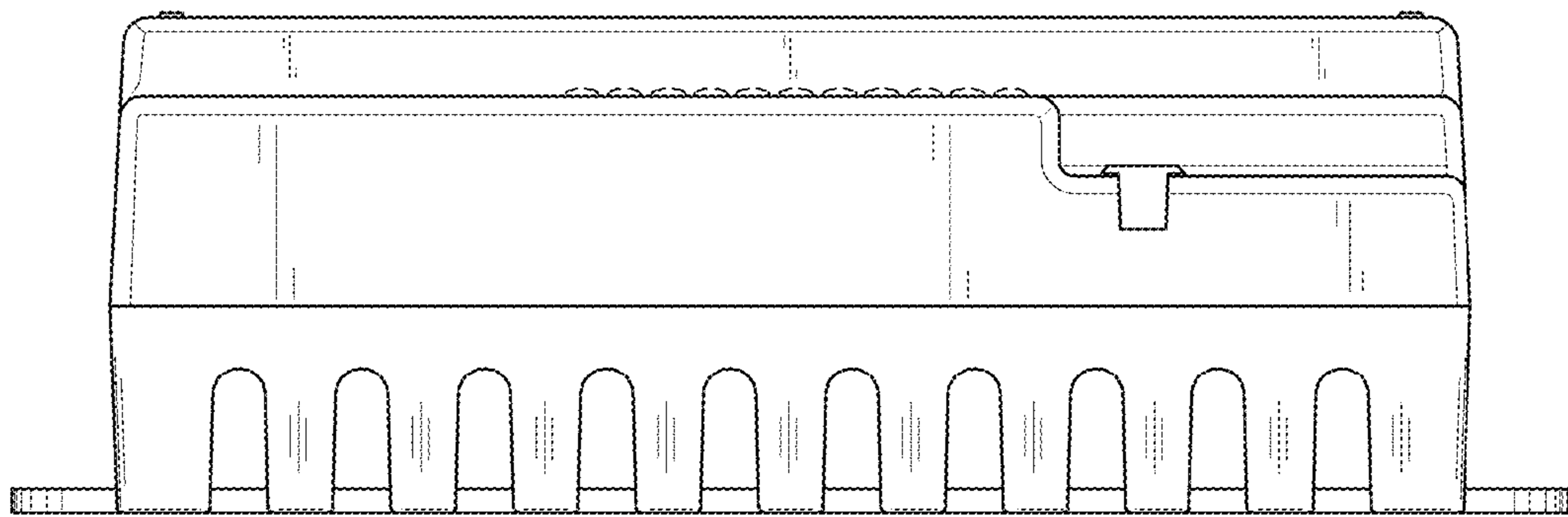


FIG. 5

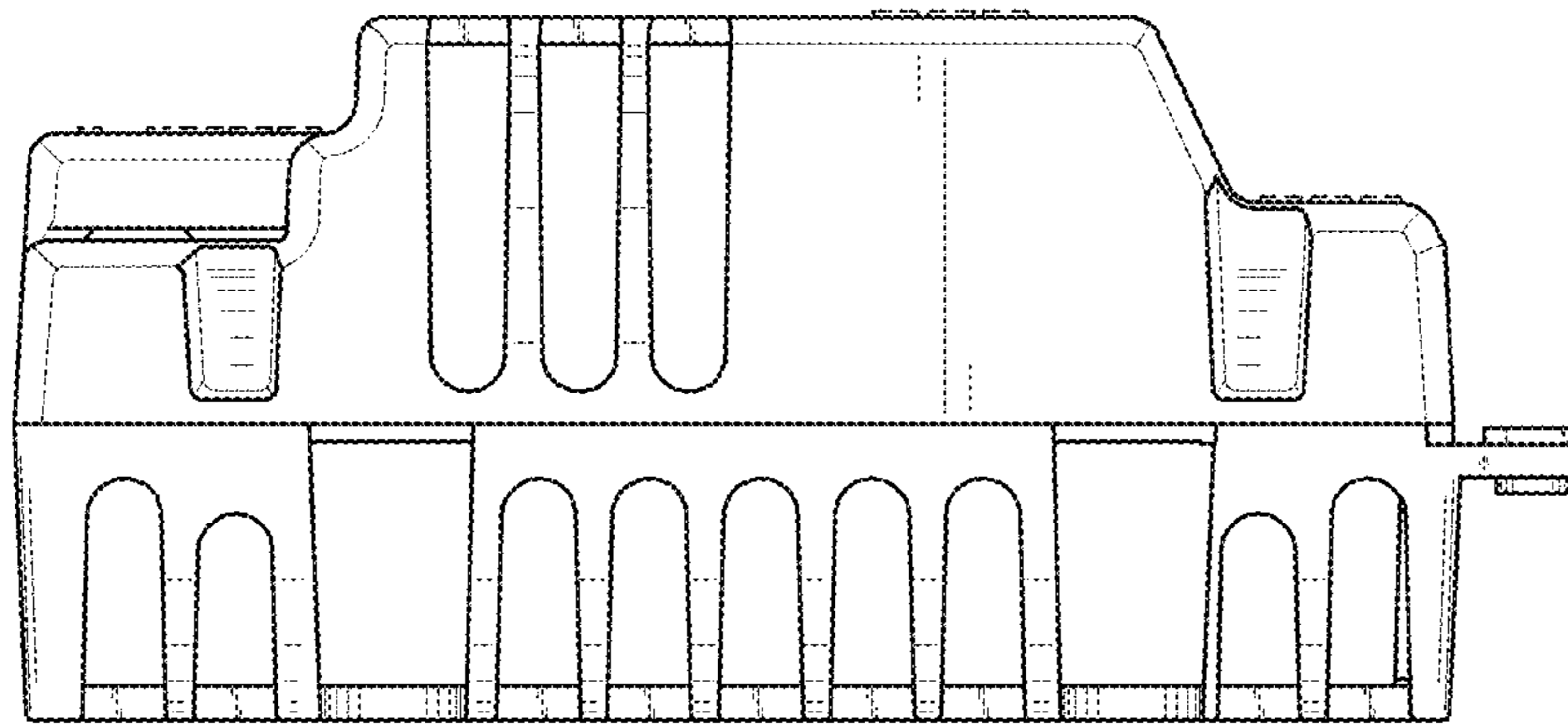


FIG. 6

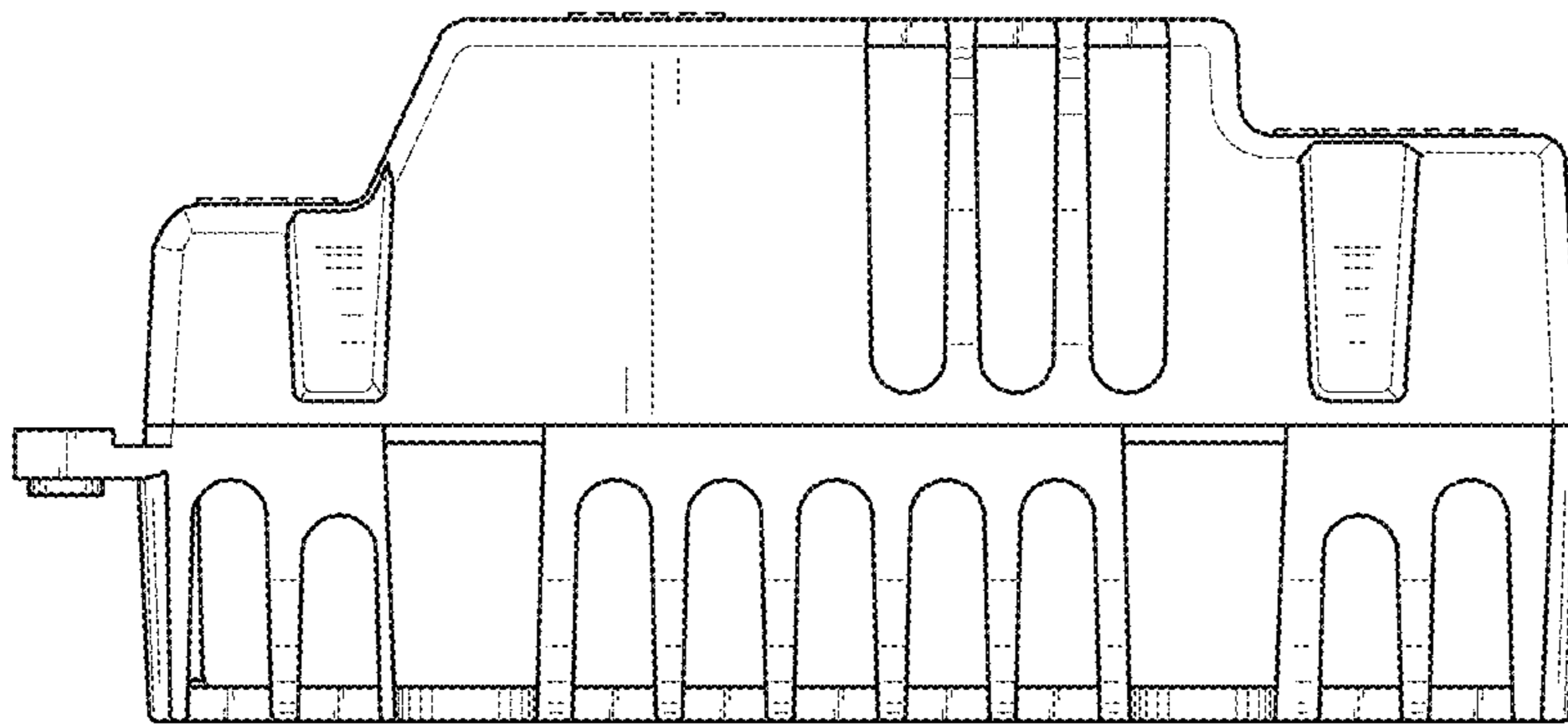


FIG. 7