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(12) **United States Design Patent**
Sharma et al.

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(54) **TRIANGULAR SEMICONDUCTOR DIE**

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(*) Notice: This patent is subject to a terminal disclaimer.

(**) Term: **14 Years**

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Related U.S. Application Data

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/110, 182; 257/668, 678, 690;
361/679.01, 713, 728, 736, 760, 761,
361/775, 820; 324/71.5, 252; 174/250, 253;
438/64, 65, 66

CPC H01L 2924/14; H01L 21/00; H01L 21/02;
H01L 21/324; H01L 23/488; H01L 23/495;
H01L 23/49503; H01L 23/49506; H01L
23/50; H01L 23/48; H01L 23/52; H01L
23/522; H01L 23/532; H01L 23/53204;
H01L 29/02; H01L 29/06; H01L 29/0657;
H01L 29/66; H01L 25/00; H01L 25/072
See application file for complete search history.

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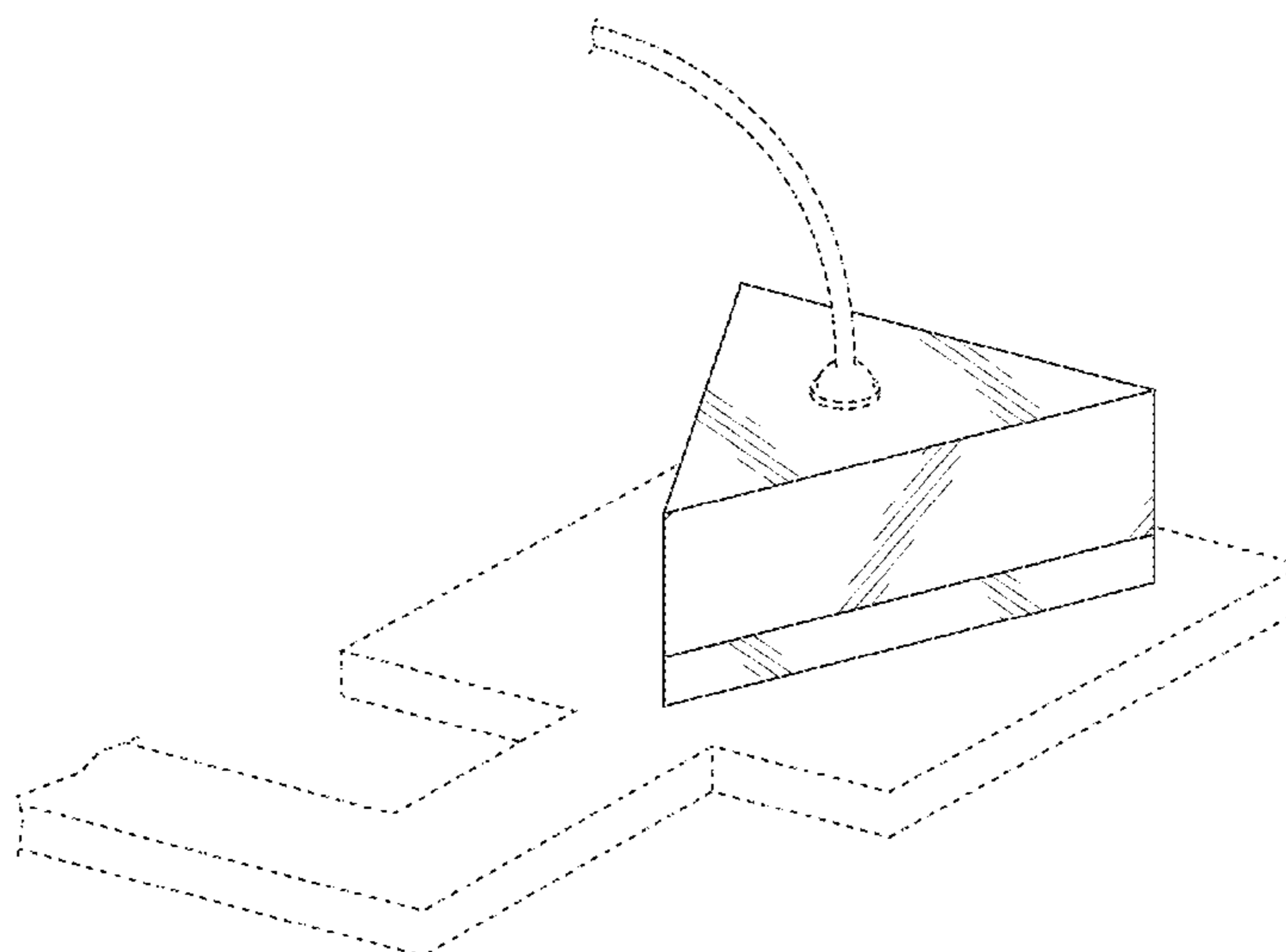
(57) **CLAIM**

The ornamental design for triangular semiconductor die, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of a triangular semiconductor die showing our new design;
FIG. 2 is another perspective view thereof;
FIG. 3 is a top plan view thereof;
FIG. 4 is a bottom plan view thereof;
FIG. 5 is a side elevation view thereof;
FIG. 6 is another side elevation view thereof;
FIG. 7 is another side elevation view thereof; and,
FIG. 8 is another side elevation view thereof.
The broken lines in the figures represent unclaimed subject matter and form no part of the claimed design.

1 Claim, 4 Drawing Sheets



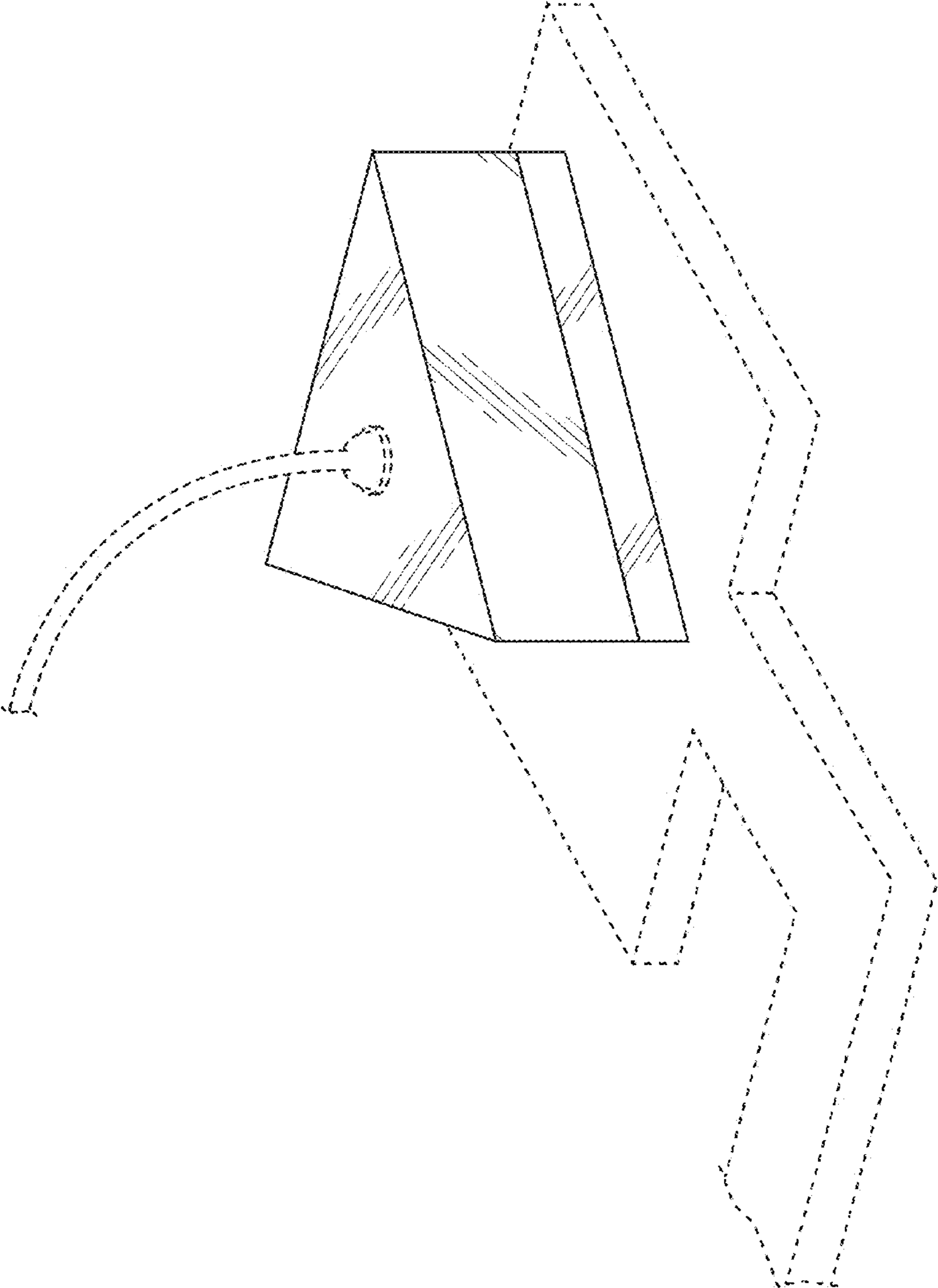


FIG. 1

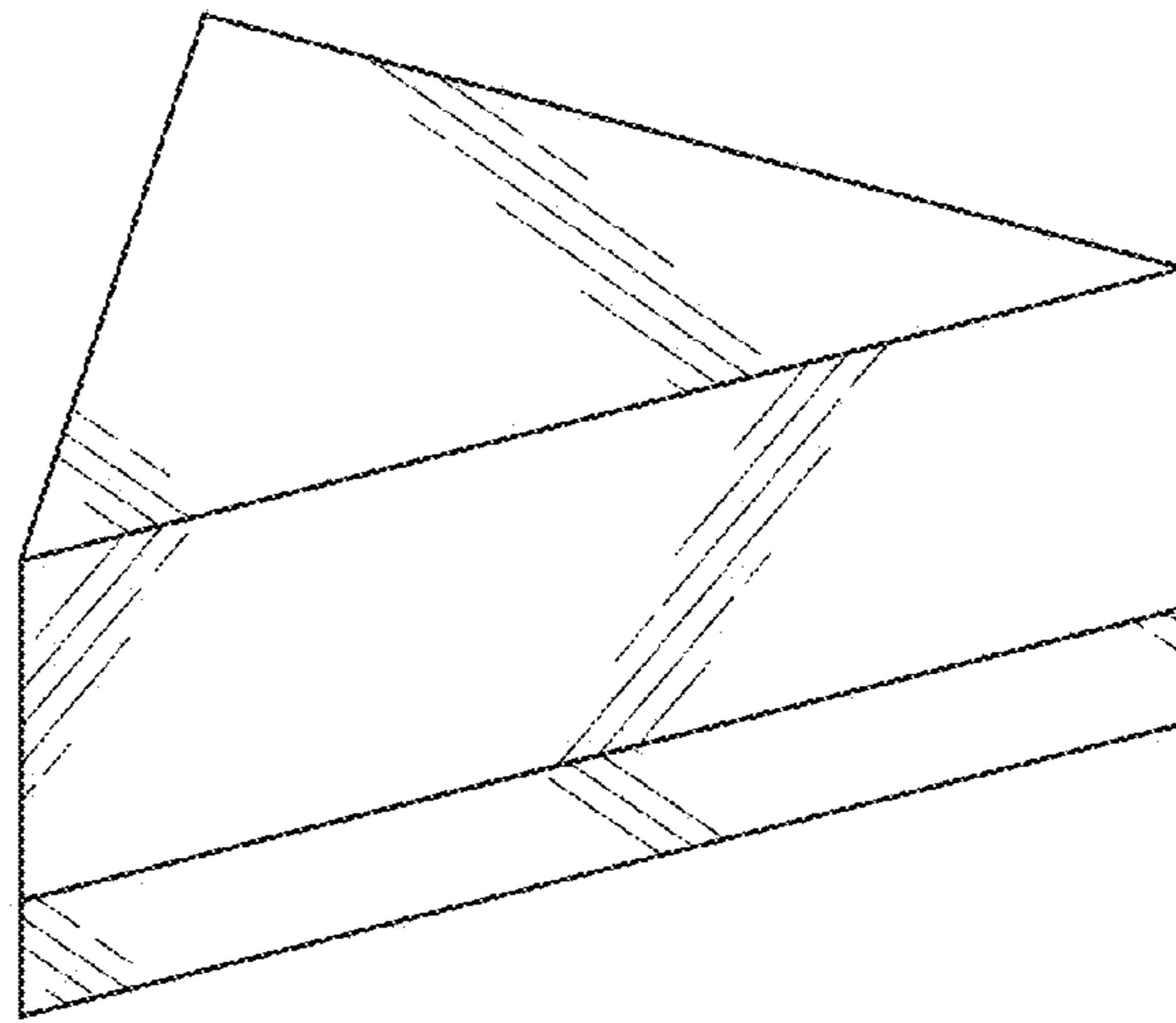


FIG. 2

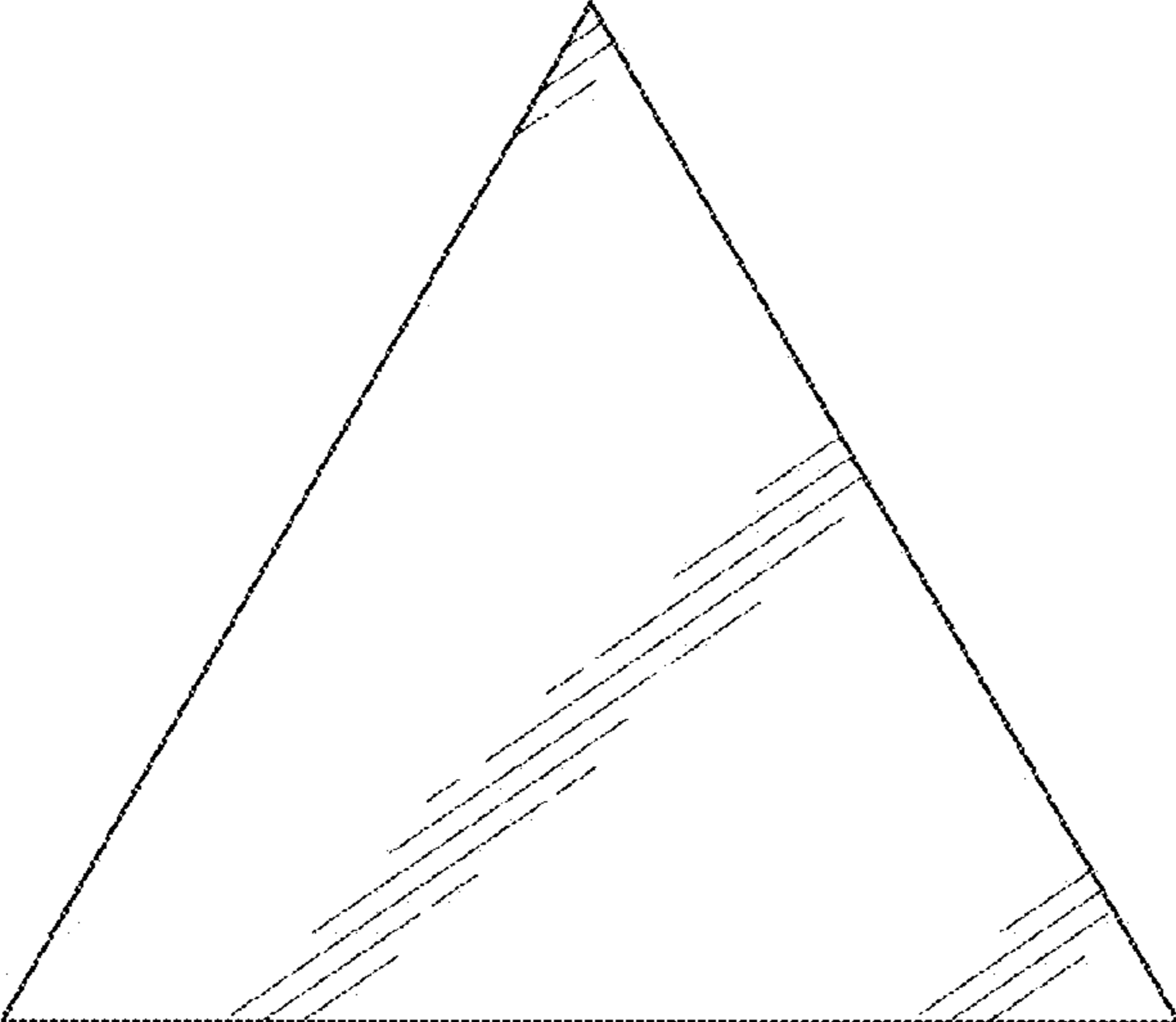


FIG. 3

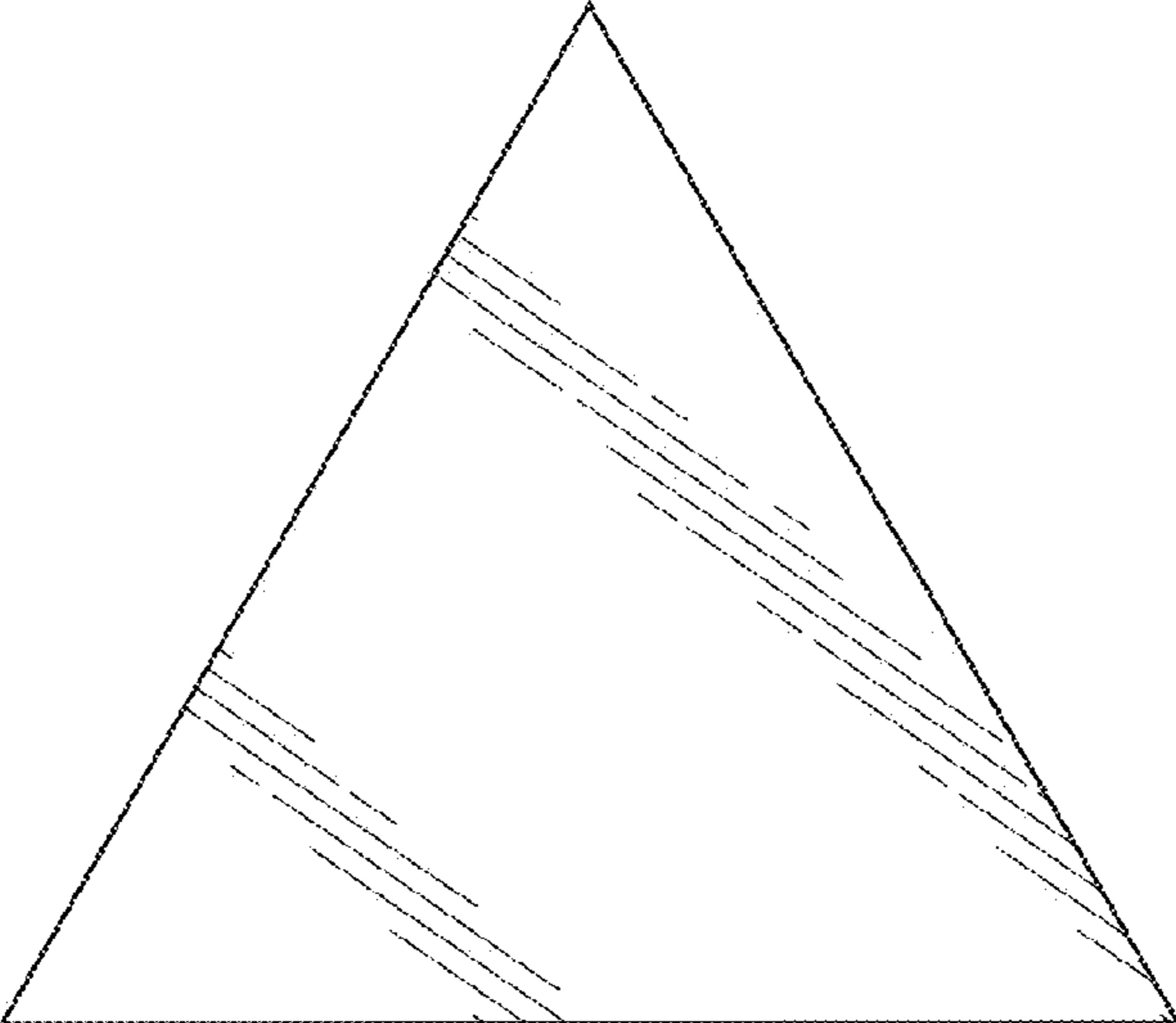


FIG. 4

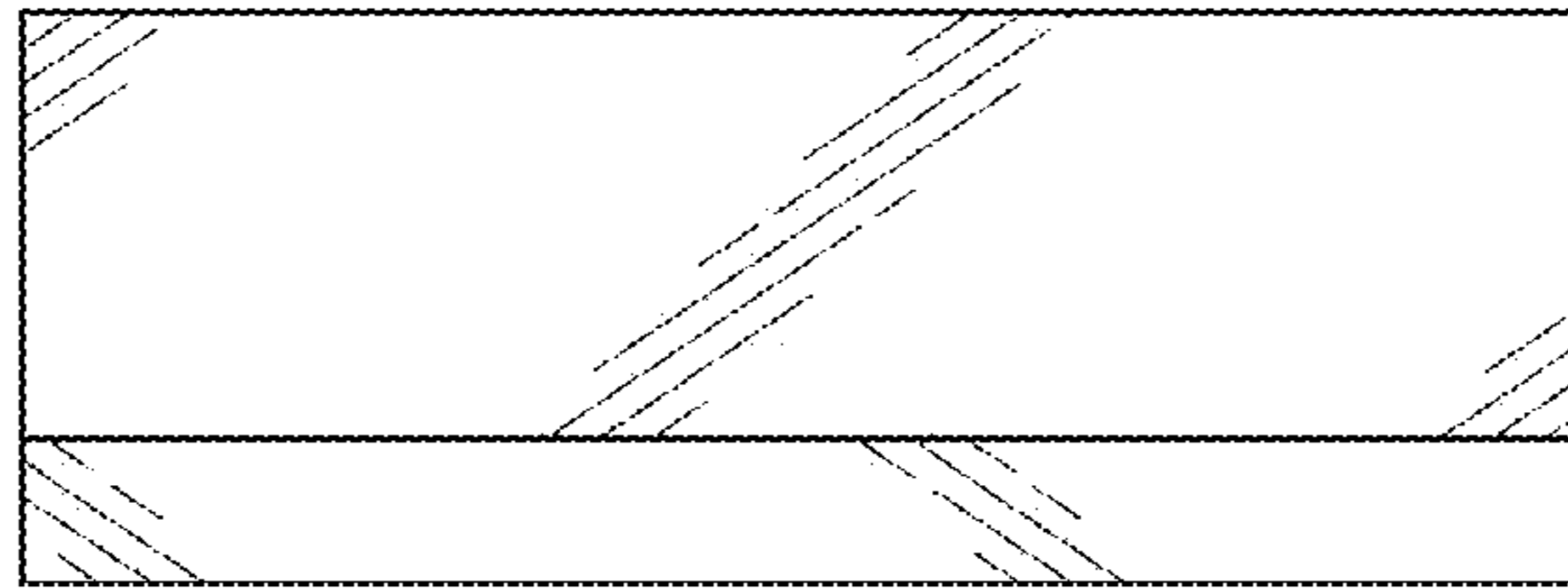


FIG. 5

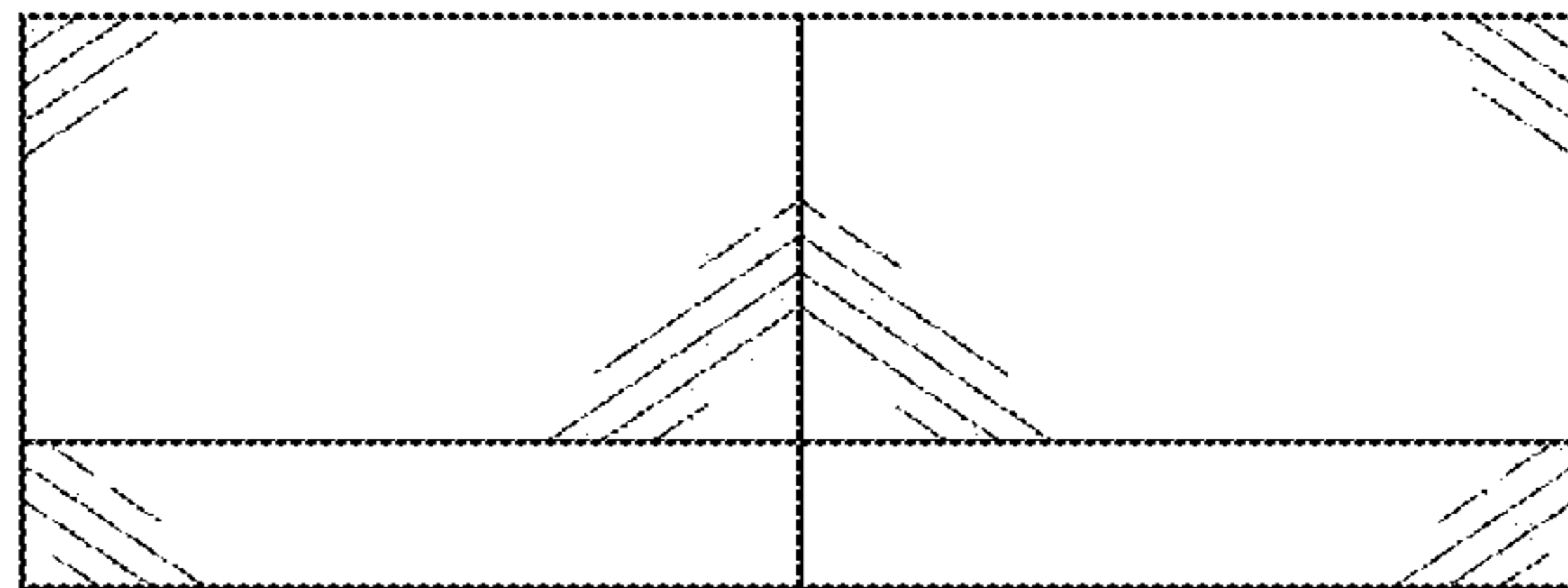


FIG. 6

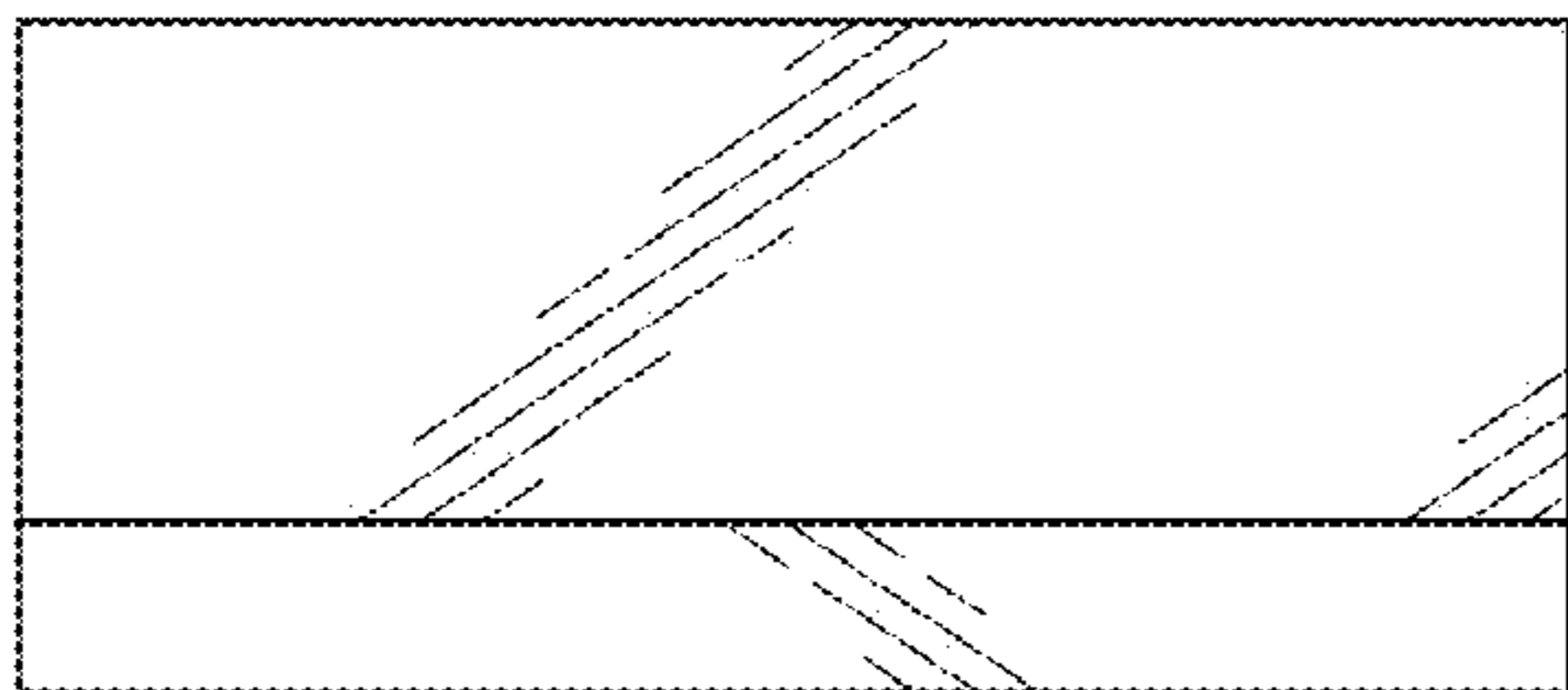


FIG. 7

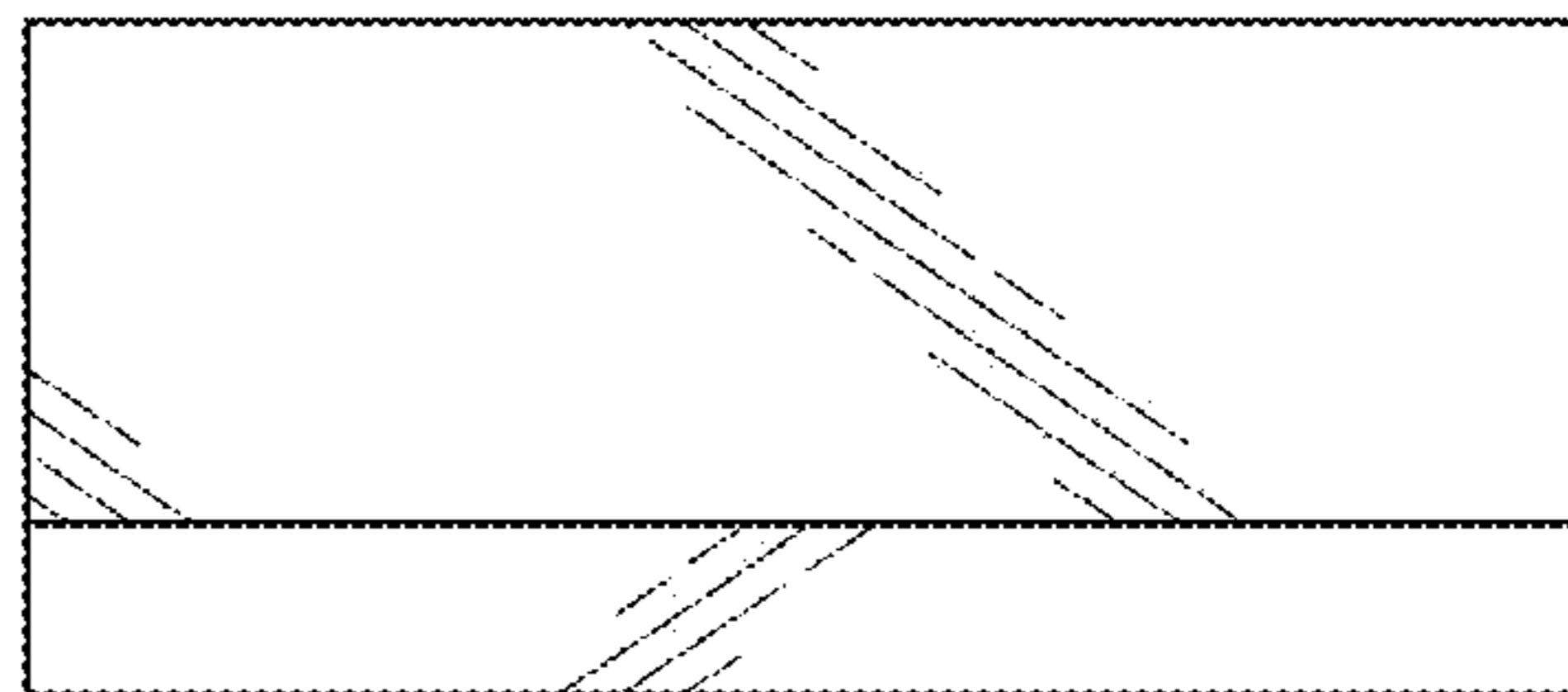


FIG. 8