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(12) **United States Design Patent**  
**Toyoshima**

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(54) **SEMICONDUCTOR MODULE FOR POWER CONVERSION**

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(30) **Foreign Application Priority Data**

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(51) **LOC (10) Cl.** ..... **13-03**

(52) **U.S. Cl.**  
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361/679.01, 713, 728, 736, 760, 761,  
361/772, 775, 783, 820; 174/250, 253;  
438/15, 25, 26, 51, 55, 63, 64, 106  
CPC . H01L 21/00; H01L 2224/42; H01L 2224/43;  
H01L 2021/00; H01L 2021/02; H01L  
2021/04; H01L 21/4814; H01L 21/4846;  
H01L 21/4871; H01L 21/67144; H01L 23/12;  
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H01L 2924/171; H01L 2924/1711; H01L  
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G02B 6/4261; G02B 6/4262; G02B 6/428;  
G02B 6/4281; H05K 1/14; H05K 1/141;  
H05K 1/142; H05K 1/144; H05K 1/18;  
H05K 1/181; H05K 1/182; H05K 1/026

See application file for complete search history.

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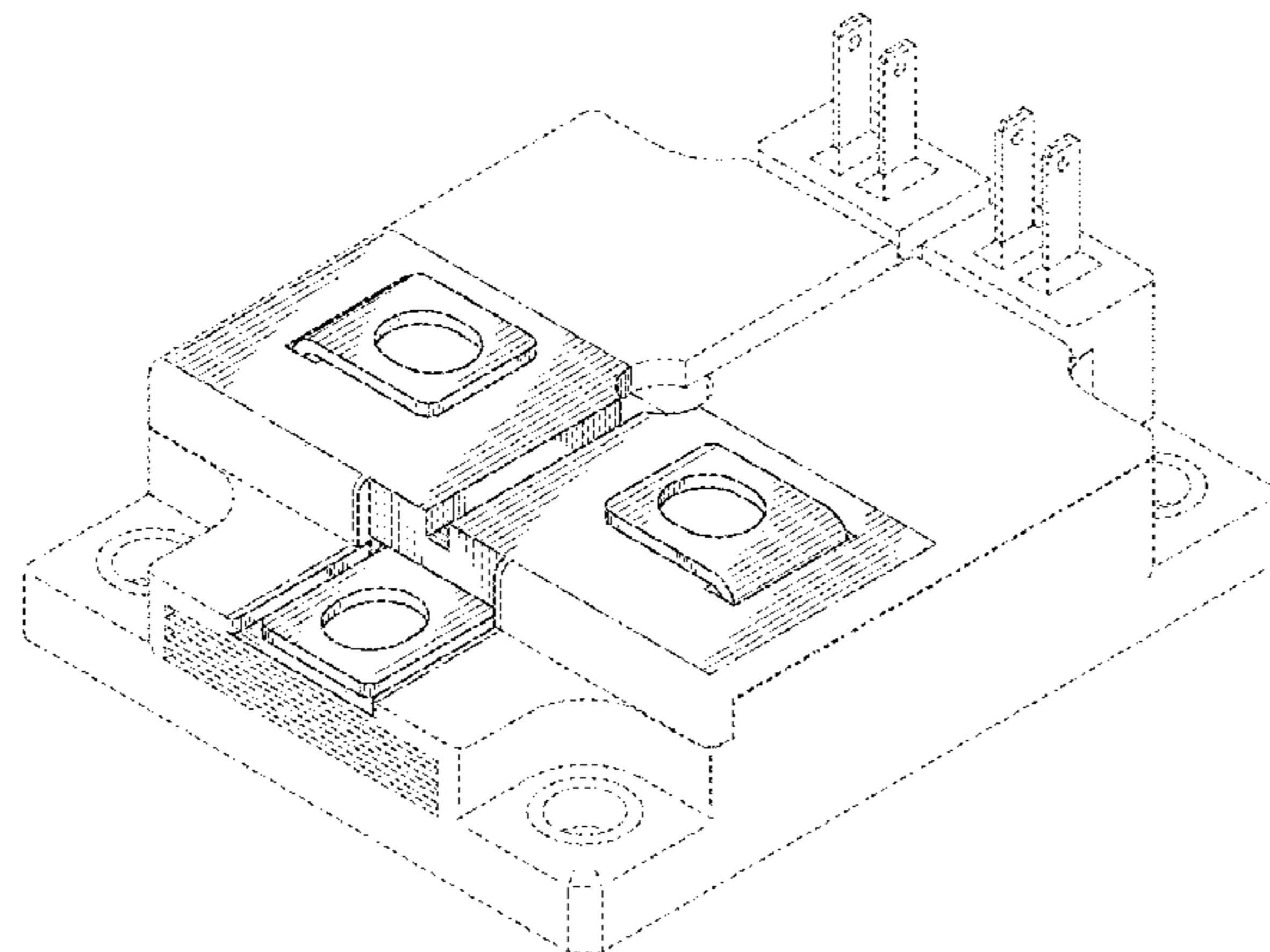
(57) **CLAIM**

The ornamental design for a semiconductor module for power conversion, as shown and described.

**DESCRIPTION**

FIG. 1 is a front view of a semiconductor module for power conversion showing my new design.  
FIG. 2 is a rear view of the semiconductor module for power conversion of FIG. 1.  
FIG. 3 is a top plan view of the semiconductor module for power conversion of FIG. 1.  
FIG. 4 is a bottom plan view of the semiconductor module for power conversion of FIG. 1.  
FIG. 5 is a right side view of the semiconductor module for power conversion of FIG. 1.  
FIG. 6 is a left side view of the semiconductor module for power conversion of FIG. 1; and,  
FIG. 7 is a perspective view of the semiconductor module for power conversion of FIG. 1.  
The dashed-dot-dashed lines represent the boundary lines of the claimed design. The even dashed lines represent unclaimed environment that form no part of the claimed design.

**1 Claim, 7 Drawing Sheets**



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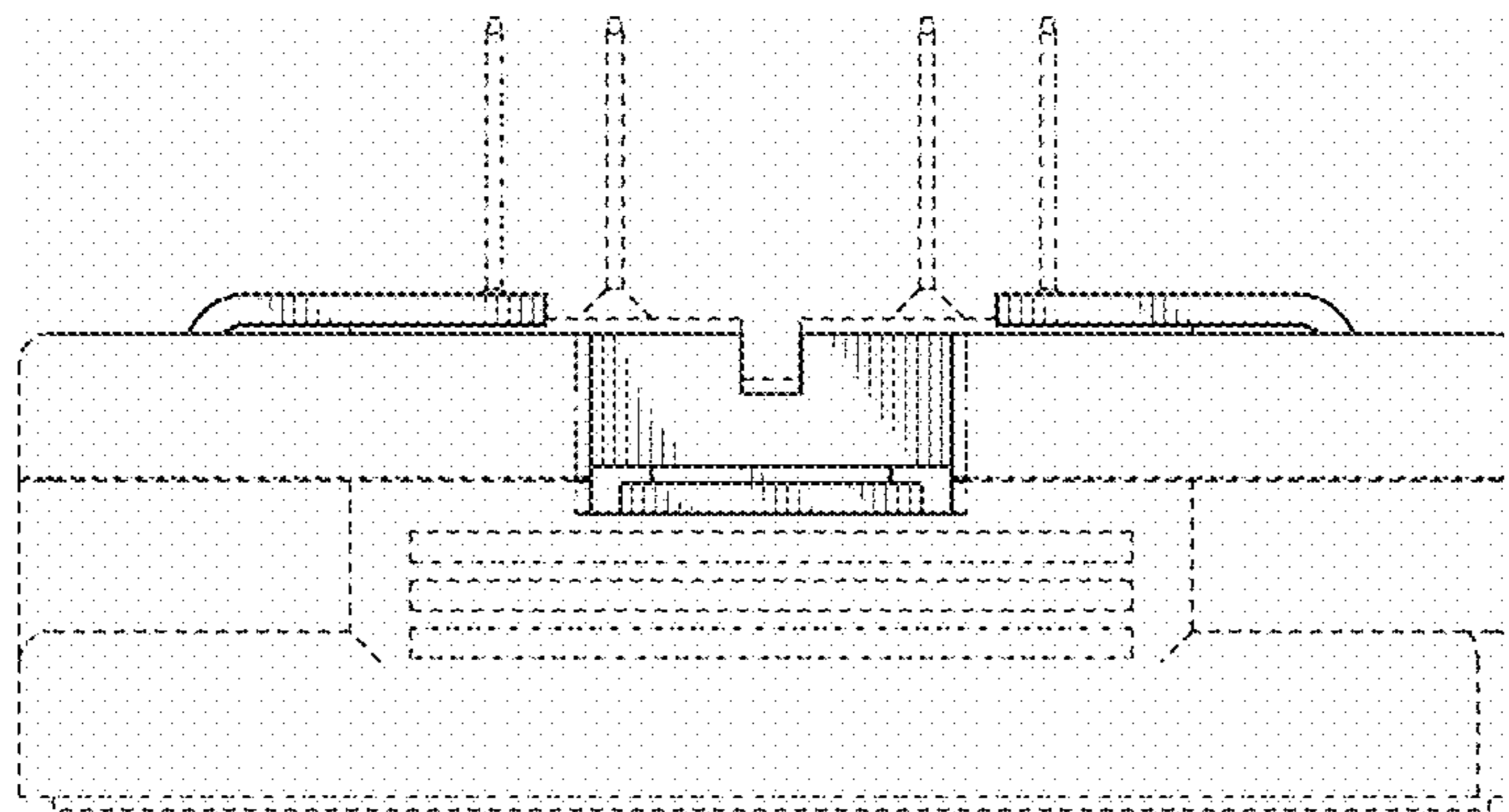


Fig. 1

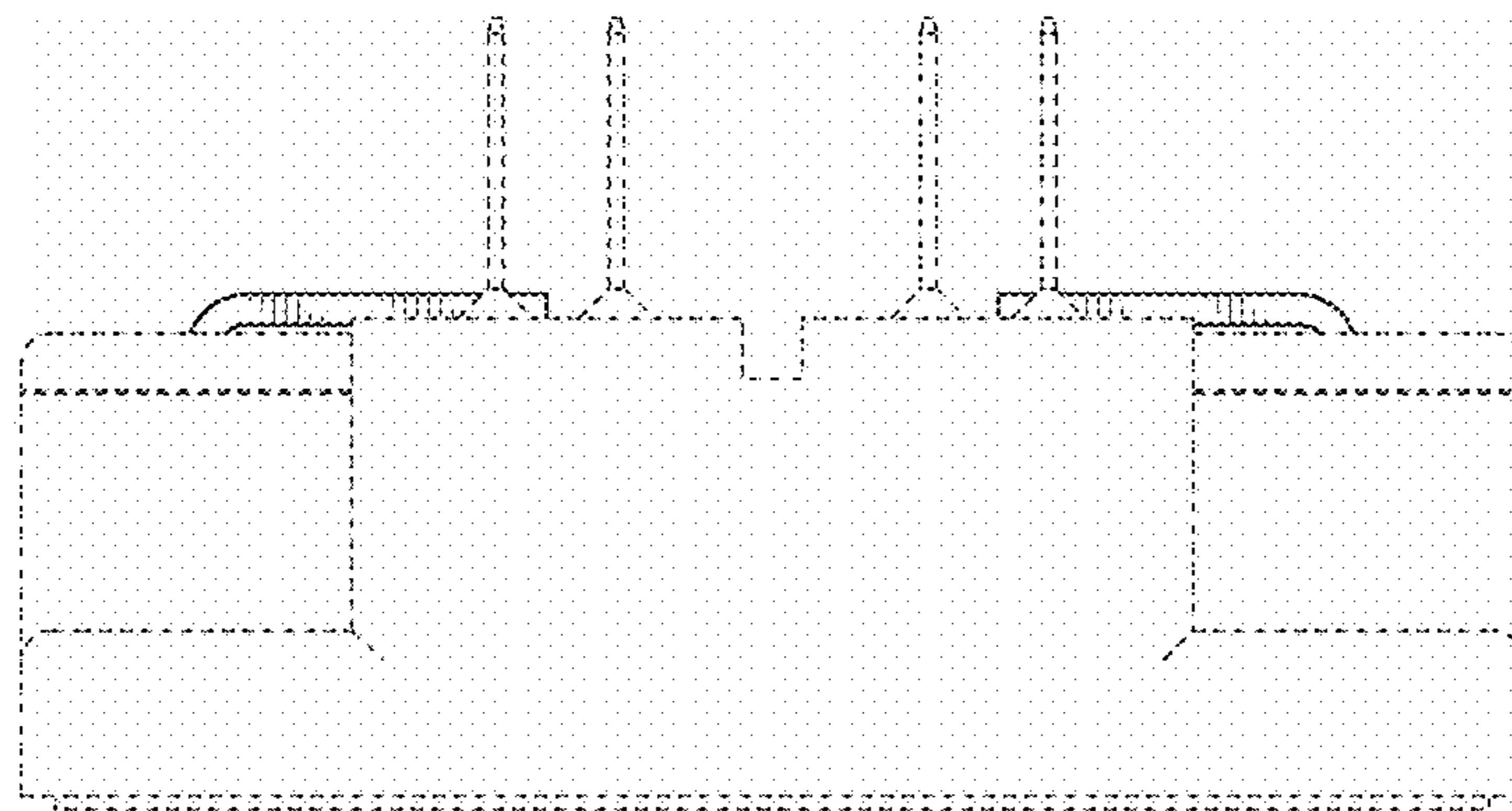


Fig.2

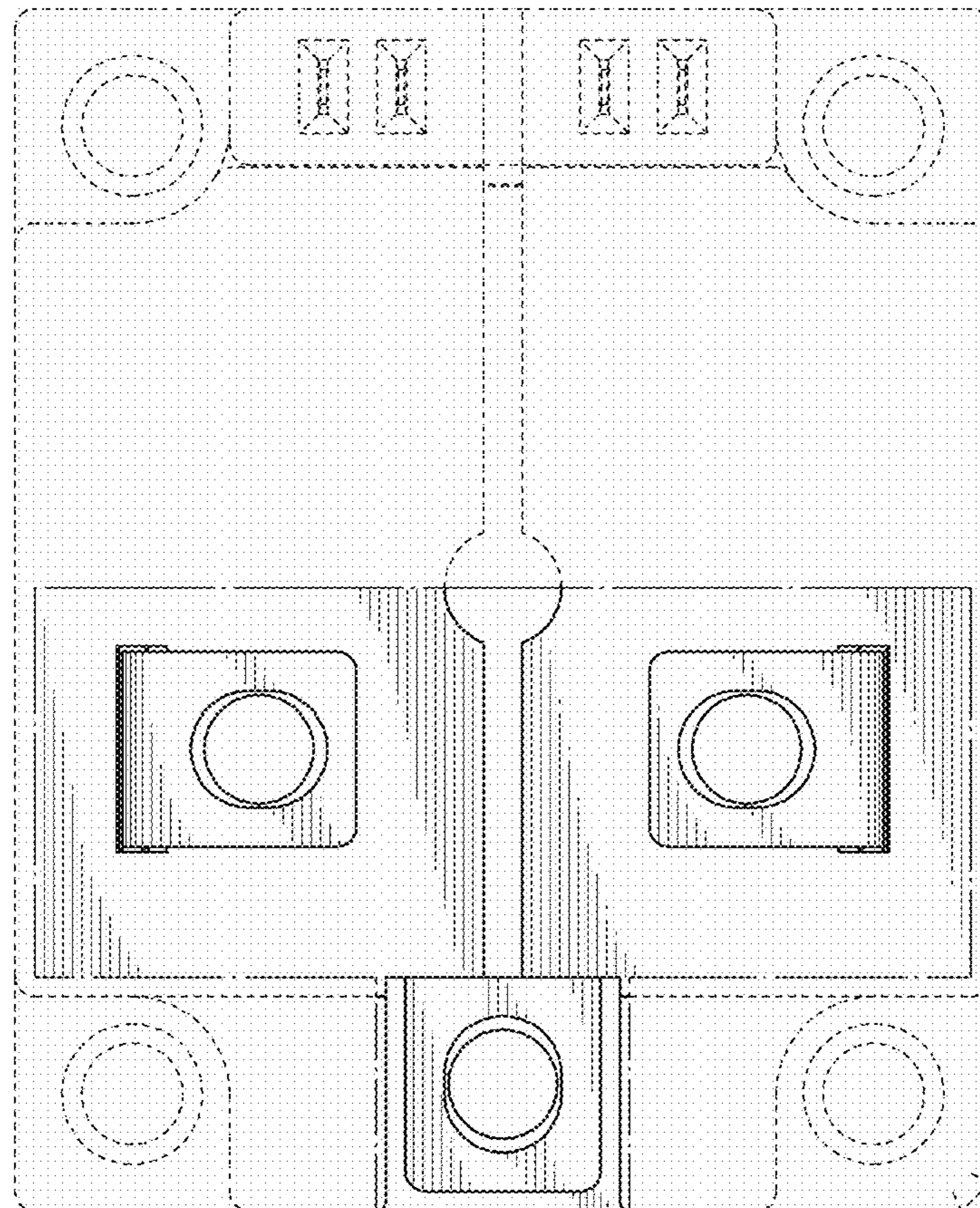


Fig.3

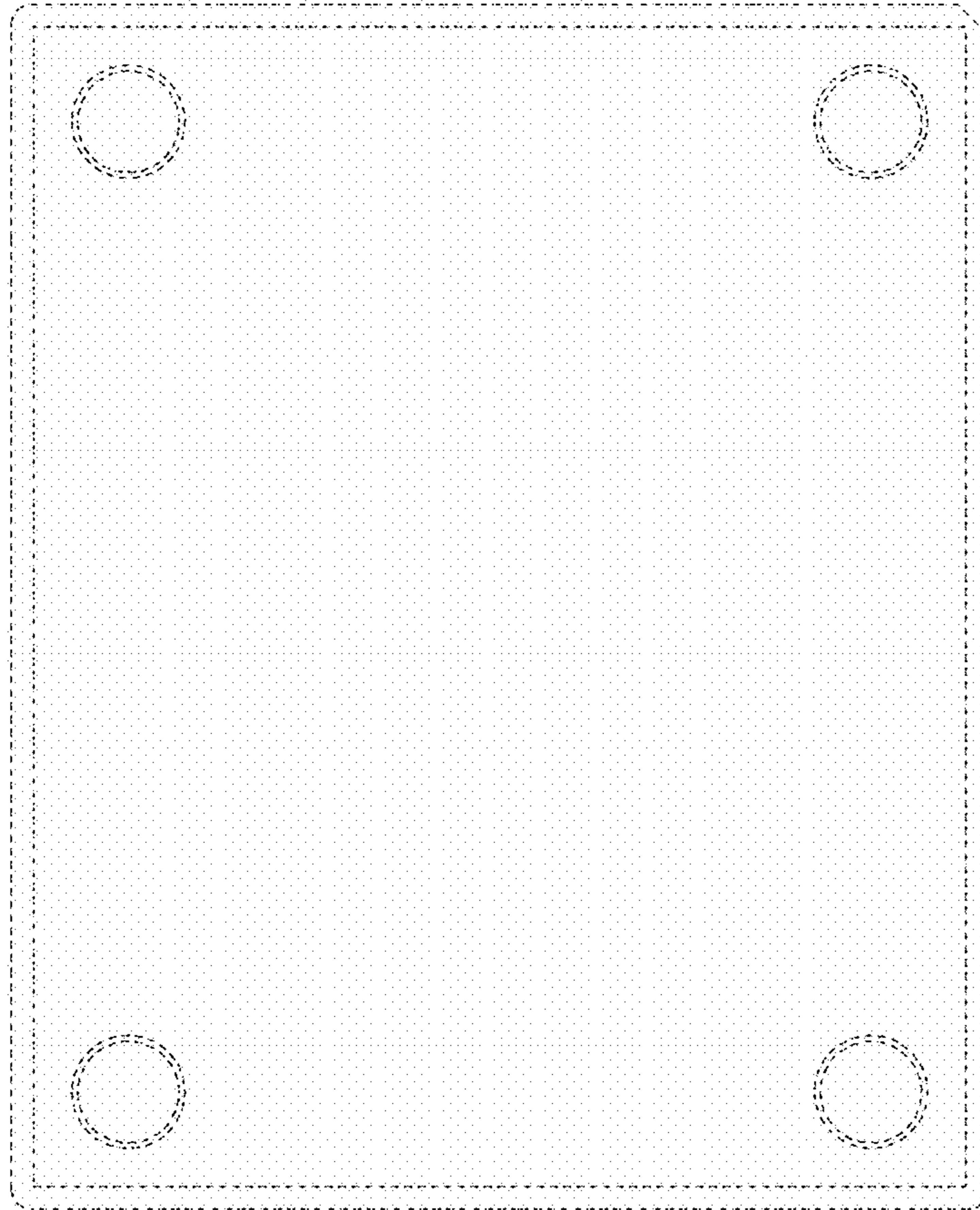


Fig.4

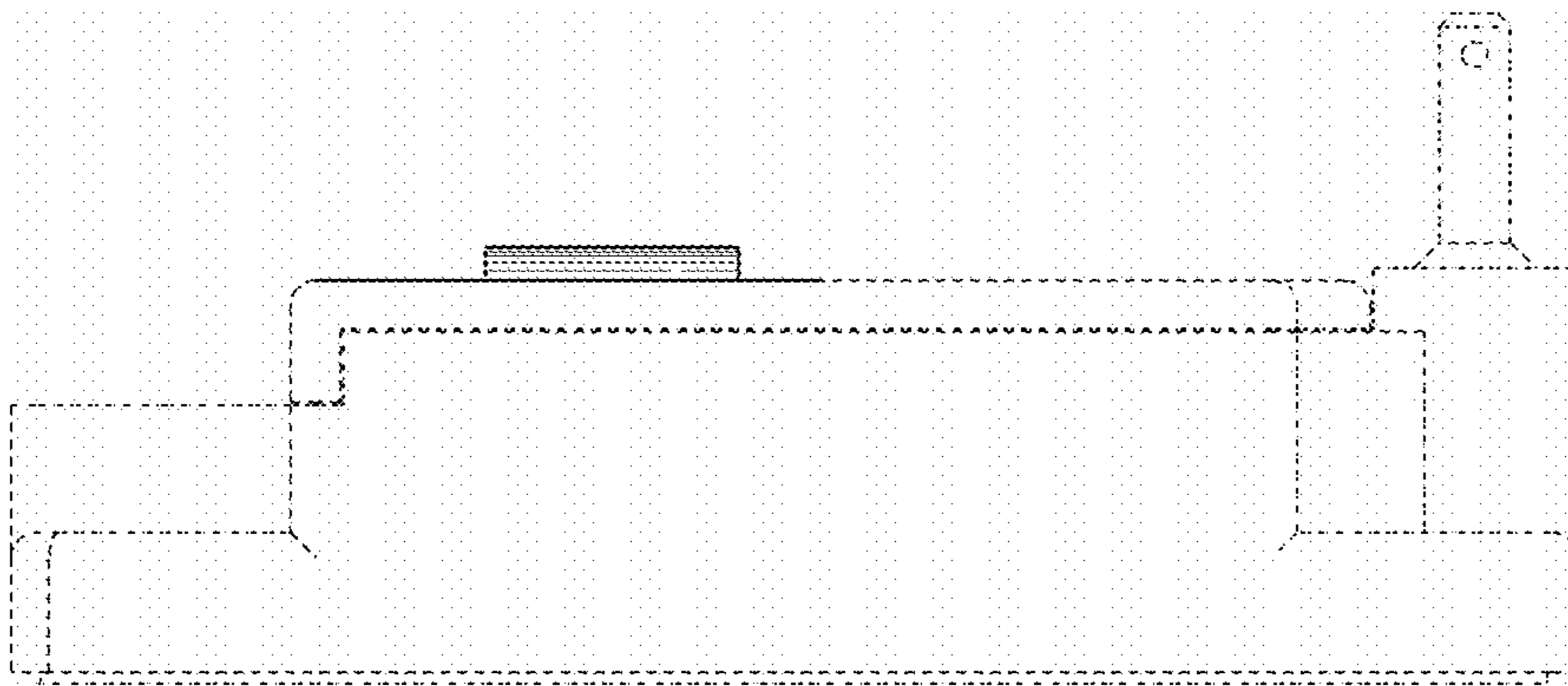


Fig.5

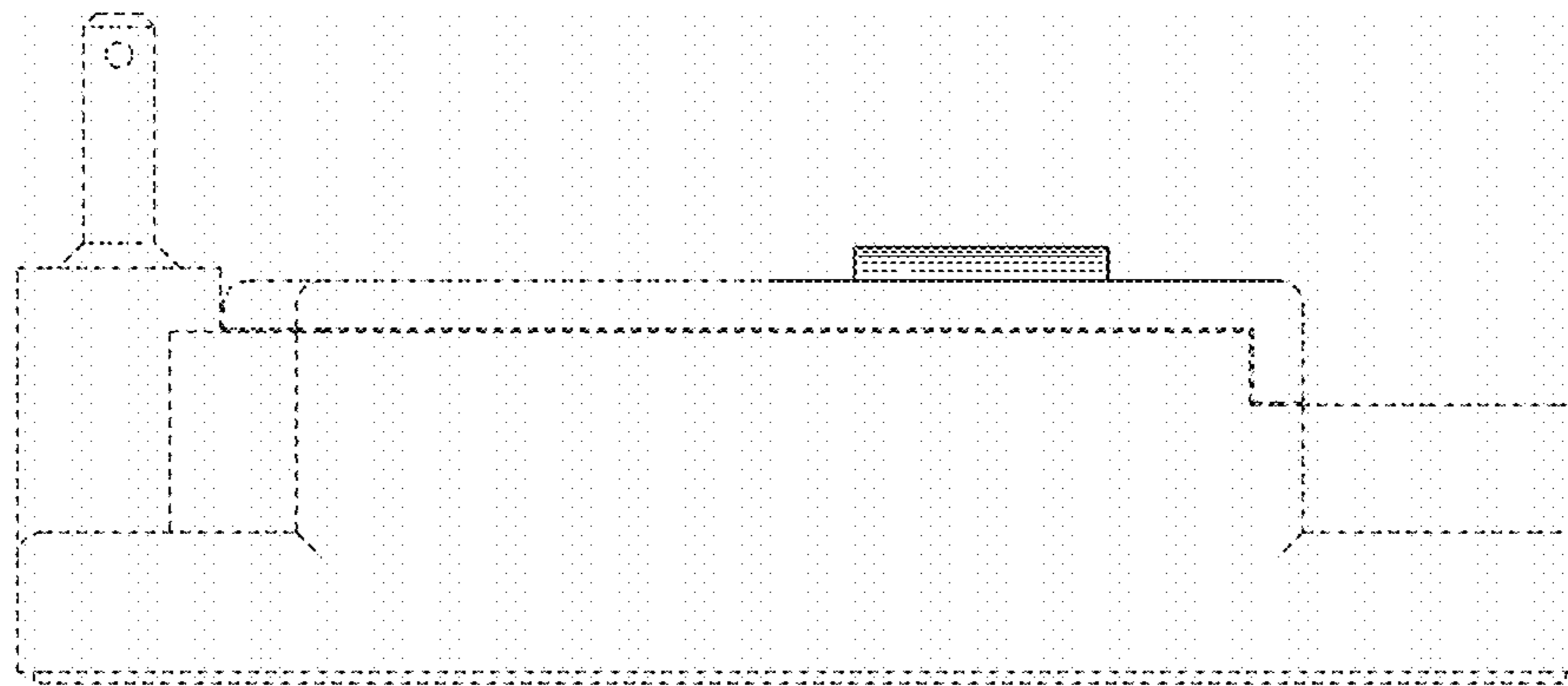


Fig.6



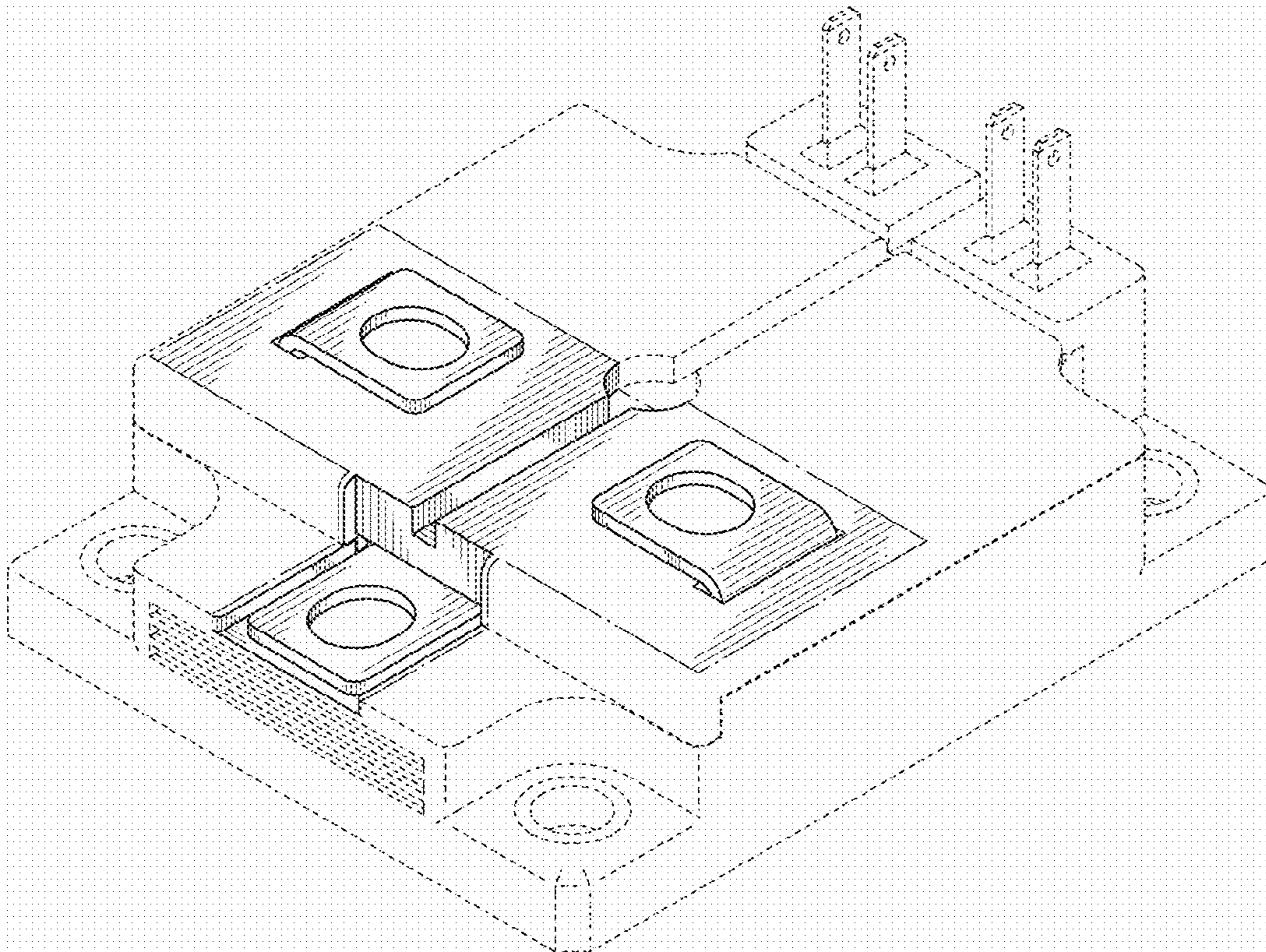


Fig.7