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(12) United States Design Patent

Shinkai

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(54) **SEMICONDUCTOR DEVICE**

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(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**

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Jun. 28, 2013 (JP) 2013-014731
Jun. 28, 2013 (JP) 2013-014732

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182
CPC . H05K 1/0228; H05K 1/0245; H05K 1/0236; H05K 1/0263; H01L 21/02433; H01L 29/04
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D68,316 S * 9/1925 Lader D5/4
2,789,344 A * 4/1957 Kaul B21C 23/03 220/581
3,579,859 A * 5/1971 Malenge A63F 9/06 40/437
D273,582 S * 4/1984 Bolt D13/182
D273,860 S * 5/1984 Bolt D13/182
D390,833 S * 2/1998 Takizawa D13/101
D436,085 S * 1/2001 Takizawa D13/182
D471,167 S * 3/2003 Ebihara D13/182
D493,152 S * 7/2004 Baker D13/182
D522,471 S * 6/2006 Sisson D13/182
D526,972 S * 8/2006 Egawa D13/180
D540,272 S * 4/2007 Higashibata D13/182
D554,084 S * 10/2007 Iizuka D13/182
D570,307 S * 6/2008 Kobayashi D13/180
D576,577 S * 9/2008 Kobayashi D13/182
D579,885 S * 11/2008 Sato D13/182
D616,395 S * 5/2010 Sato D13/182
D621,804 S * 8/2010 Sip D13/180
D674,759 S * 1/2013 Chang D13/182
D687,788 S * 8/2013 Chen D13/180
D692,843 S * 11/2013 Masuda D13/182
D695,241 S * 12/2013 Gurary D13/182
D699,201 S * 2/2014 Petsch D13/182
D699,693 S * 2/2014 Otsuka D13/182
D701,843 S * 4/2014 Masuda D13/182
D704,155 S * 5/2014 Chang D13/182
D705,184 S * 5/2014 Takahashi D13/182
(Continued)

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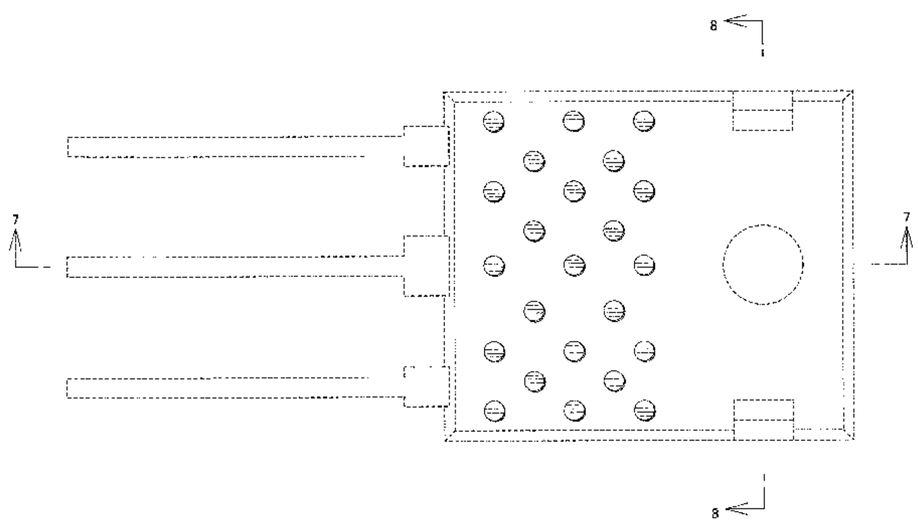
(57) **CLAIM**

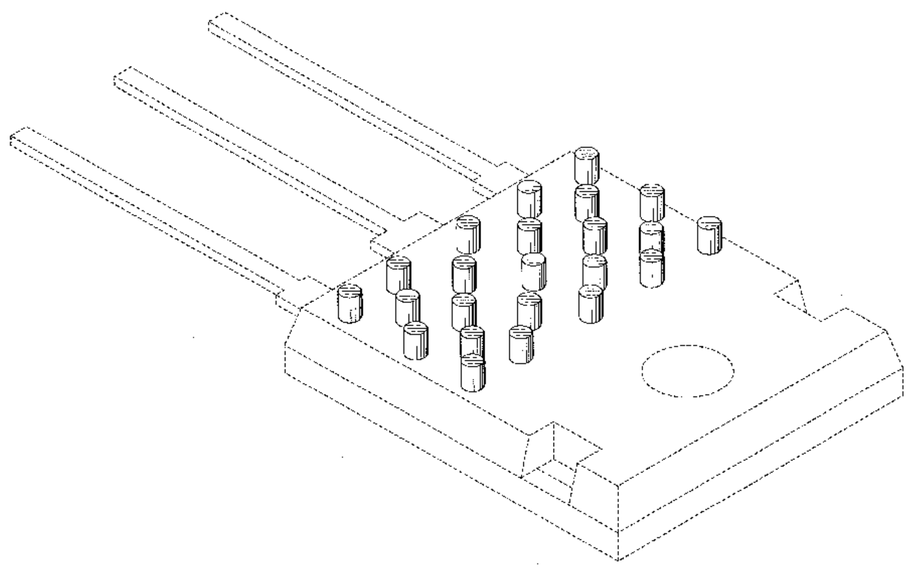
The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a semiconductor device showing my new design;
FIG. **2** is rear view thereof;
FIG. **3** is a top plan view thereof;
FIG. **4** is a bottom plan view thereof;
FIG. **5** is a right side view thereof;
FIG. **6** is a left side view thereof;
FIG. **7** is a cross sectional view taken along line **7-7** of FIG. **1** thereof;
FIG. **8** is a cross sectional view taken along line **8-8** of FIG. **1** thereof; and,
FIG. **9** is a perspective view thereof.

1 Claim, 9 Drawing Sheets





(56) **References Cited**

U.S. PATENT DOCUMENTS

D712,853	S *	9/2014	Nakamura		D13/182
D721,047	S *	1/2015	Vinciarelli		D13/182
D721,048	S *	1/2015	Nakamura		D13/182
D721,340	S *	1/2015	Nakamura		D13/182
D724,554	S *	3/2015	Motohashi		D13/182
D730,304	S *	5/2015	Matsumoto		D13/182
D731,990	S *	6/2015	Nakano		D13/182
D737,229	S *	8/2015	Masuda		D13/182
D737,230	S *	8/2015	Masuda		D13/182
2002/0027762	A1 *	3/2002	Yamaguchi	G03F 7/707	361/234
2002/0066693	A1 *	6/2002	Zhu	H01L 21/67333	206/725
2007/0086189	A1 *	4/2007	Raos	G09F 9/33	362/249.01

* cited by examiner

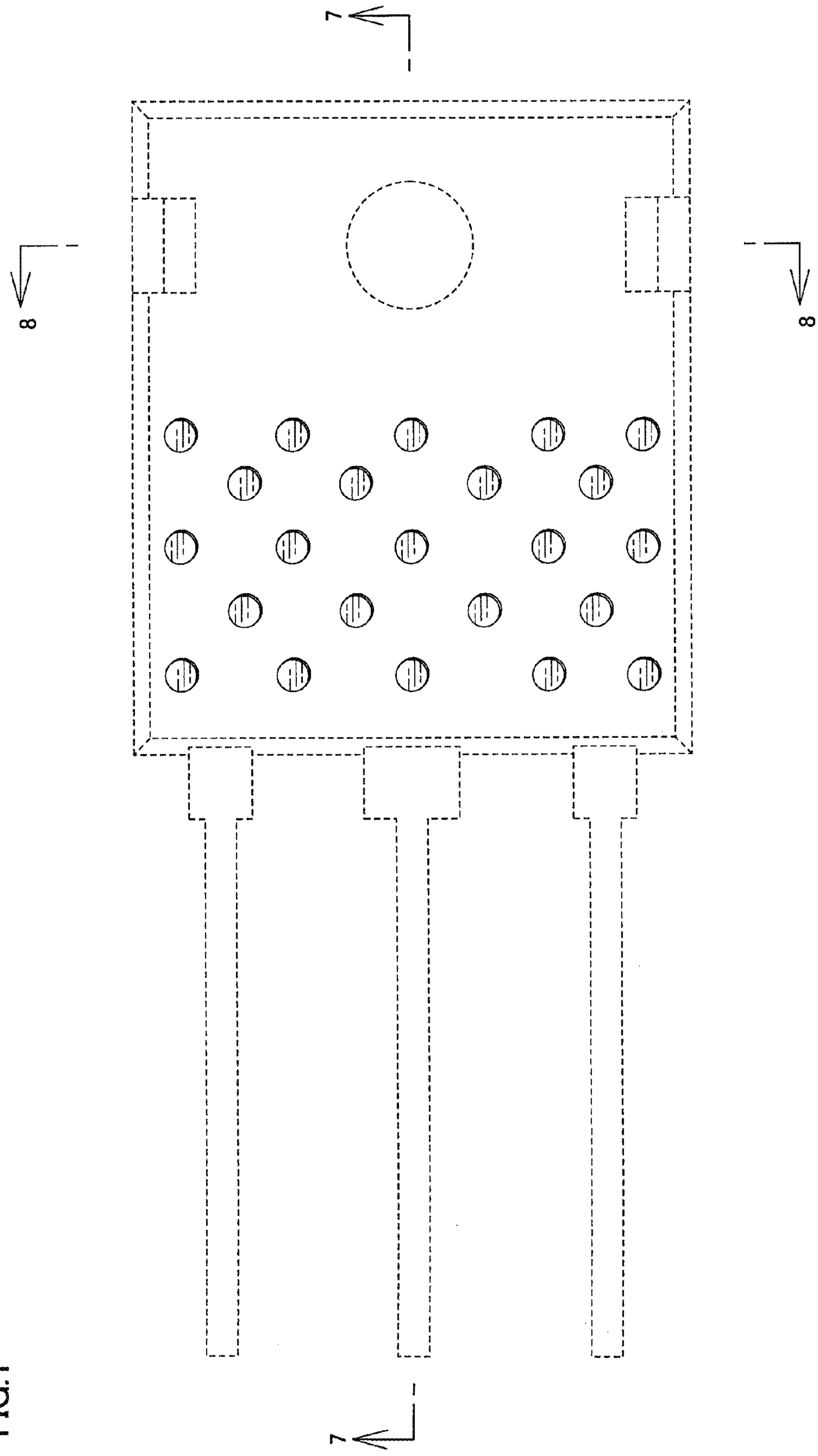


FIG.1

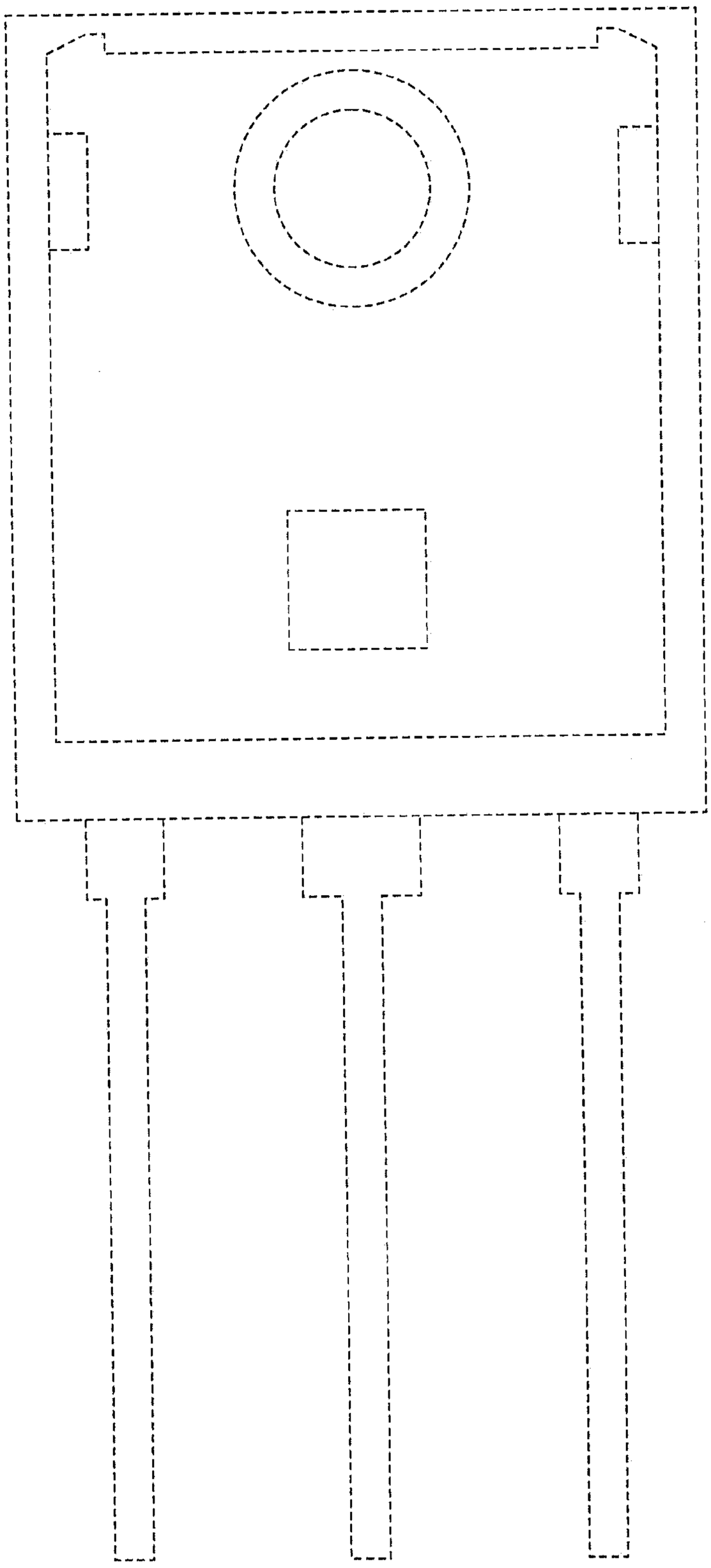


FIG.2

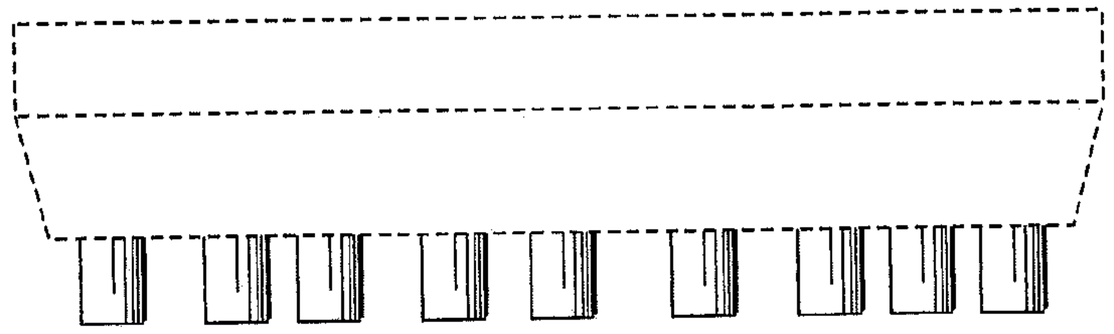


FIG.3

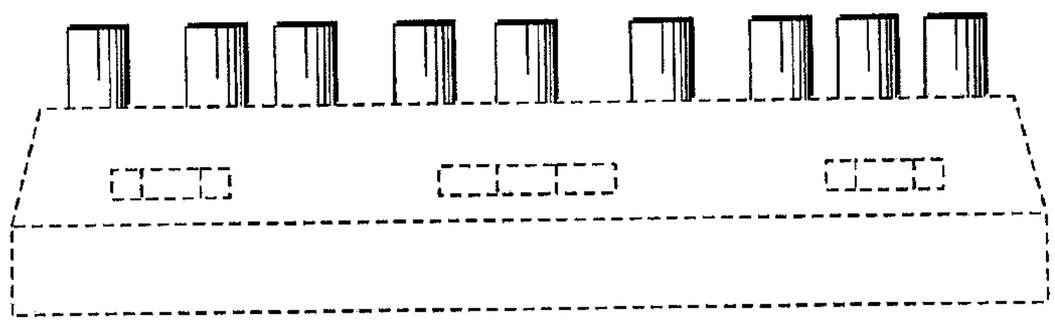


FIG.4

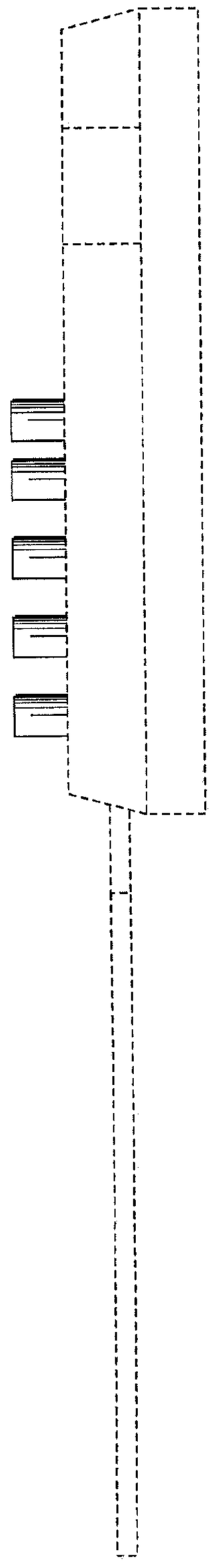


FIG.5

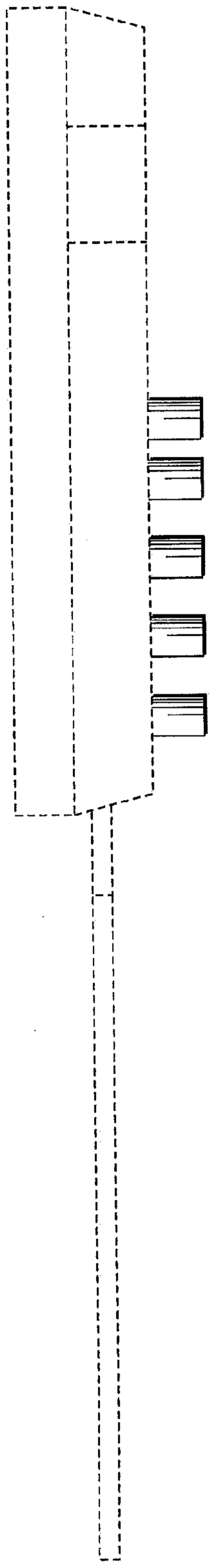


FIG.6

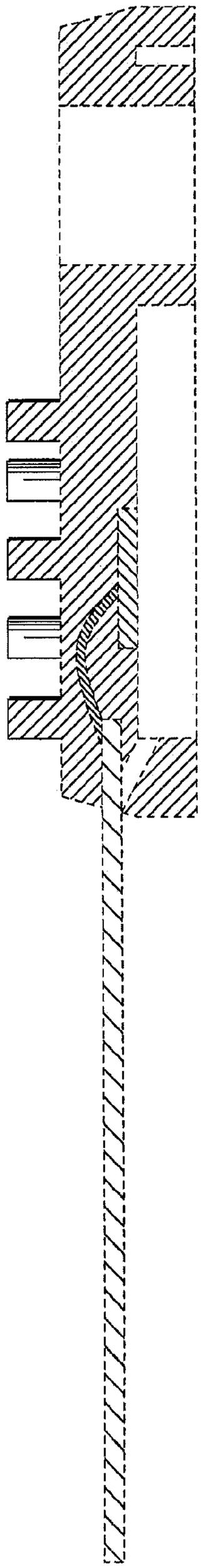


FIG.7

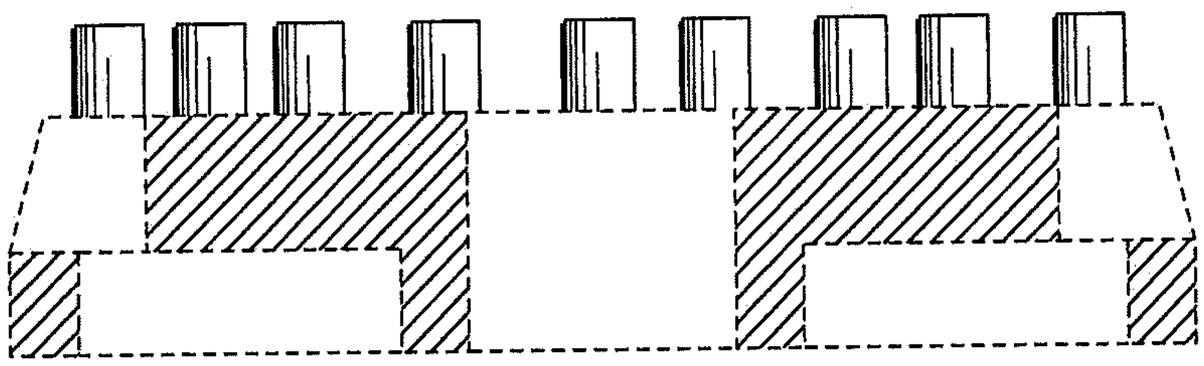


FIG.8

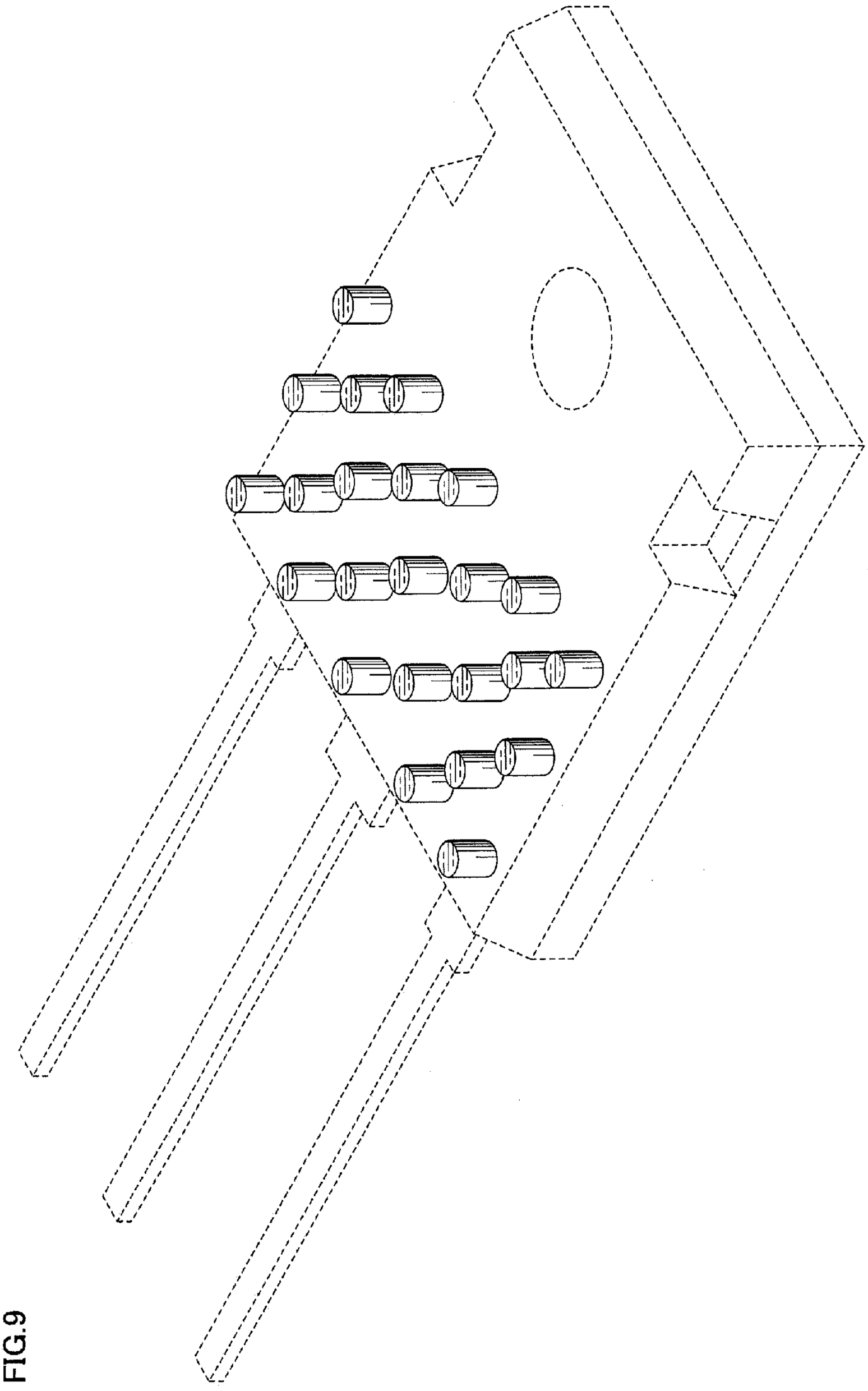


FIG.9