



US00D758843S

(12) **United States Design Patent**
Russo et al.

(10) **Patent No.:** **US D758,843 S**
(45) **Date of Patent:** **** Jun. 14, 2016**

- (54) **ELECTRONICS PACKAGE**
- (71) Applicant: **GoPro, Inc.**, San Mateo, CA (US)
- (72) Inventors: **Stephanie Russo**, San Francisco, CA (US); **Derek Yap**, San Carlos, CA (US)
- (73) Assignee: **GoPro, Inc.**, San Mateo, CA (US)
- (**) Term: **14 Years**
- (21) Appl. No.: **29/523,184**
- (22) Filed: **Apr. 7, 2015**
- (51) **LOC (10) Cl.** **09-03**
- (52) **U.S. Cl.**
USPC **D9/418**
- (58) **Field of Classification Search**
USPC D9/414-419, 432, 499, 687, 517, 445;
D20/15; D23/366; D13/184;
206/315.1, 320, 783; D27/189;
229/125.17; 132/229; D30/101;
D28/73; D7/679; D21/311
CPC B65D 85/64; B65D 5/5038; B65D 81/36;
B65D 5/14; B65D 25/10; A45D 4/16
See application file for complete search history.

D288,452 S *	2/1987	Takizawa	D21/311
D317,718 S *	6/1991	Carol	D9/418
5,100,052 A *	3/1992	Vajtay	B65D 5/14 229/125.17
D405,007 S *	2/1999	Naas, Sr.	D27/189
6,047,833 A *	4/2000	Salomon	B65D 25/10 206/315.1
D453,106 S *	1/2002	Peltrault	D9/687
D508,026 S *	8/2005	Phipps	D13/184
D520,623 S *	5/2006	Lablaine	D23/366
D531,043 S *	10/2006	Houtart	D9/432
D553,488 S *	10/2007	Pacheco	D9/418
D556,566 S *	12/2007	Steele, IV	D9/418
D572,581 S *	7/2008	Steele, IV	D9/517
D685,433 S *	7/2013	De Iuliis	D20/15
D691,884 S *	10/2013	Kwon	D9/415
D728,368 S *	5/2015	Alschbach	D9/445
D747,960 S *	1/2016	Sculler	D9/418

* cited by examiner

Primary Examiner — Holly Baynham

Assistant Examiner — Rhea Shields

(74) *Attorney, Agent, or Firm* — Fenwick & West LLP

(57) **CLAIM**

The ornamental design for an electronics package, as shown.

DESCRIPTION

FIG. 1 is a front, top and left side perspective view of an electronics package showing our new design;

FIG. 2 is a front elevational view thereof;

FIG. 3 is a rear elevational view thereof;

FIG. 4 is a right side elevational view thereof;

FIG. 5 is a left side elevational view thereof;

FIG. 6 is a top plan view thereof; and,

FIG. 7 is a bottom plan view thereof.

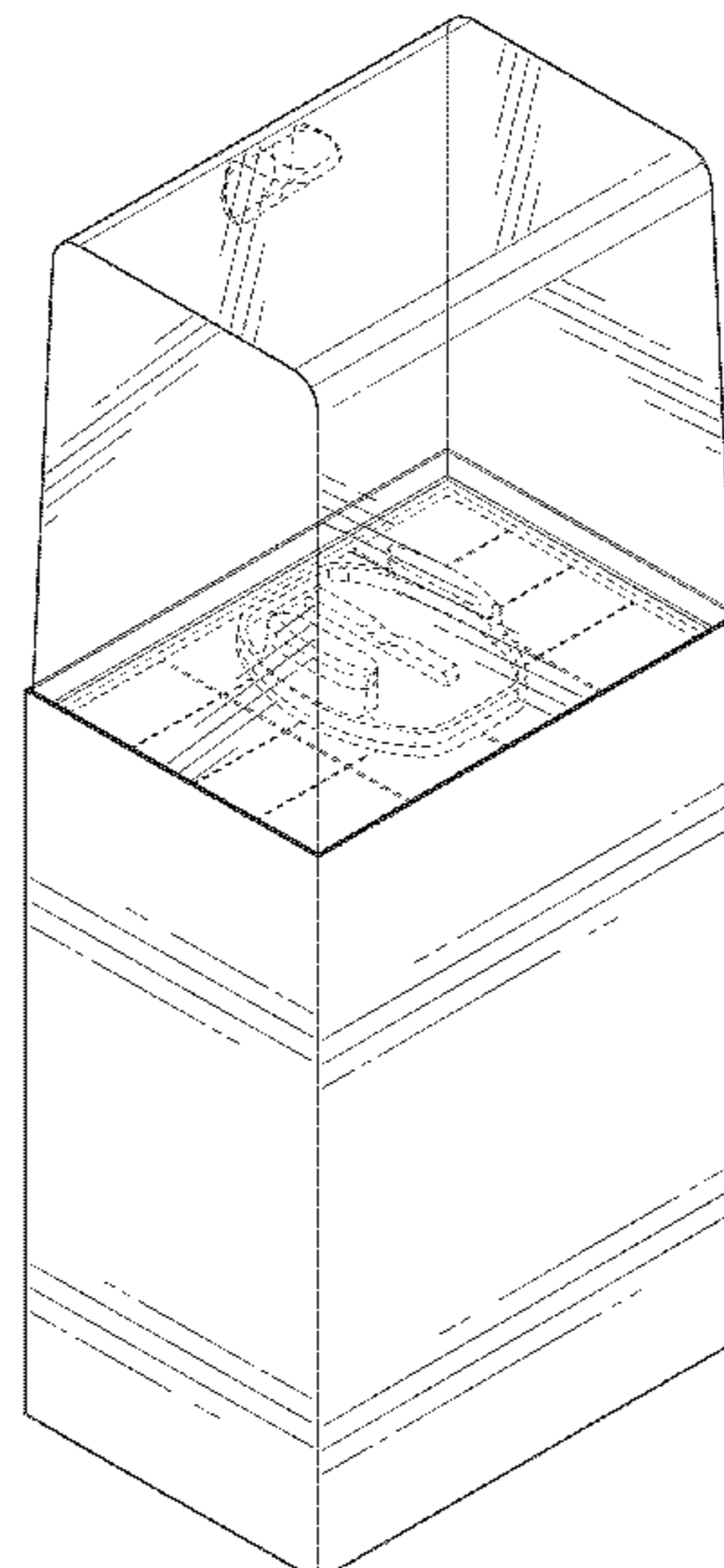
The broken lines in the drawings showing portions of the electronics package are included for the purpose of illustrating environmental structure and form no part of the claimed design.

1 Claim, 6 Drawing Sheets

(56) **References Cited**

U.S. PATENT DOCUMENTS

3,410,985 A *	11/1968	Giacchero	A45D 4/16 132/229
3,616,986 A *	11/1971	Wolfe	B65D 85/64 206/320
4,109,786 A *	8/1978	Roccaforte	B65D 5/5038 206/783
D259,922 S *	7/1981	Seki	D30/101
4,317,515 A *	3/1982	Feeley	B65D 81/36 206/315.1
D269,467 S *	6/1983	Mann	D28/73
D287,209 S *	12/1986	Bounds	D7/679



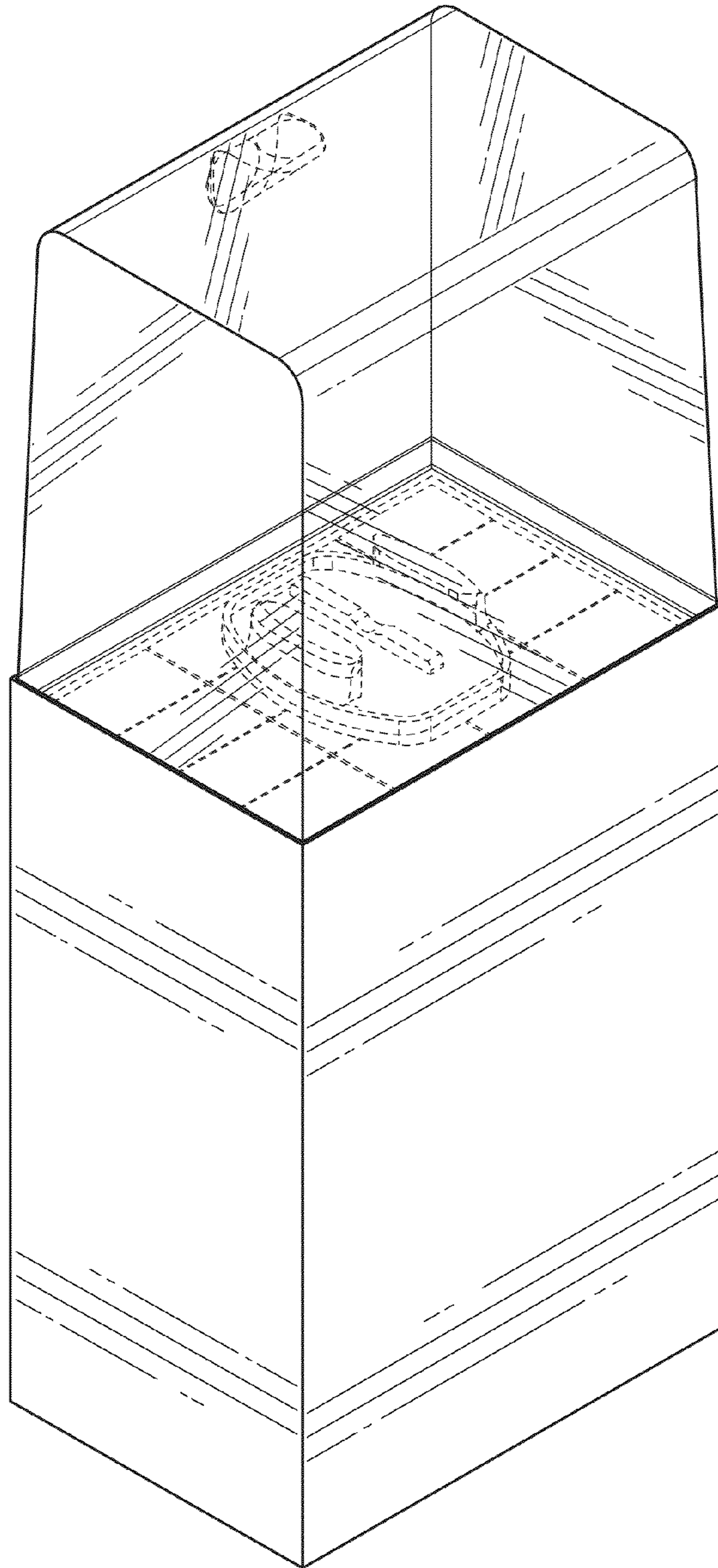


FIG. 1

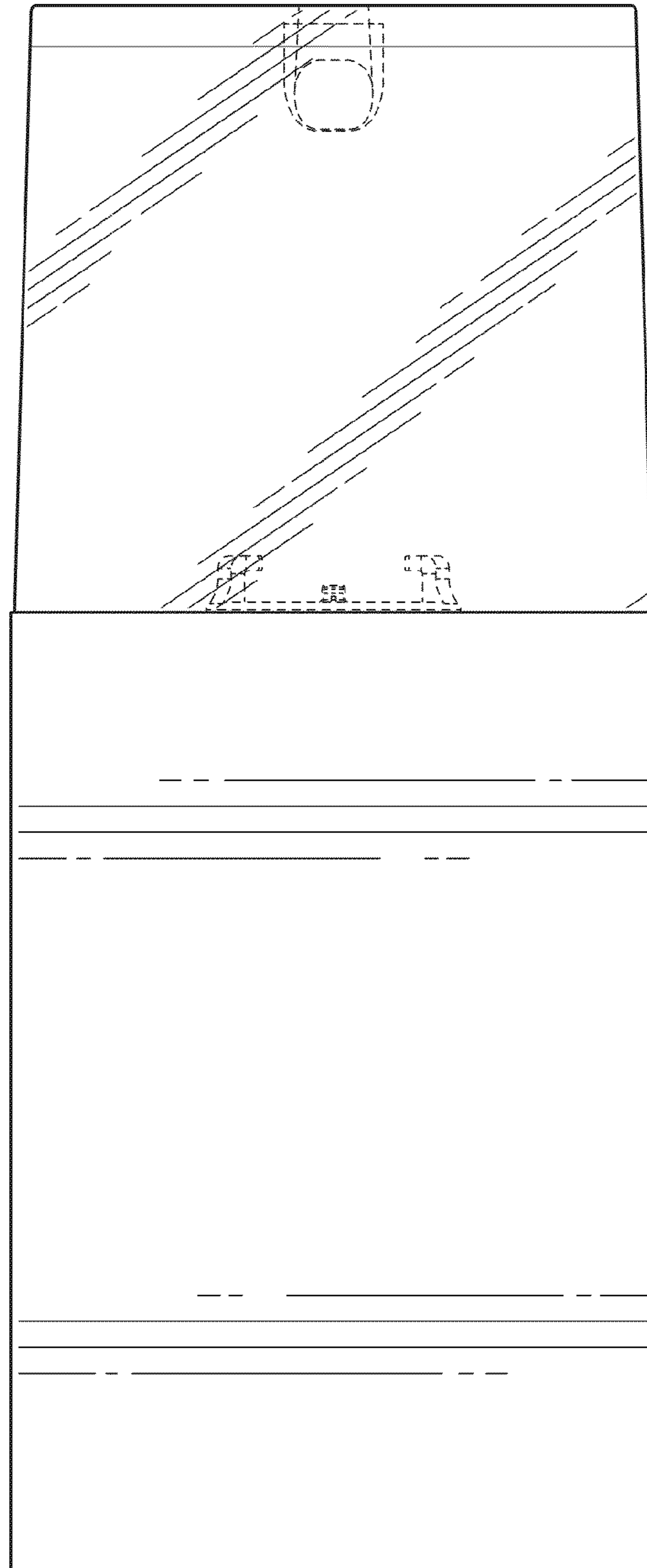


FIG. 2

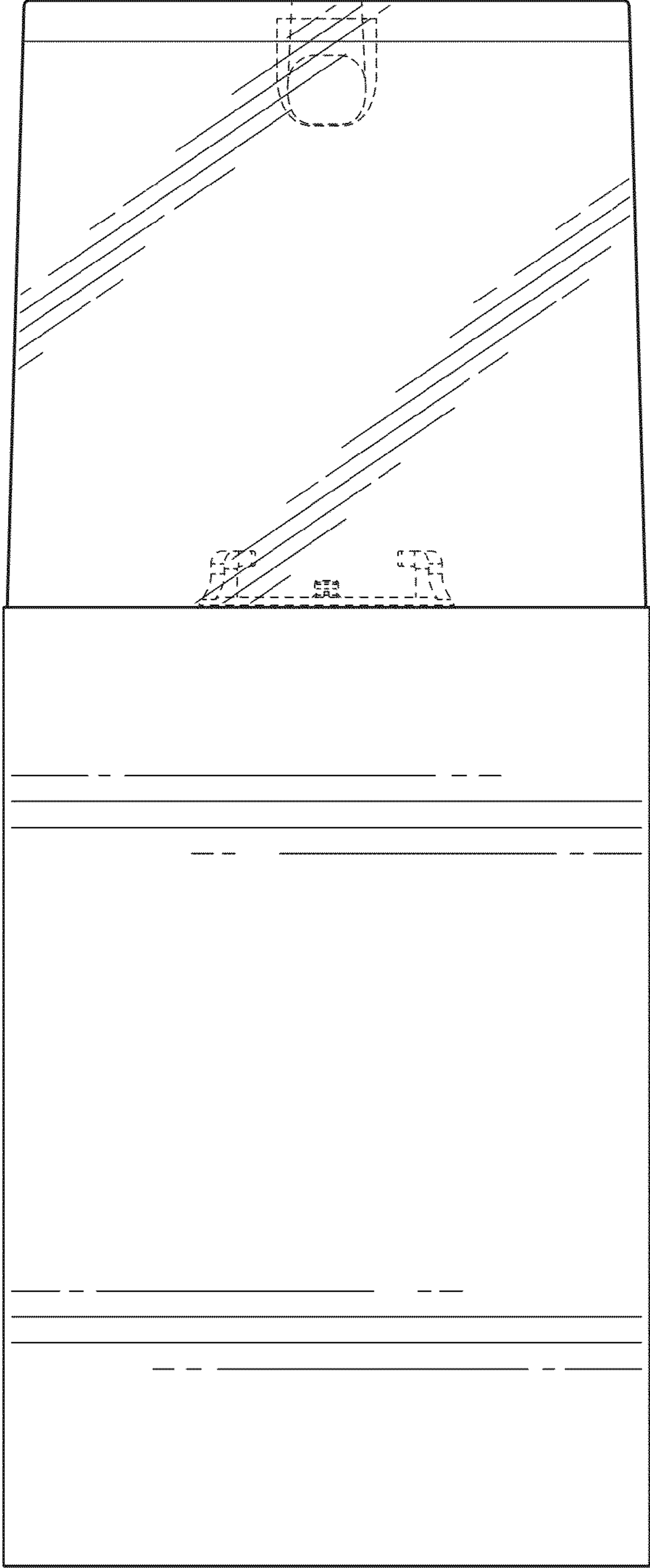


FIG. 3

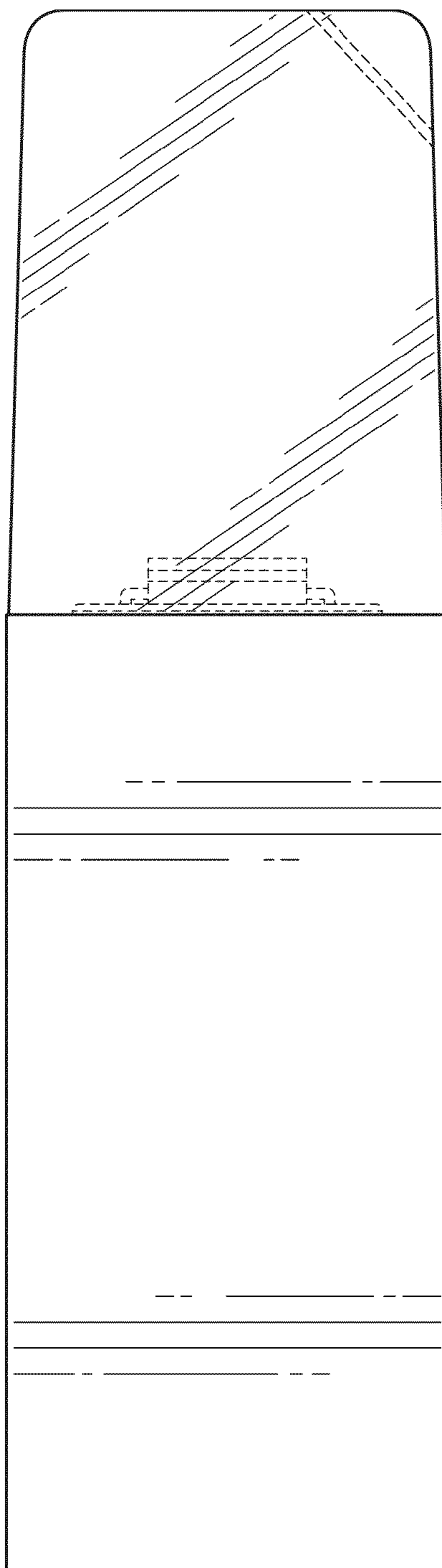


FIG. 4

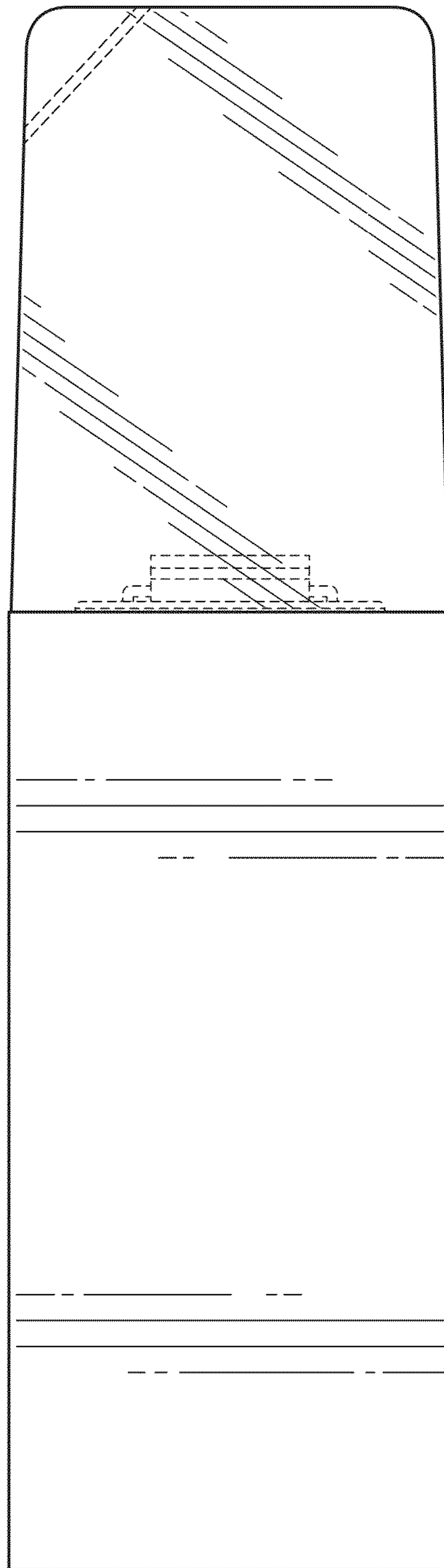


FIG. 5

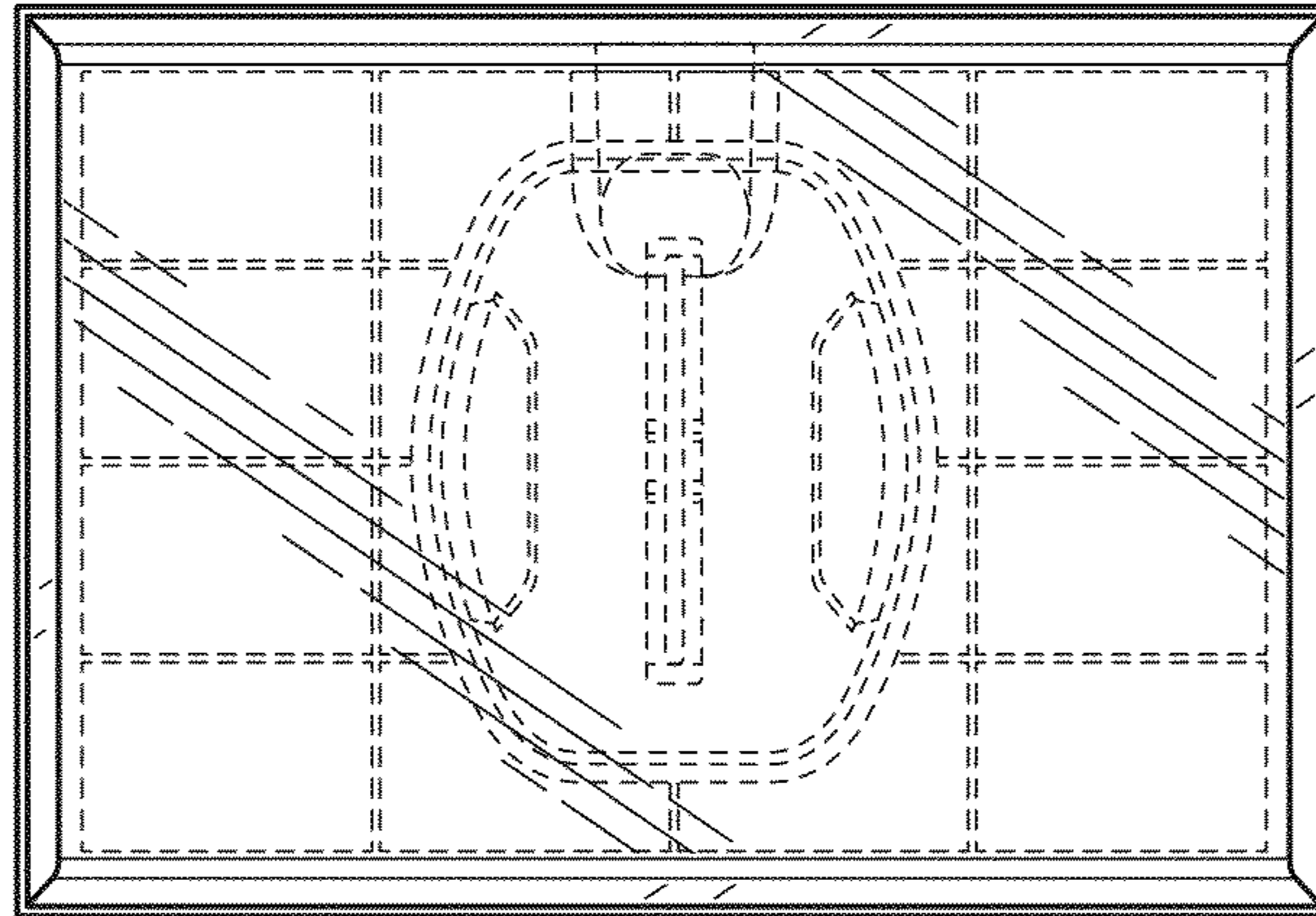


FIG. 6

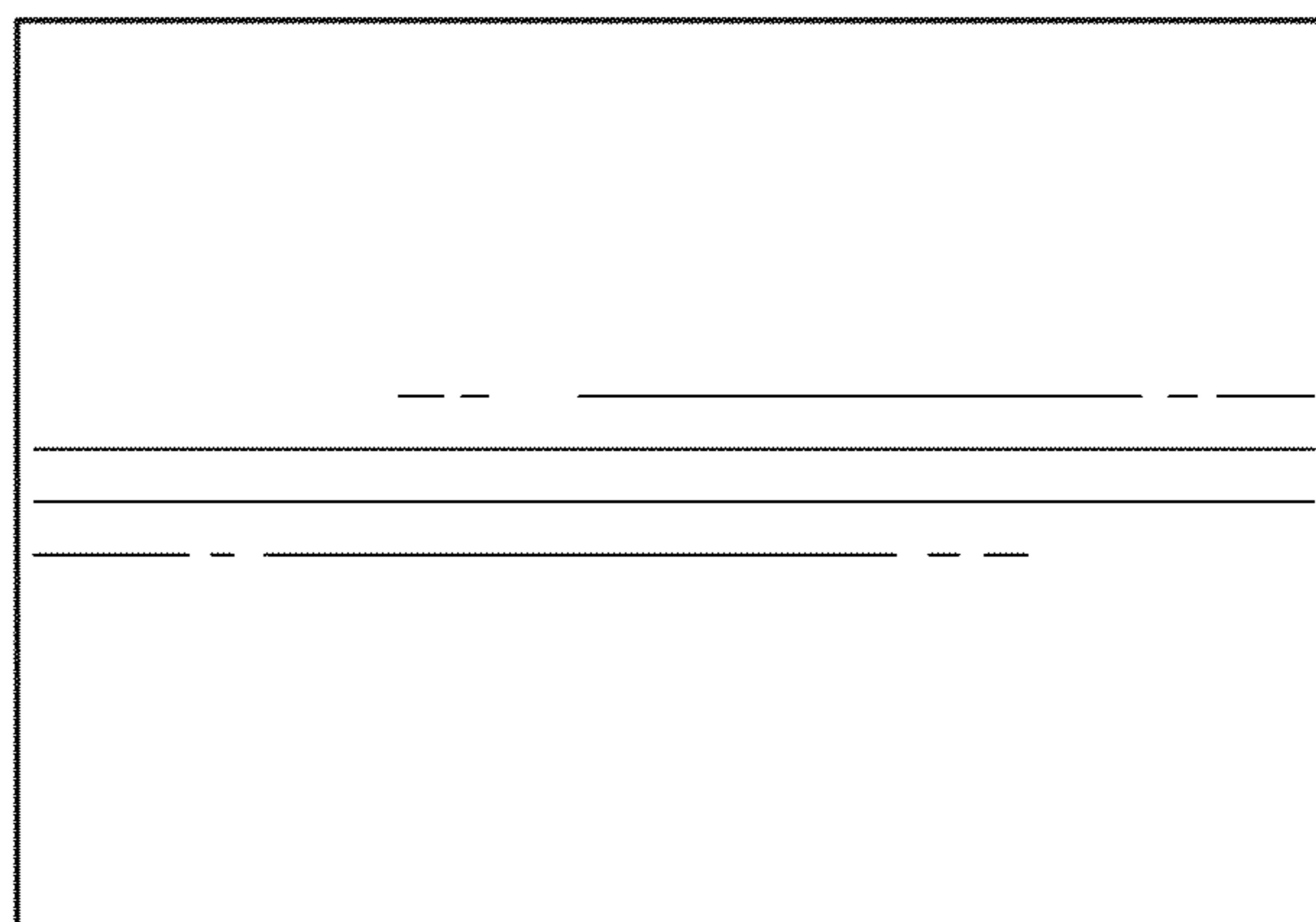


FIG. 7