



US00D753002S

(12) **United States Design Patent**  
**Russell**

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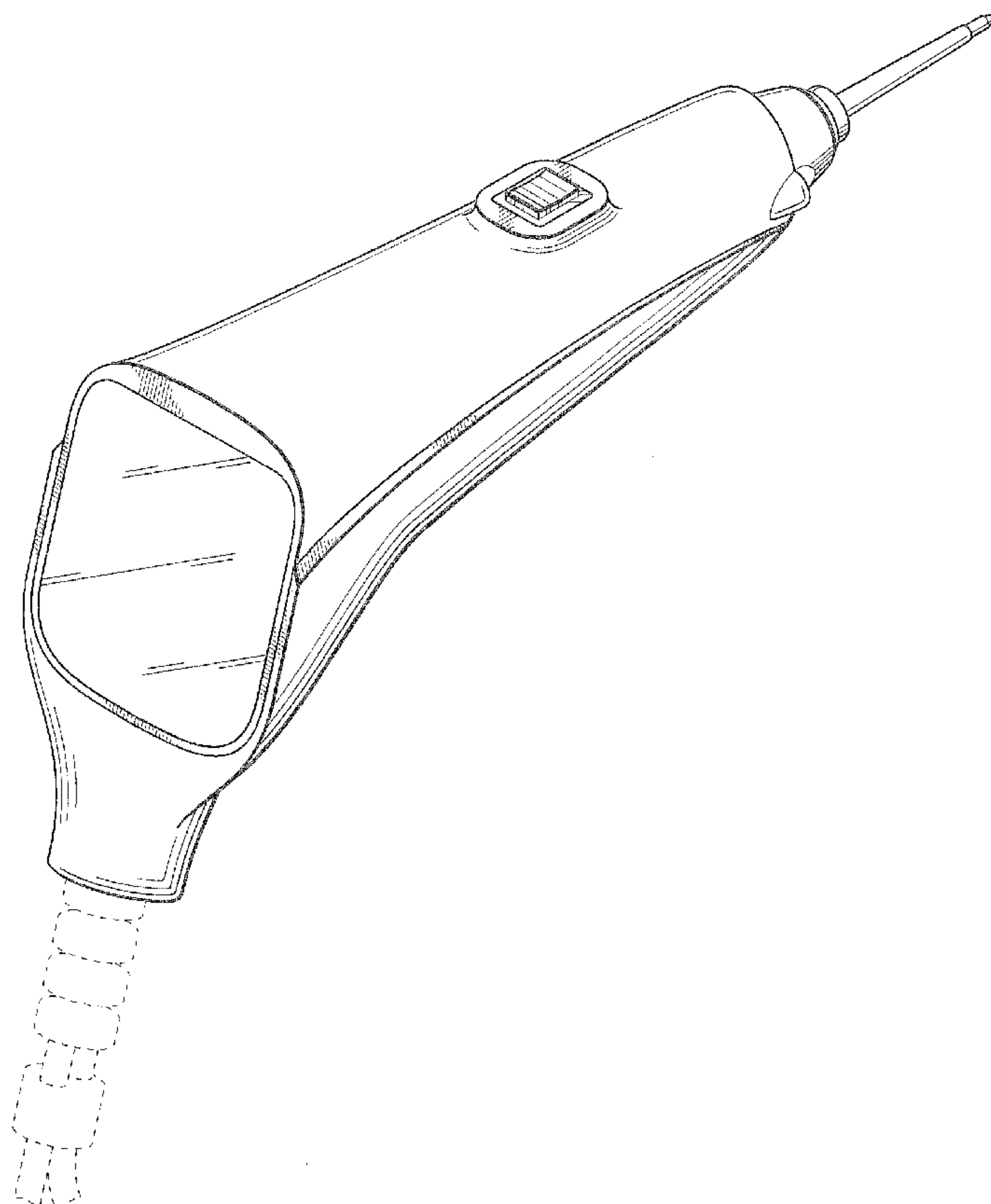
- (54) **DIAGNOSTIC CIRCUIT TEST DEVICE**
  - (71) Applicant: **Wayne Russell**, Ontario, CA (US)
  - (72) Inventor: **Wayne Russell**, Ontario, CA (US)
  - (73) Assignee: **Power Probe TEK, LLC**, Brea, CA (US)
  - (\*\*) Term: **14 Years**
  - (21) Appl. No.: **29/514,629**
  - (22) Filed: **Jan. 14, 2015**
  - (51) **LOC (10) Cl.** ..... **10-04**
  - (52) **U.S. Cl.**  
USPC ..... **D10/78**
  - (58) **Field of Classification Search**  
USPC ..... D10/78  
CPC ..... G01R 19/14; G01R 19/145; G01R 1/15;  
G01R 19/155; G01R 1/07; G01R 1/06788;  
G01R 1/06794; G01R 1/071; G01R 1/072;  
G01R 1/067; G01R 1/06705; G01R 1/06711;  
G01R 1/06733; G01R 1/06738; G01R  
1/06744; G01R 1/0675; G01R 1/06
- See application file for complete search history.

- (56) **References Cited**  
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D345,117 S \* 3/1994 Pacetti ..... D10/112  
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*Primary Examiner* — Antoine D Davis  
(74) *Attorney, Agent, or Firm* — Rutan & Tucker LLP; Hani Z. Sayed

(57) **CLAIM**  
The ornamental design for an diagnostic circuit test device, as shown and described.

**DESCRIPTION**  
FIG. 1 is a top, front, right side perspective view of the diagnostic circuit test device of the present invention; FIG. 2 is a left side elevation view, the right side elevation view being a mirror image; FIG. 3 is a front elevation view; FIG. 4 is a rear elevation view; FIG. 5 is a top plan view; and, FIG. 6 is a bottom plan view.  
The broken lines of the bottom surface shown in the drawings views are included for the purpose of illustrating environmental structure and form no part of the claimed invention.

**1 Claim, 4 Drawing Sheets**



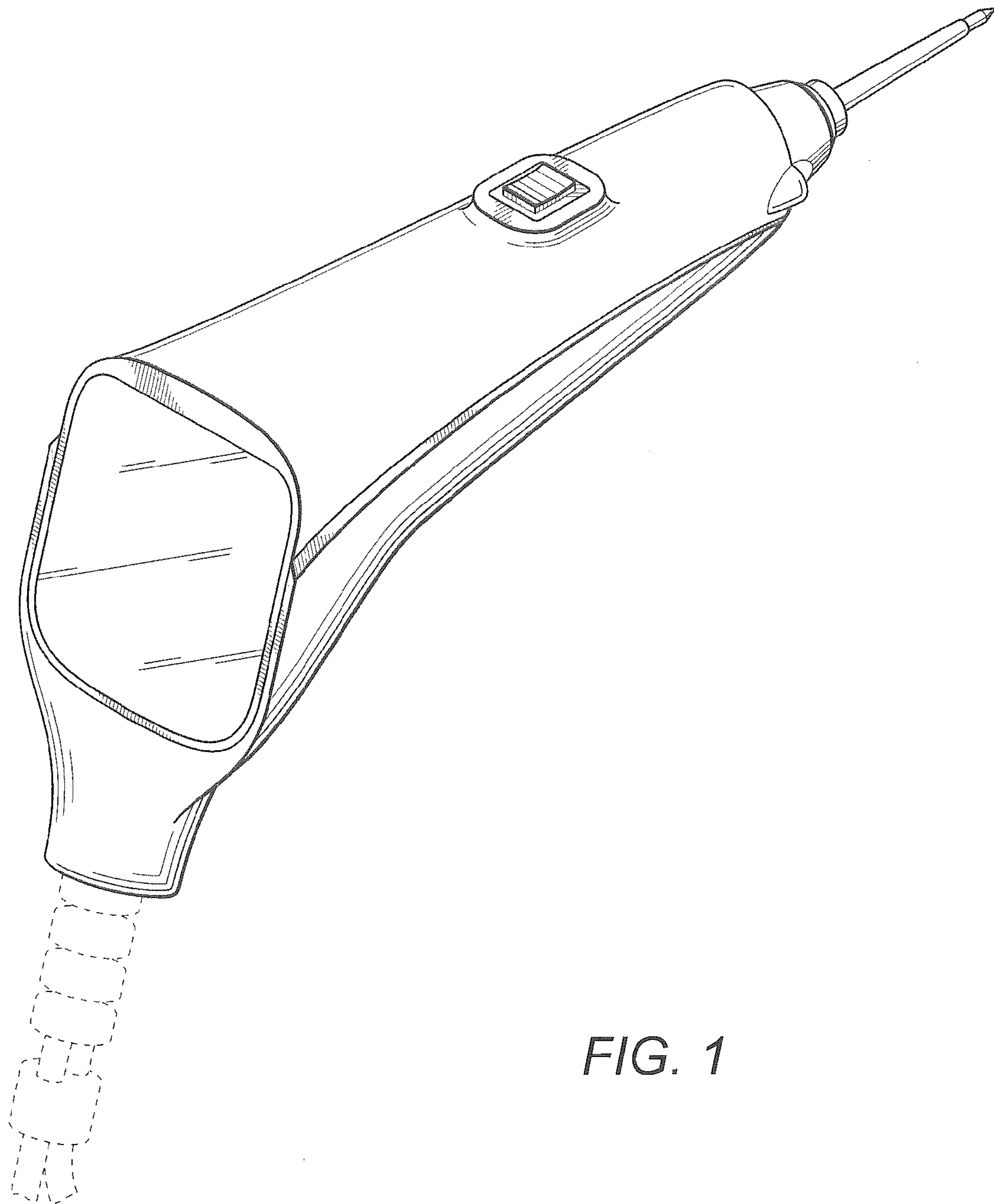


FIG. 1

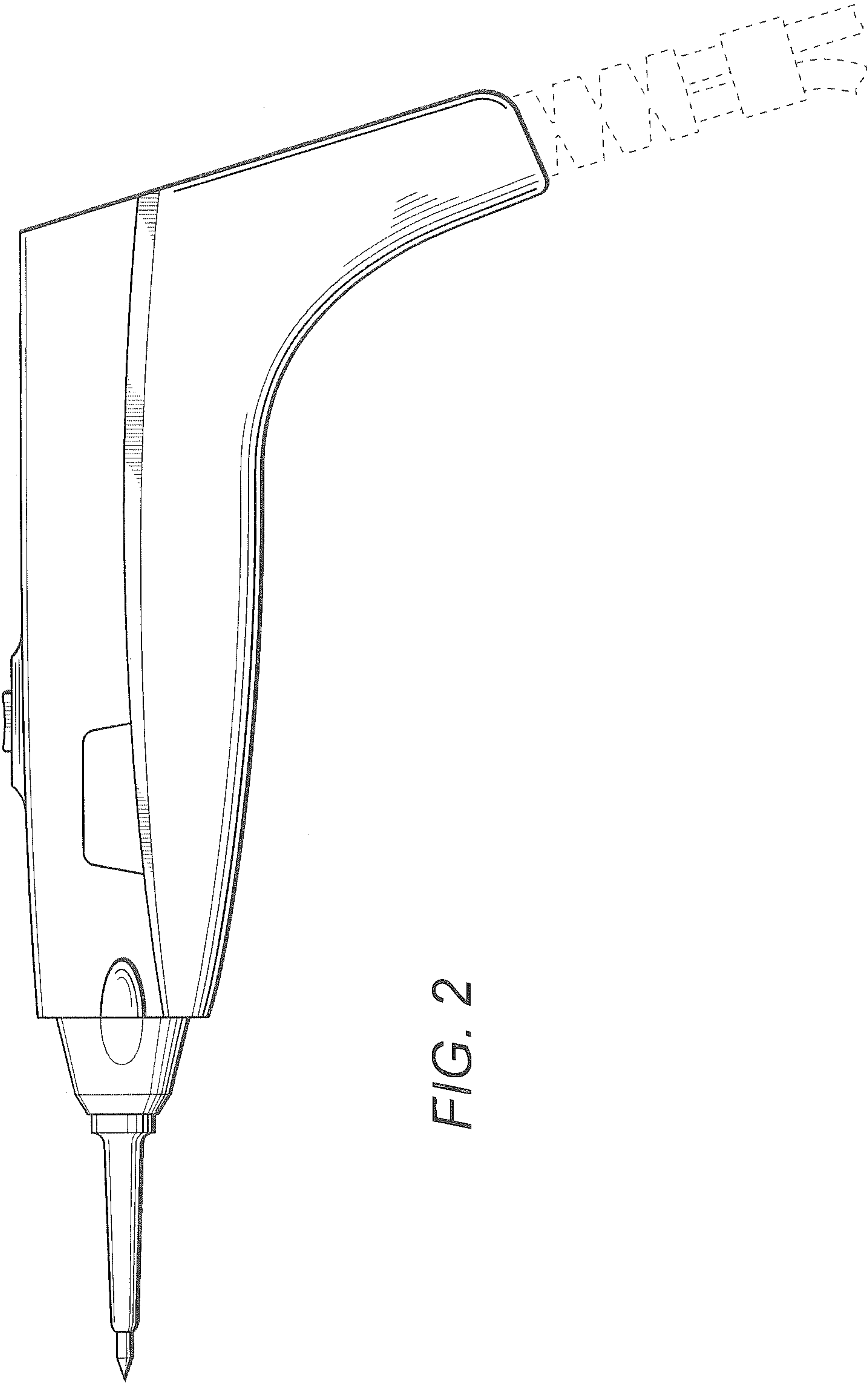


FIG. 2

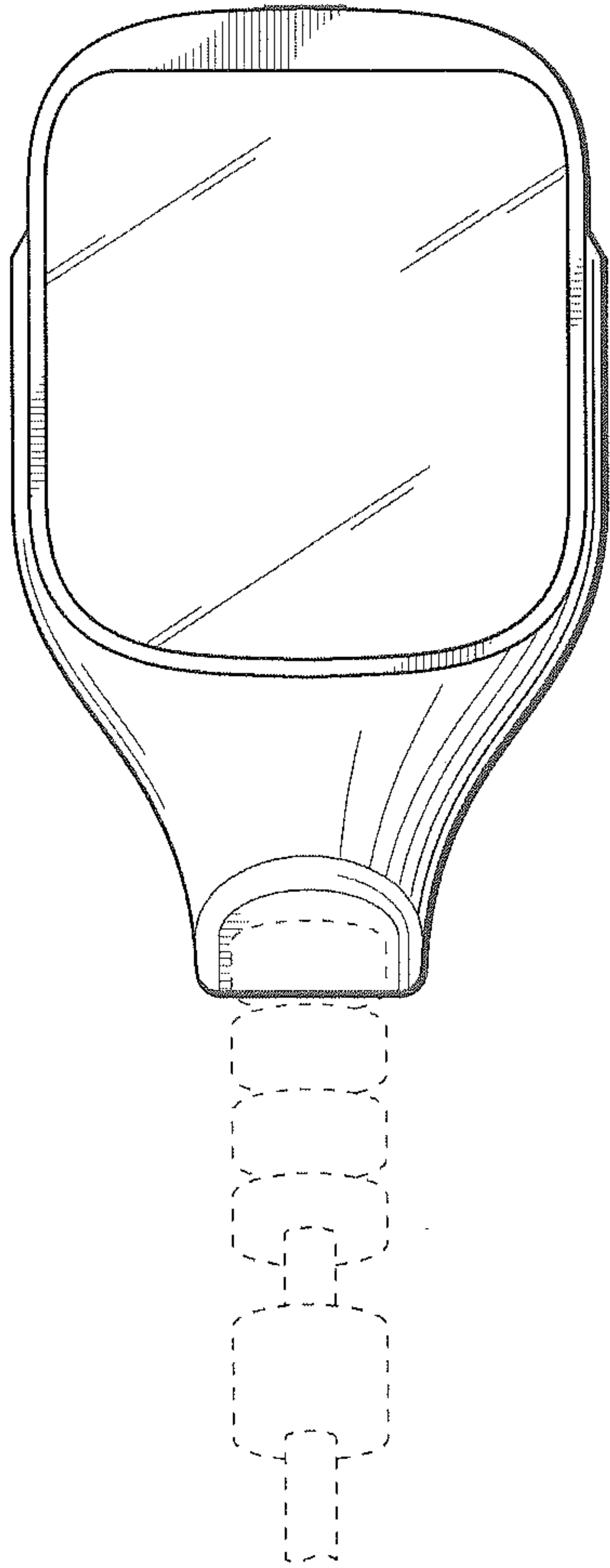


FIG. 3

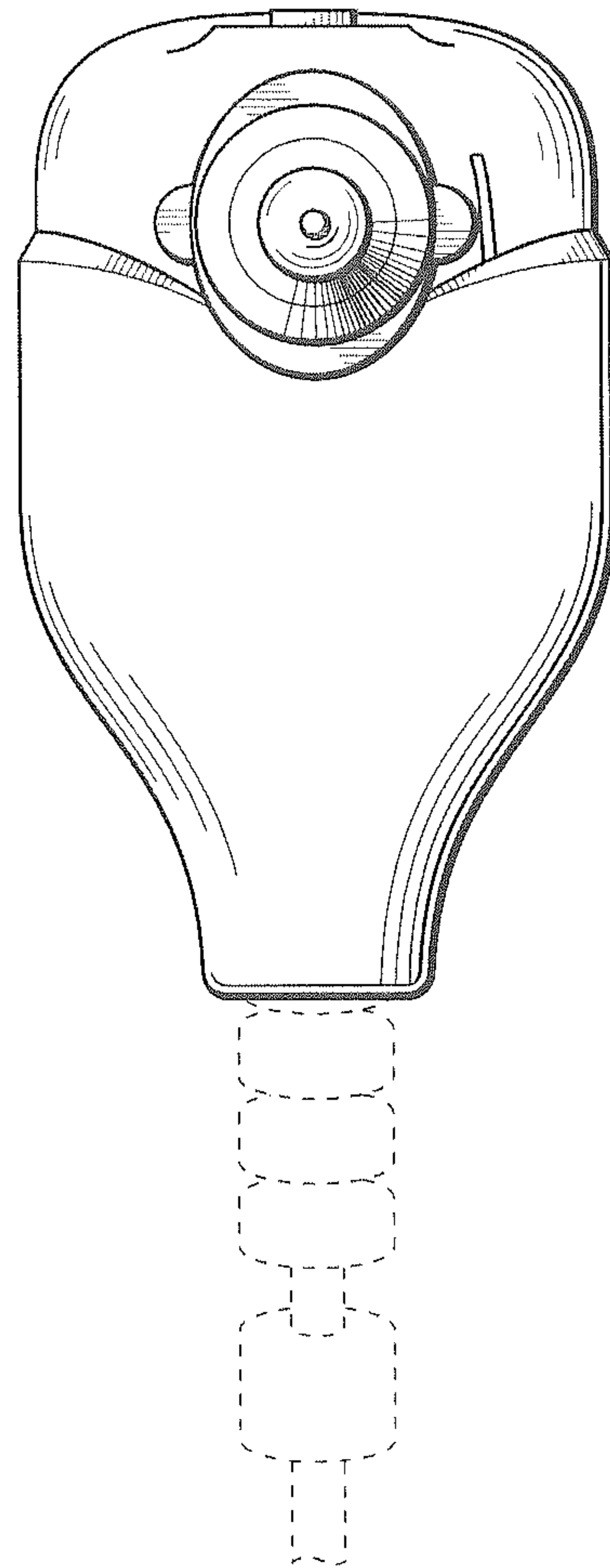


FIG. 4

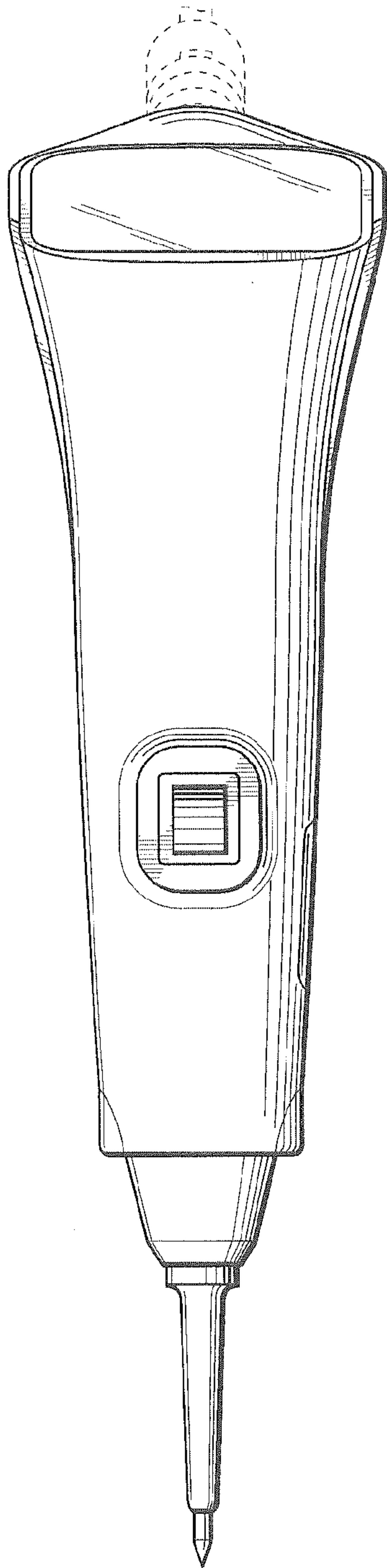


FIG. 5

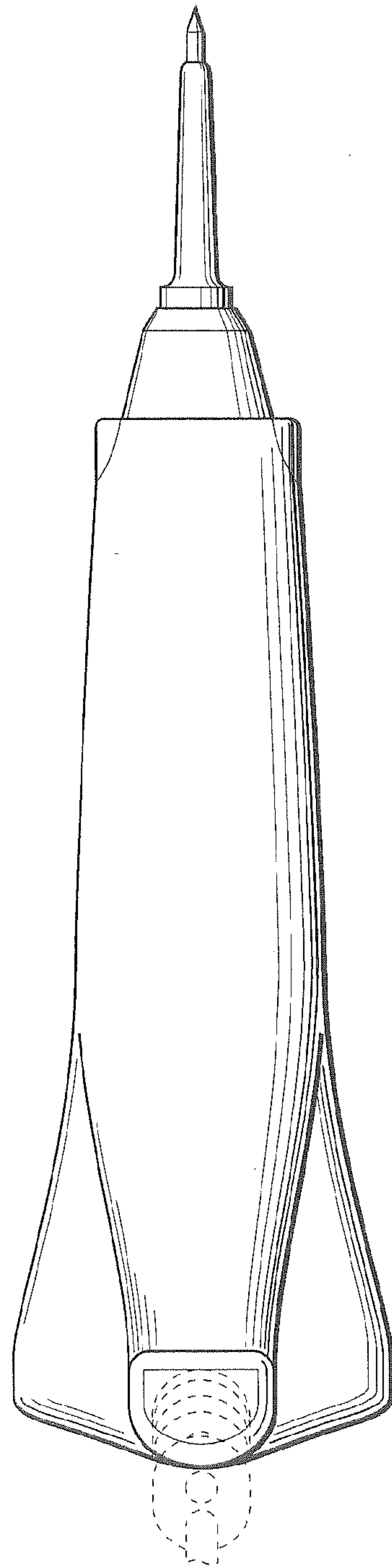


FIG. 6