



US00D752000S

(12) **United States Design Patent**  
**Vinciarelli et al.**

(10) **Patent No.:** **US D752,000 S**  
(45) **Date of Patent:** **\*\* Mar. 22, 2016**

- (54) **SEMICONDUCTOR DEVICE**
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- (73) Assignee: **VLT, Inc.**, Sunnyvale, CA (US)
- (\*\*) Term: **14 Years**
- (21) Appl. No.: **29/509,740**
- (22) Filed: **Nov. 20, 2014**

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**Related U.S. Application Data**

- (60) Division of application No. 29/448,057, filed on Mar. 8, 2013, now Pat. No. Des. 721,047, which is a continuation-in-part of application No. 13/789,065, filed on Mar. 7, 2013, now Pat. No. 8,975,694.
- (51) **LOC (10) Cl.** ..... **13-03**
- (52) **U.S. Cl.**  
USPC ..... **D13/182**
- (58) **Field of Classification Search**  
USPC ..... D13/110, 182; 257/668, 678, 690;  
361/679.01, 713, 728, 736, 760, 761,  
361/775, 820; 324/71.5, 252; 174/250, 253;  
438/64, 65, 66  
CPC ..... H01L 2924/14; H01L 29/01014;  
H01L 2924/00; H01L 25/072; H01L  
2924/301; H01L 2924/30107; H01L 21/00;  
H01L 21/02; G01N 27/414; G01N 27/4148  
See application file for complete search history.

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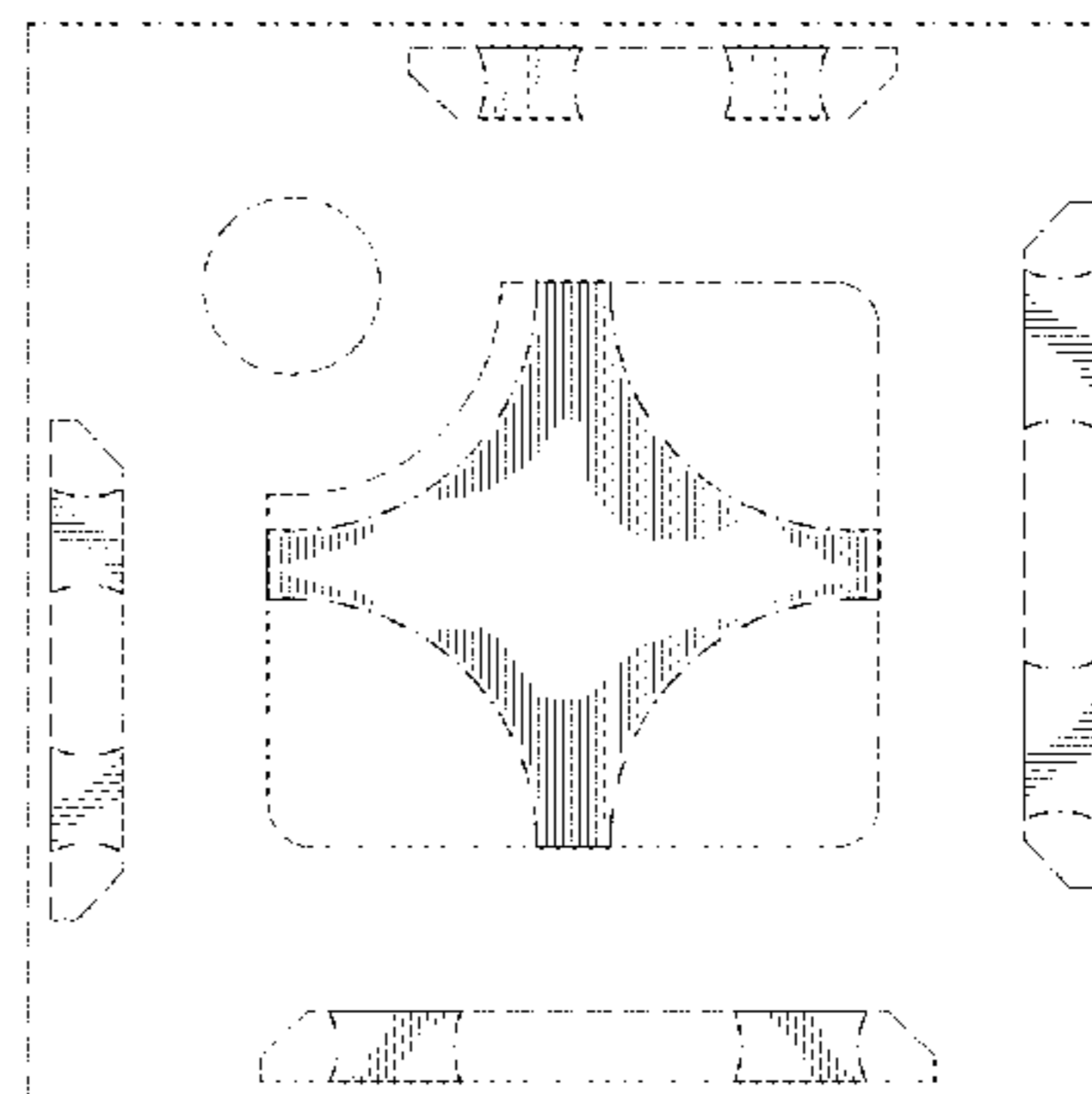
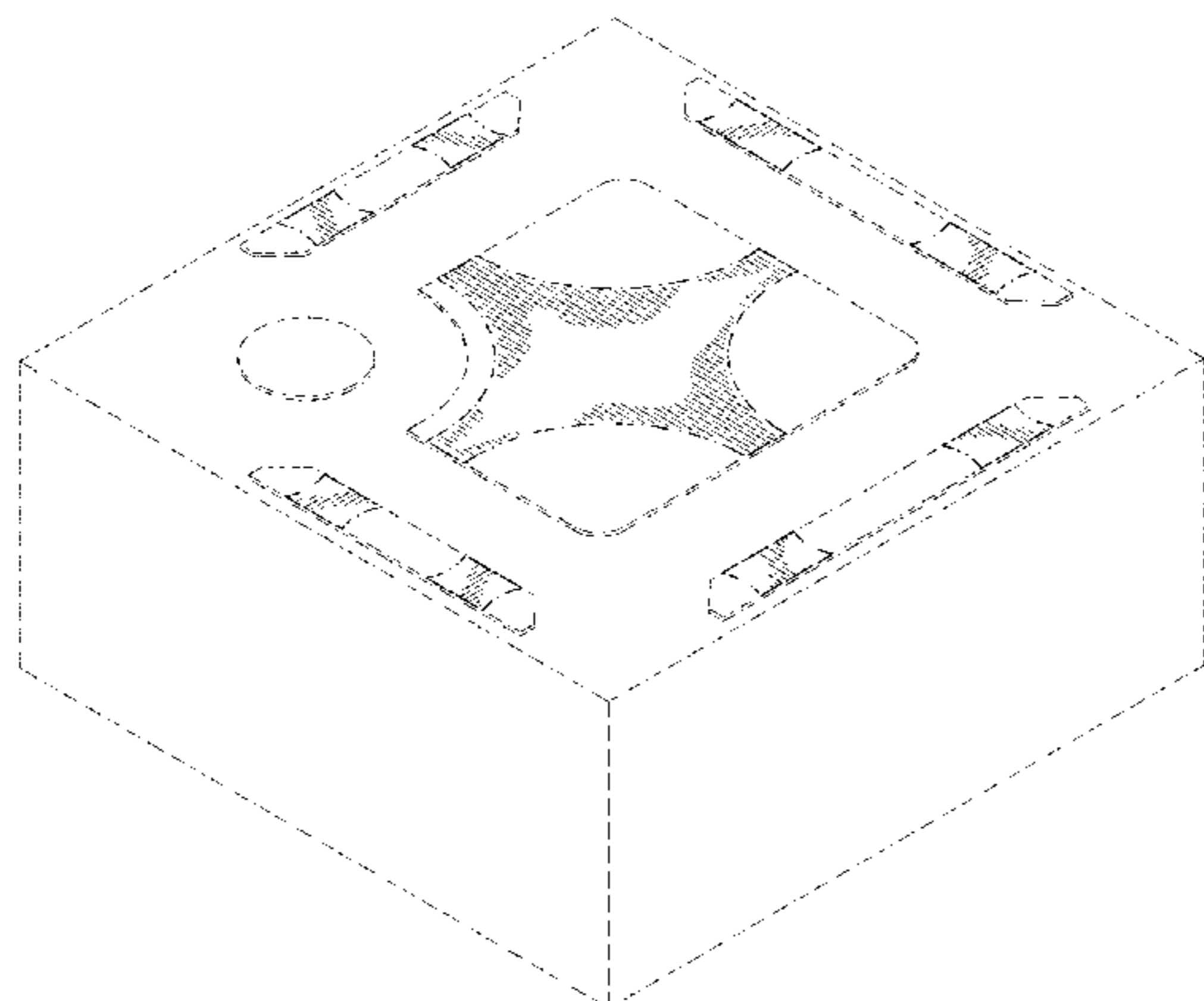
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(57) **CLAIM**  
We claim the ornamental design for a semiconductor device, as shown and described.

**DESCRIPTION**

FIG. 1 is a perspective view of a semiconductor device showing our new design;  
FIG. 2 is a top view thereof;  
FIG. 3 is a bottom view thereof;  
FIG. 4 is a front elevation view thereof;  
FIG. 5 is a rear elevation view thereof;  
FIG. 6 is a right side elevation view thereof; and,  
FIG. 7 is a left side elevation view thereof.  
The broken lines shown in the drawings represent portions of the semiconductor device that form no part of the claimed design.

**1 Claim, 5 Drawing Sheets**



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Fig. 1

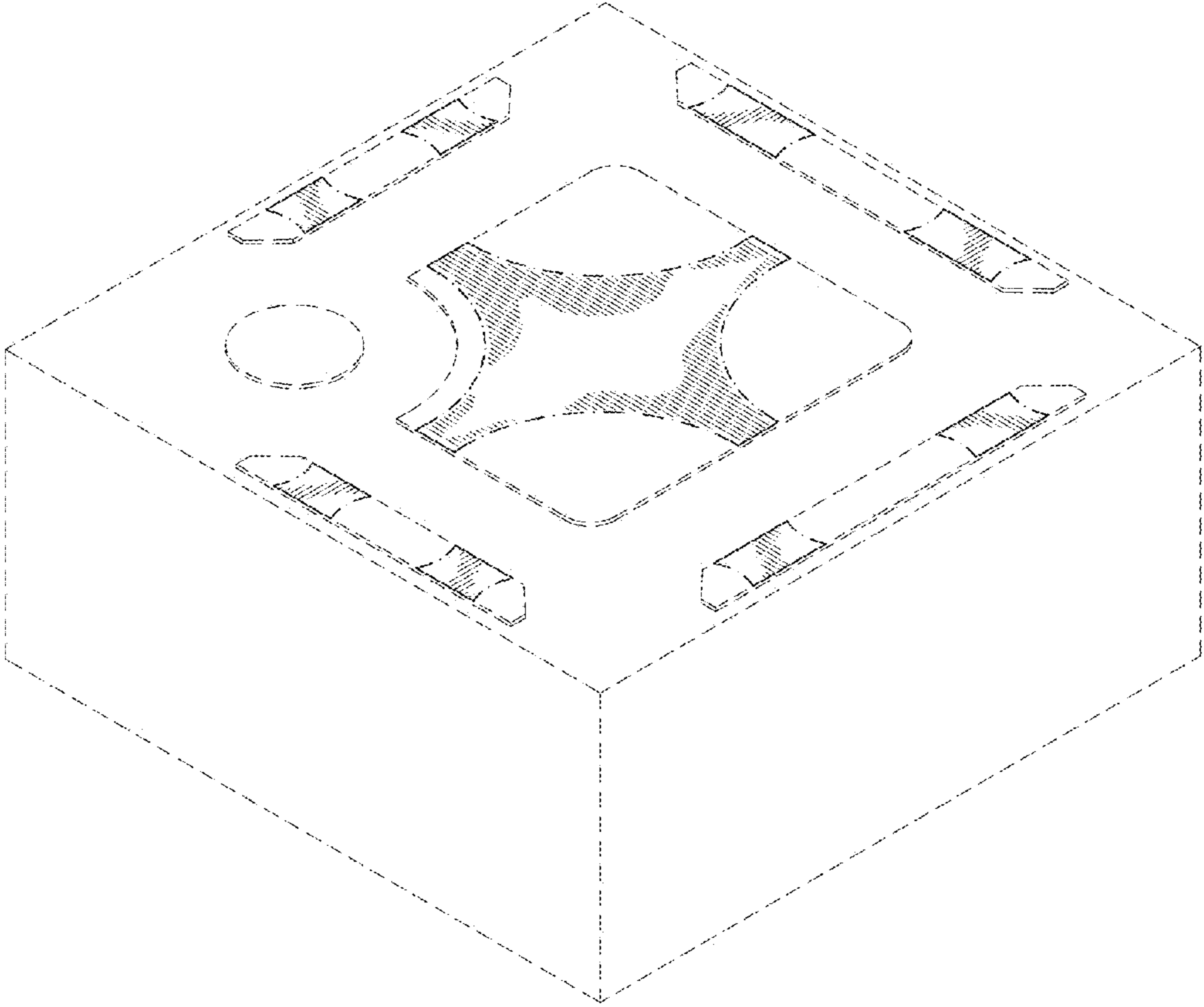
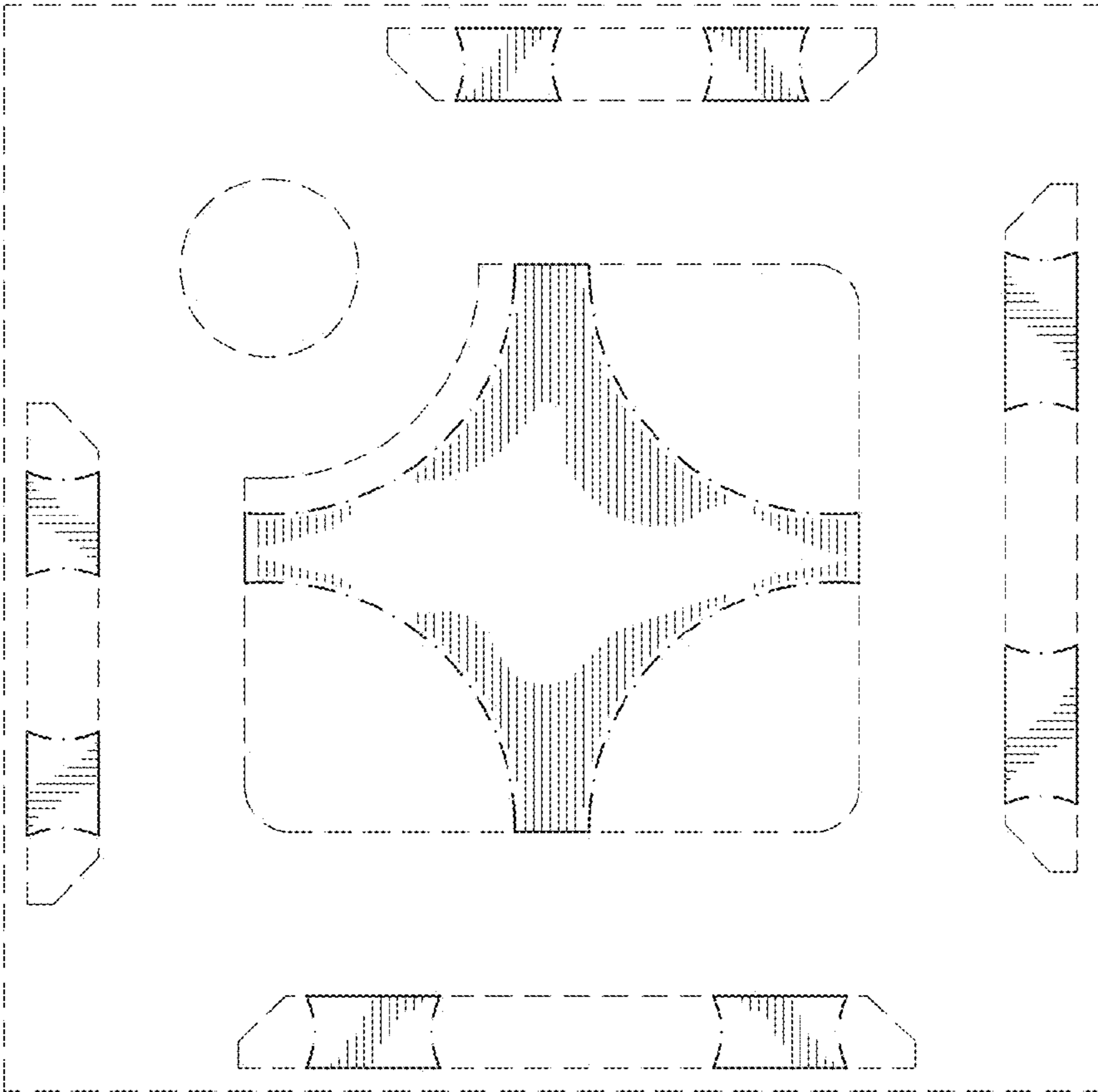


Fig. 2



**Fig. 3**

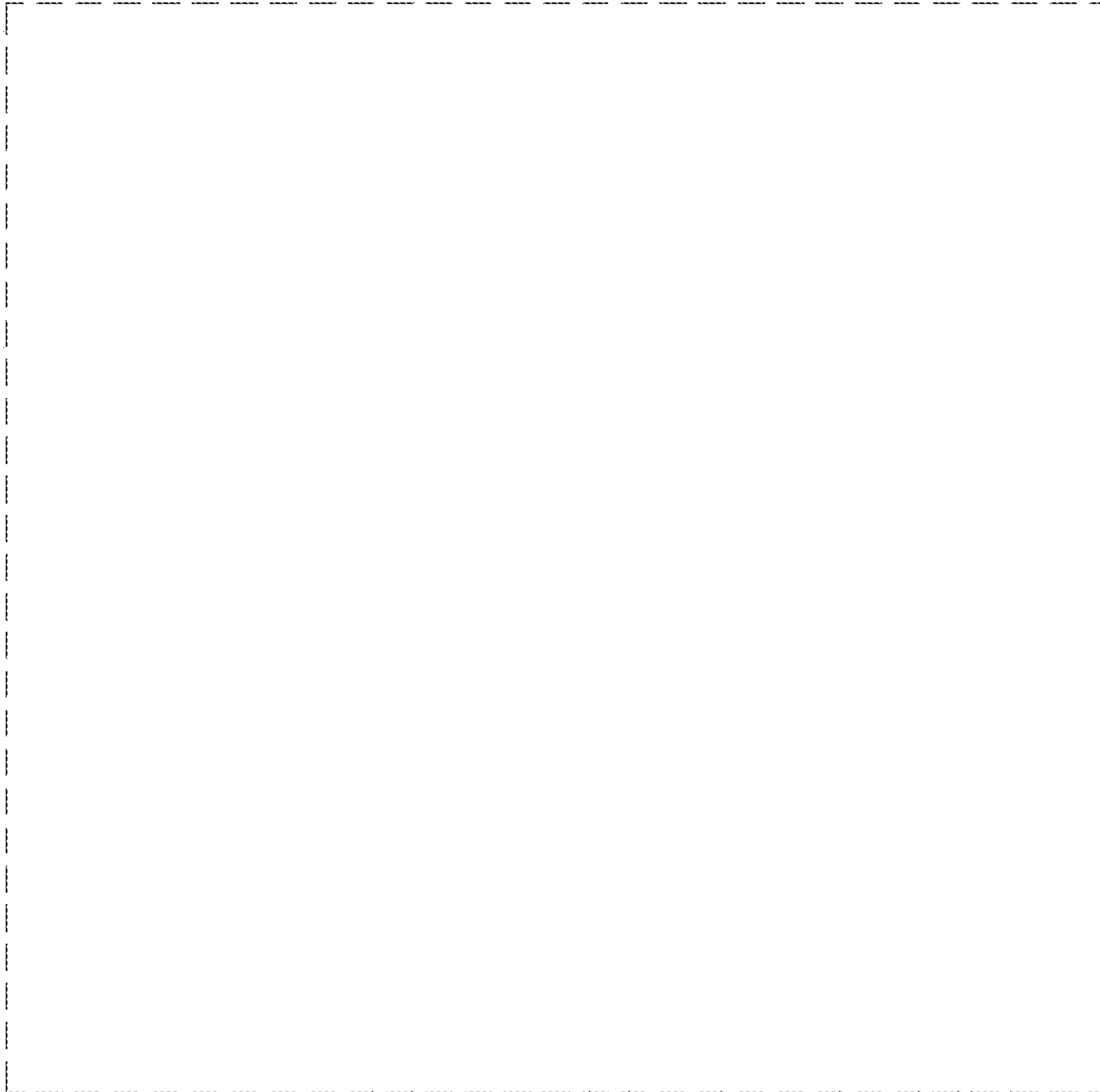


Fig. 4

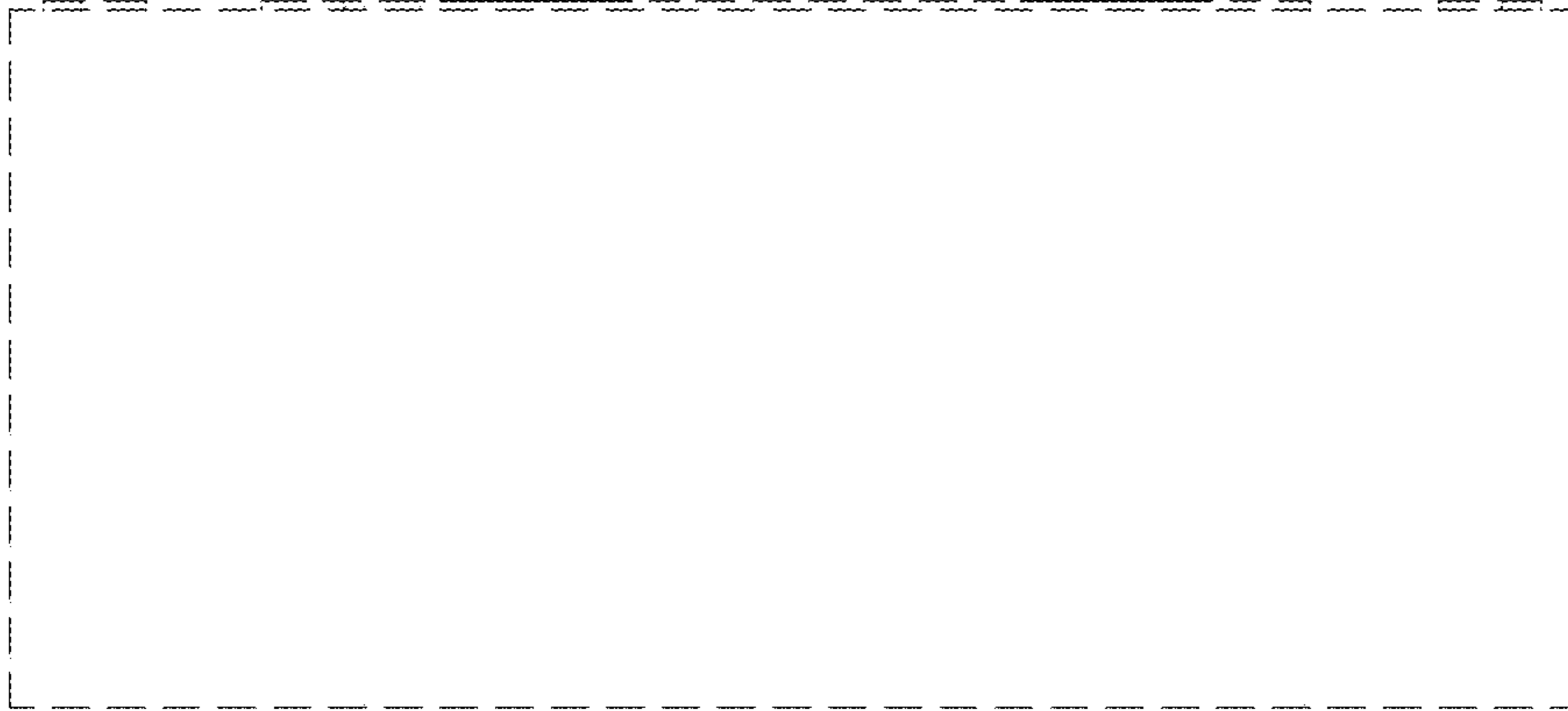


Fig. 5



Fig. 6

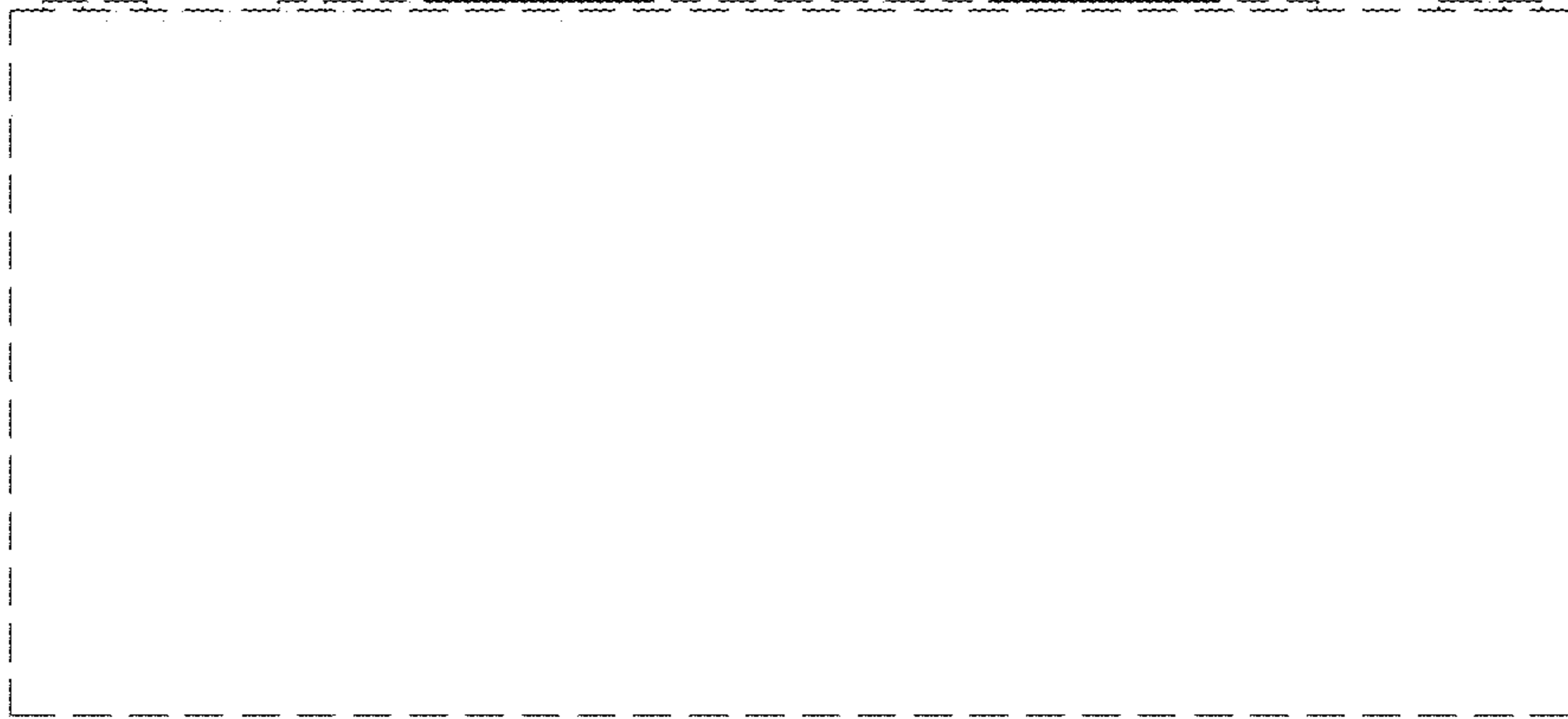


Fig. 7

