



US00D743350S

(12) **United States Design Patent**
Ringer

(10) **Patent No.:** **US D743,350 S**

(45) **Date of Patent:** **** Nov. 17, 2015**

(54) **PERIPHERY DATA PROCESSING DEVICE**

(71) Applicant: **SIEMENS**
AKTIENGESELLSCHAFT, Munich
(DE)

(72) Inventor: **Ulrich Ringer, Amberg (DE)**

(73) Assignee: **Siemens Aktiengesellschaft, Munich**
(DE)

(**) Term: **14 Years**

(21) Appl. No.: **29/501,980**

(22) Filed: **Sep. 10, 2014**

Related U.S. Application Data

(62) Division of application No. 29/424,798, filed on Jun. 15, 2012, now Pat. No. Des. 733,665.

(30) **Foreign Application Priority Data**

Dec. 16, 2011 (EM) 001306500

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/162; D13/162.1**

(58) **Field of Classification Search**
USPC D13/162, 162.1; D14/301, 439
CPC G05B 19/05; G06F 3/147; G06F 11/3636;
H05K 7/1432; H05K 7/1467; H05K 7/1468;
H05K 7/1471; H05K 7/1474; H05K 7/1478;
H05K 7/1481
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D269,605 S * 7/1983 Provanzano et al. D13/162.1
D281,493 S * 11/1985 Prager et al. D13/162.1
D302,972 S * 8/1989 Boucher D13/162.1

D307,263 S * 4/1990 Ishida D13/162.1
4,920,453 A * 4/1990 Onose et al. 361/736
D309,446 S * 7/1990 Russell D13/162.1
D309,600 S * 7/1990 Backes D13/162.1
5,065,141 A * 11/1991 Whitsitt 340/635
5,253,140 A * 10/1993 Inoue et al. 361/728
5,791,916 A * 8/1998 Schirbl et al. 439/76.1
5,802,389 A * 9/1998 McNutt 710/1
5,984,734 A * 11/1999 Piper et al. 439/717
6,008,985 A * 12/1999 Lake et al. 361/679.32
6,172,875 B1 * 1/2001 Suzuki et al. 361/729
6,456,495 B1 * 9/2002 Wieloch et al. 361/729
6,686,672 B2 * 2/2004 Brown et al. 307/125
D488,133 S * 4/2004 Droulin et al. D13/162.1
6,904,471 B2 * 6/2005 Boggs et al. 710/8

(Continued)

Primary Examiner — Selina Sikder

(74) *Attorney, Agent, or Firm* — Cozen O'Connor

(57) **CLAIM**

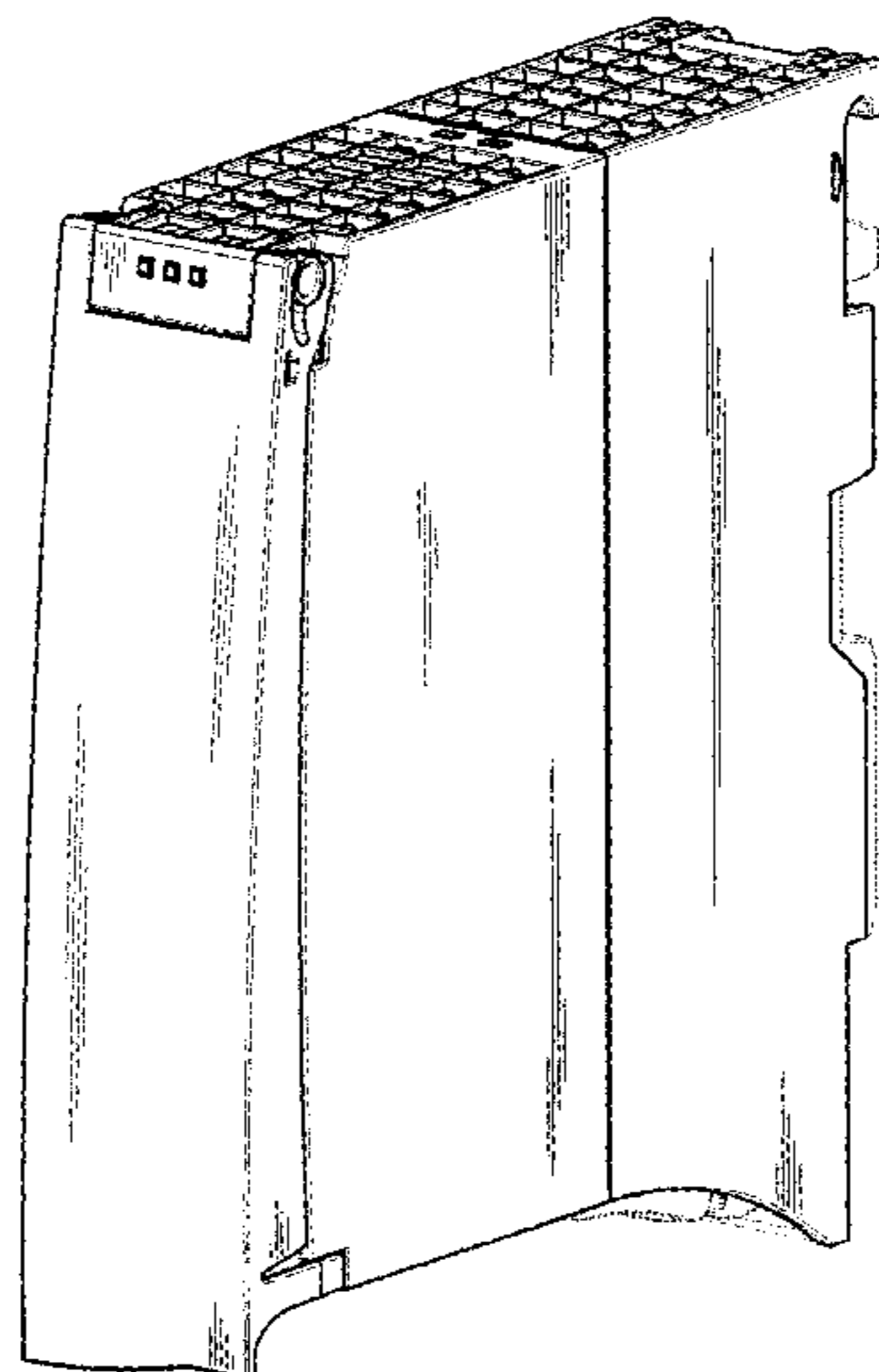
The ornamental design for a periphery data processing device, as shown and described.

DESCRIPTION

FIG. 1 is a front elevational view of a periphery data processing device for a programmable logic controller (PLC) showing my new design;
FIG. 2 is a rear elevational view of the periphery data processing device;
FIG. 3 is a top plan view of the periphery data processing device;
FIG. 4 is a bottom plan view of the periphery data processing device;
FIG. 5 is a right-side elevation view of the periphery data processing device;
FIG. 6 is left-side elevation view of the periphery data processing device; and,
FIG. 7 is a perspective view of the periphery data processing device.

The broken lines shown in the drawing views are for illustrative purposes only and forms no part of the claimed design.

1 Claim, 7 Drawing Sheets



(56)

References Cited

U.S. PATENT DOCUMENTS

7,027,296	B2 *	4/2006	Bock	361/622
D520,992	S *	5/2006	Lee	D14/301
7,066,677	B2 *	6/2006	Ruter	403/231
D524,760	S *	7/2006	Ohlwine et al.	D13/162.1
D527,349	S *	8/2006	Lee	D13/162.1
D563,903	S *	3/2008	Radau et al.	D13/162
D588,552	S *	3/2009	Radau et al.	D13/162
D598,867	S *	8/2009	Nada et al.	D13/162.1
D692,397	S *	10/2013	Liu et al.	D13/162.1
8,602,816	B2 *	12/2013	Donhauser et al.	439/532
D702,647	S *	4/2014	Liu et al.	D13/162.1
D733,665	S *	7/2015	Ringer	D13/162.1
2002/0072256	A1 *	6/2002	Lostoski et al.	439/76.1
2012/0043378	A1 *	2/2012	Vazach et al.	235/375
2012/0129368	A1 *	5/2012	Donhauser et al.	439/137
2014/0118958	A1 *	5/2014	Hamada et al.	361/728
2014/0156029	A1 *	6/2014	Godau et al.	700/19

* cited by examiner

FIG 1

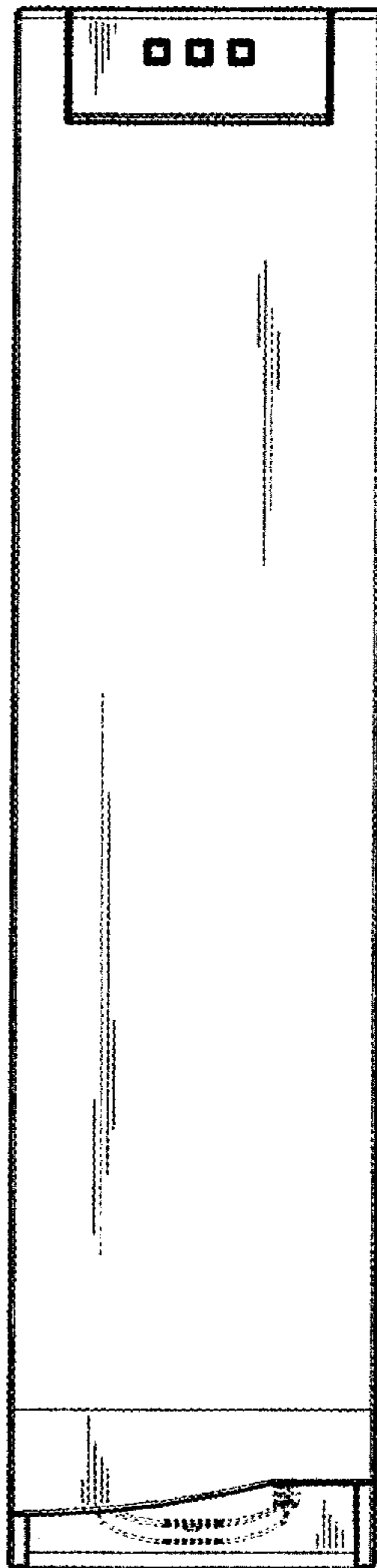


FIG 2

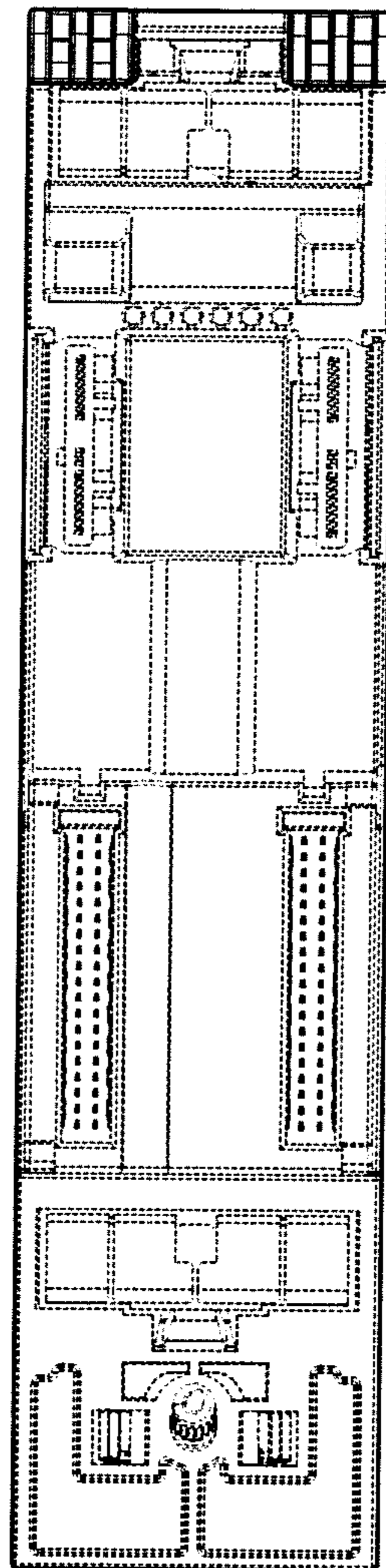


FIG 3

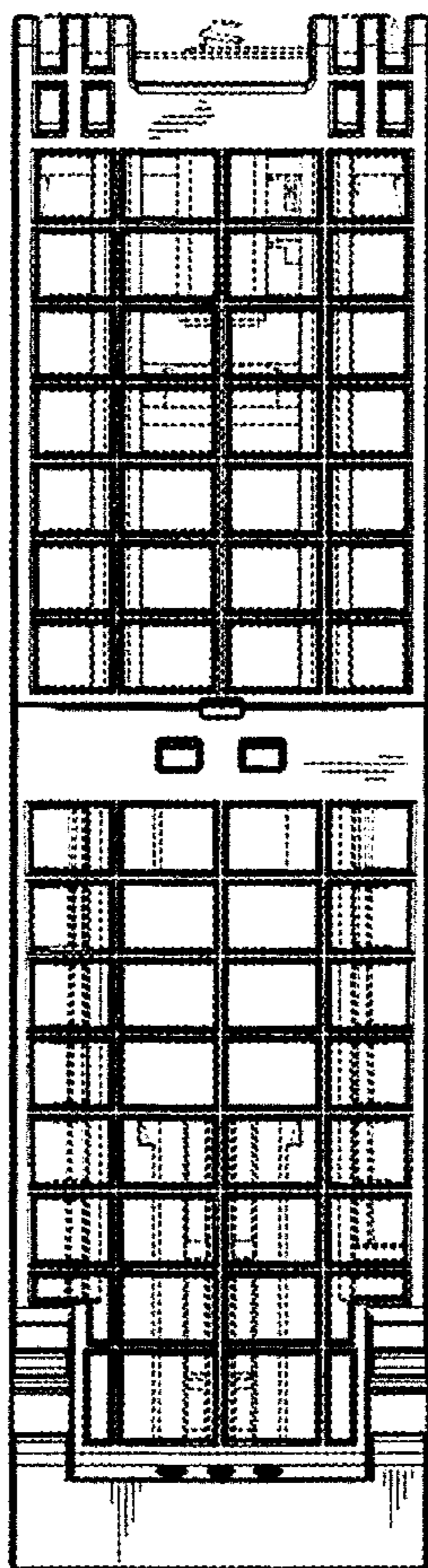


FIG 4

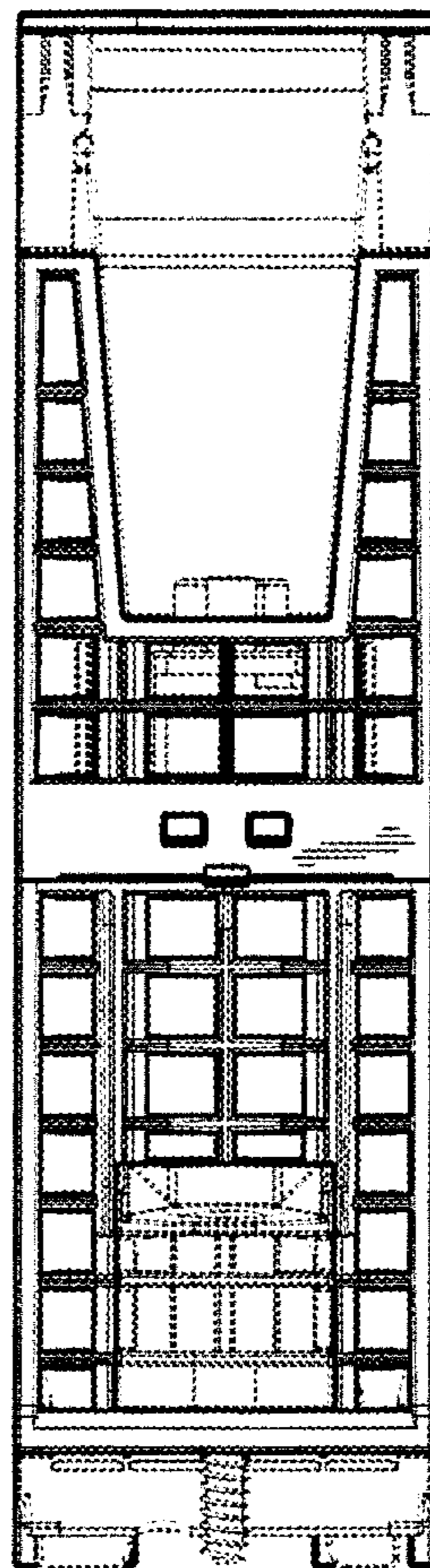


FIG 5

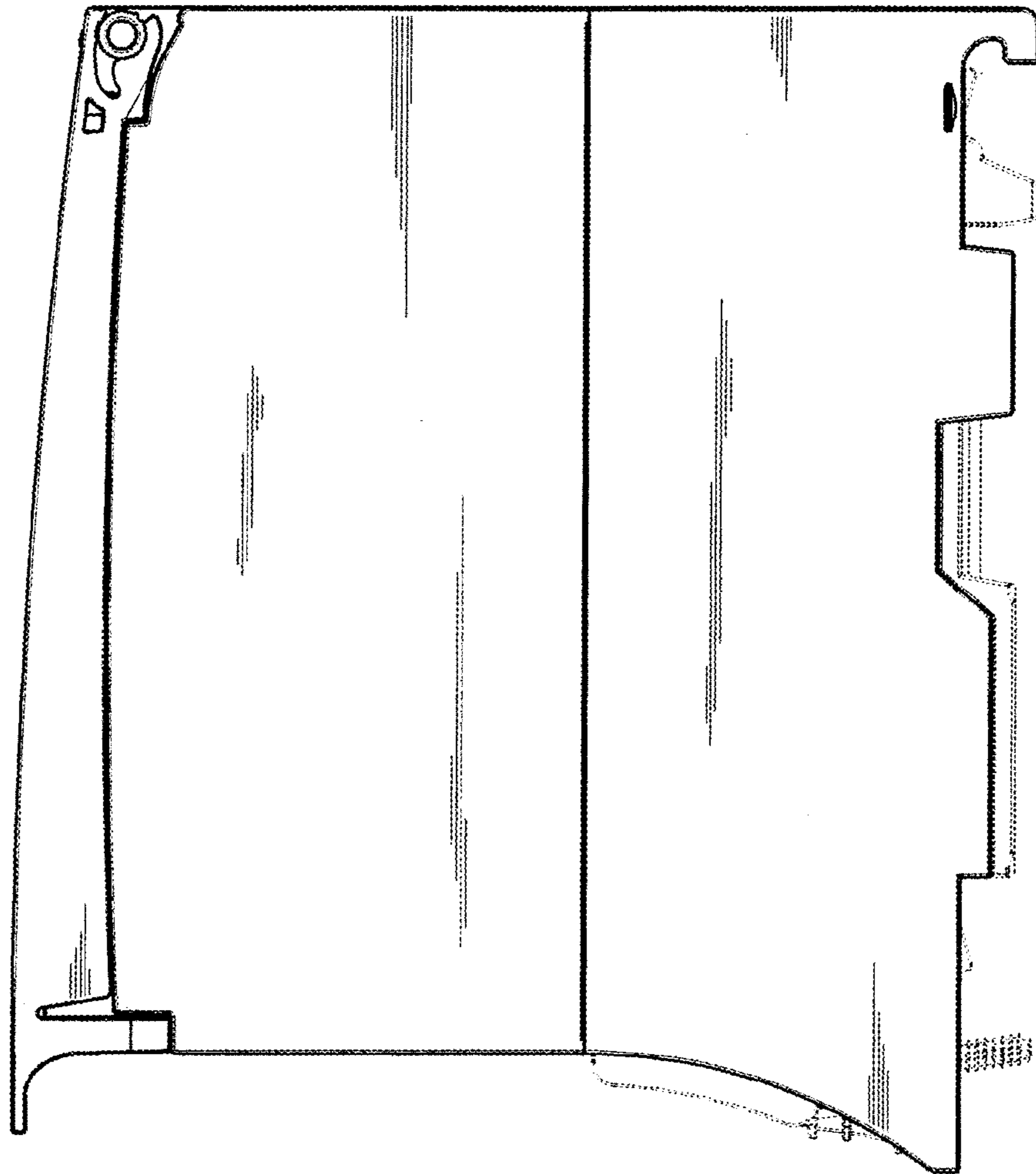


FIG 6

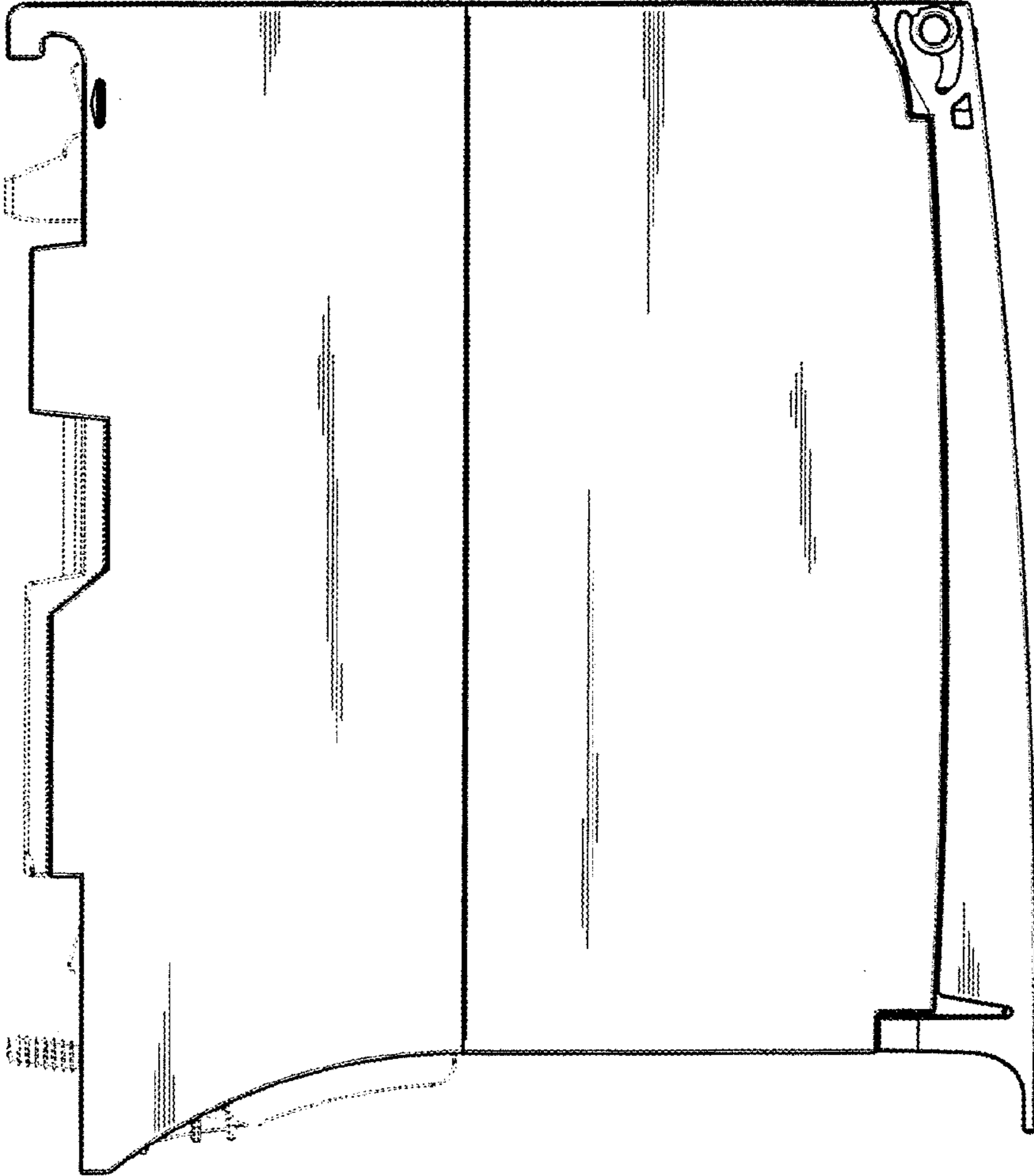


FIG 7

