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(12) **United States Design Patent**  
**Masuda**

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(54) **SEMICONDUCTOR DEVICE**

(71) Applicant: **Sumitomo Electric Industries, Ltd.**,  
Osaka (JP)

(72) Inventor: **Takeyoshi Masuda**, Osaka (JP)

(73) Assignee: **Sumitomo Electric Industries, Ltd.**,  
Osaka-shi (JP)

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**Related U.S. Application Data**

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(52) **U.S. Cl.**  
USPC ..... **D13/182**

(58) **Field of Classification Search**  
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CPC . H05K 1/0228; H05K 1/0245; H05K 1/0236;  
H05K 1/0263; H01L 21/02433; H01L 29/04  
See application file for complete search history.

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*Primary Examiner* — Selina Sikder

(74) *Attorney, Agent, or Firm* — Venable LLP; Michael A. Sartori; Tamatane J. Aga

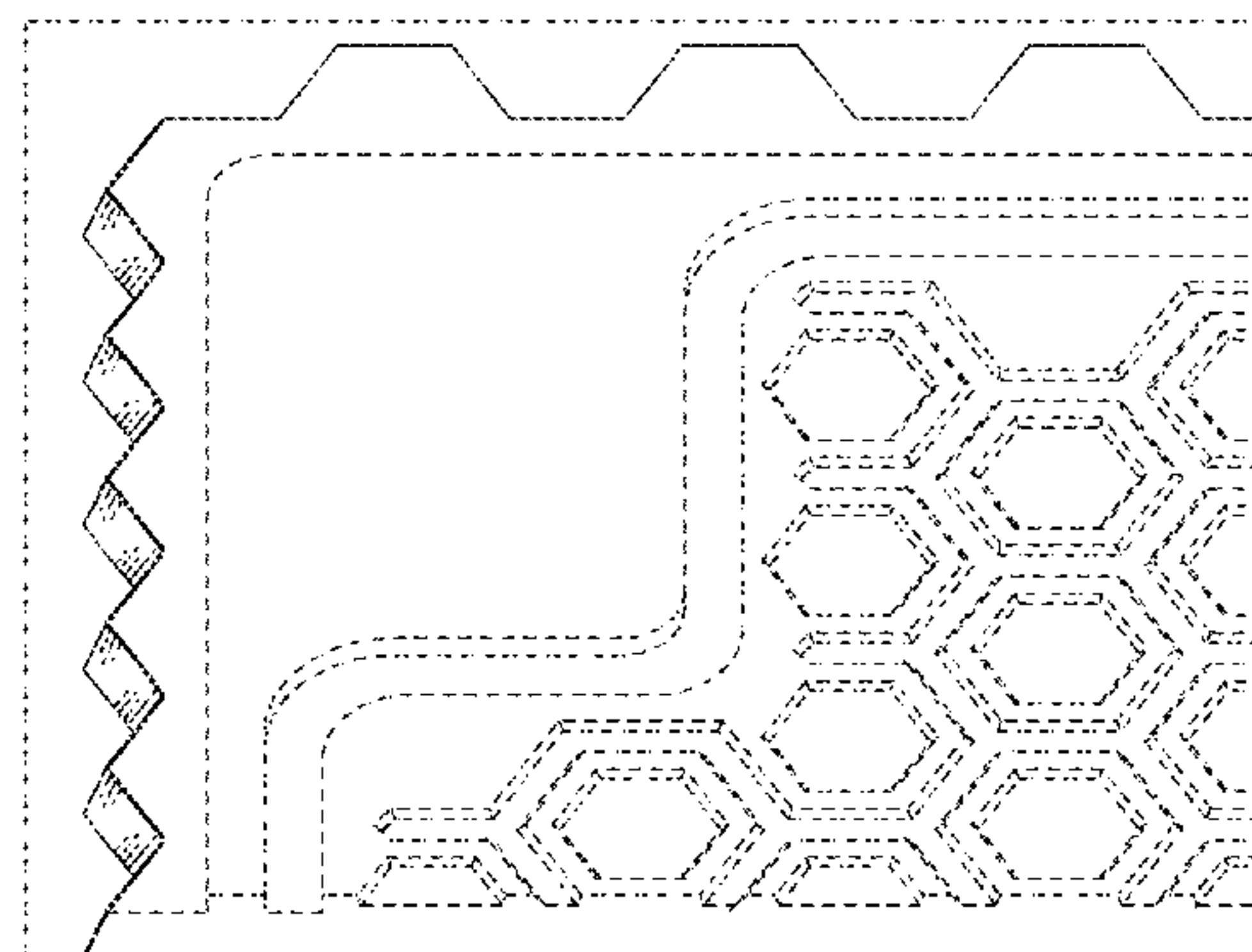
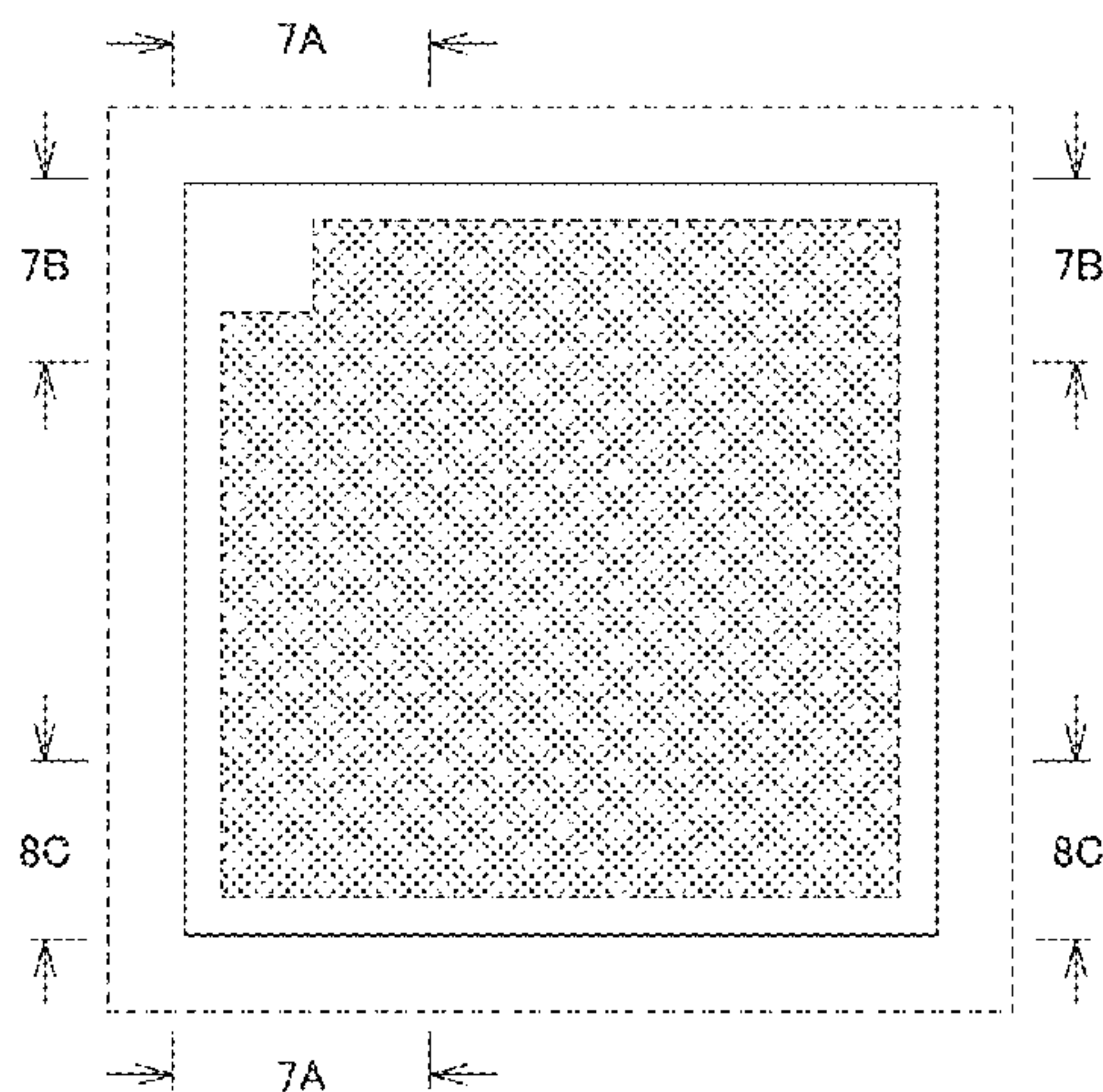
(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

**DESCRIPTION**

FIG. 1 is a front view of a semiconductor device showing my new design;  
FIG. 2 is a rear view thereof;  
FIG. 3 is a top plan view thereof;  
FIG. 4 is a bottom plan view thereof;  
FIG. 5 is a right side view thereof;  
FIG. 6 is a left side view thereof;  
FIG. 7 is an enlarged perspective view showing the area defined by indicia 7A and 7B of FIG. 1 thereof; and,  
FIG. 8 is an enlarged perspective view showing the area defined by indicia 7A and 8C of FIG. 1 thereof.  
The broken line showing is for illustrative purpose only and forms no part of the claimed design.

**1 Claim, 4 Drawing Sheets**



(56)

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FIG.1

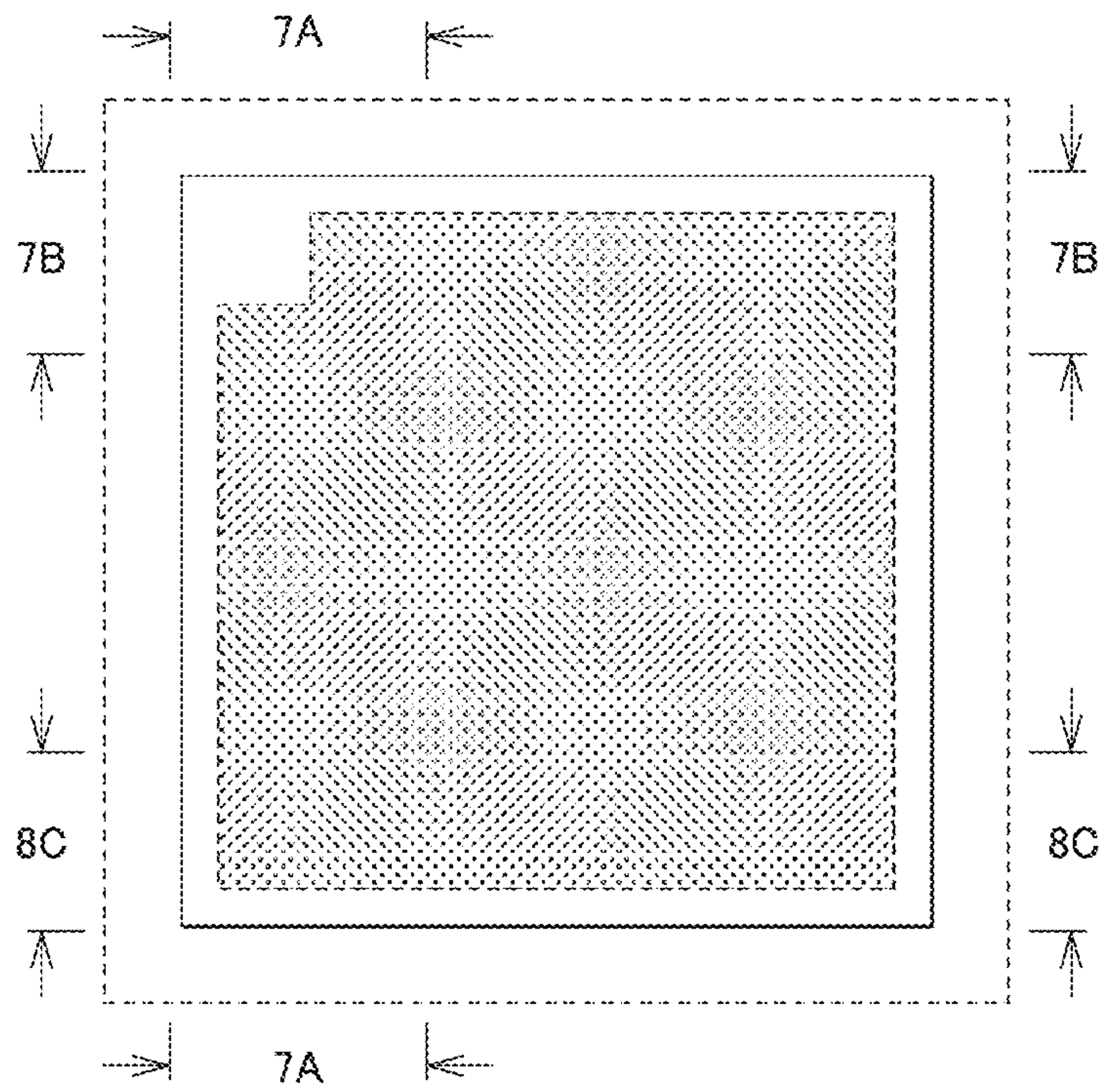


FIG.2

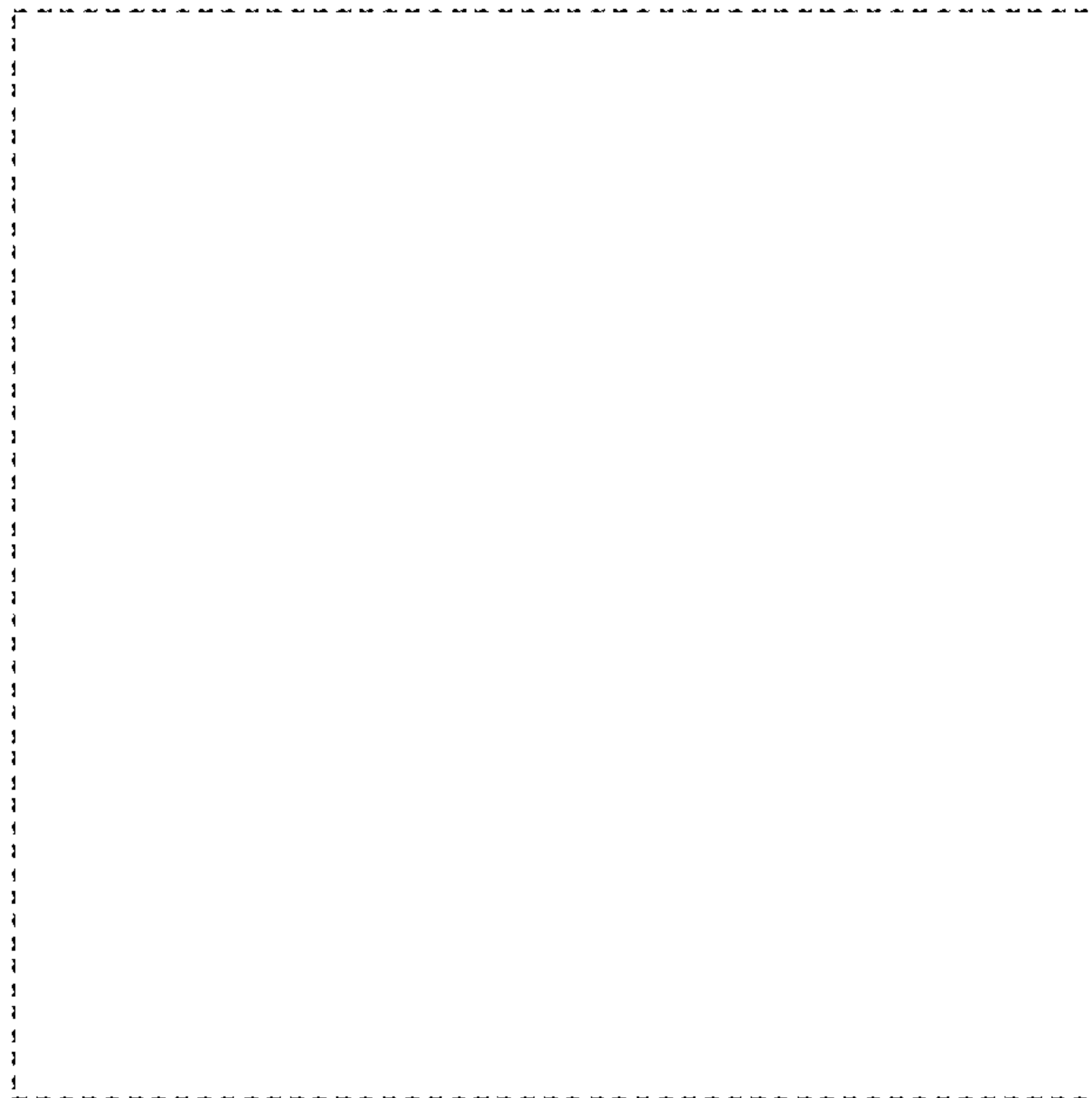


FIG.3



FIG.4



FIG.5

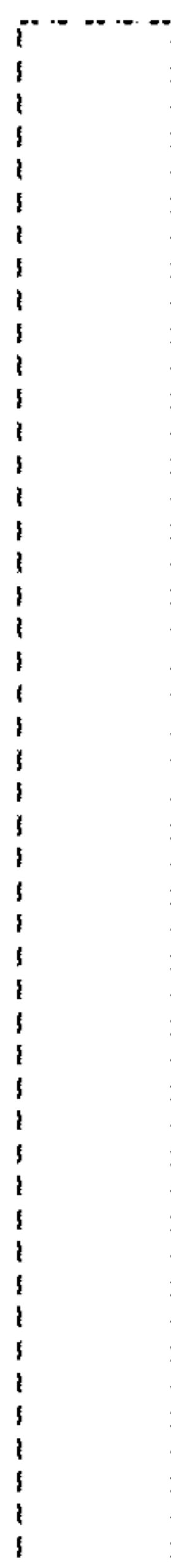


FIG.6



FIG.7

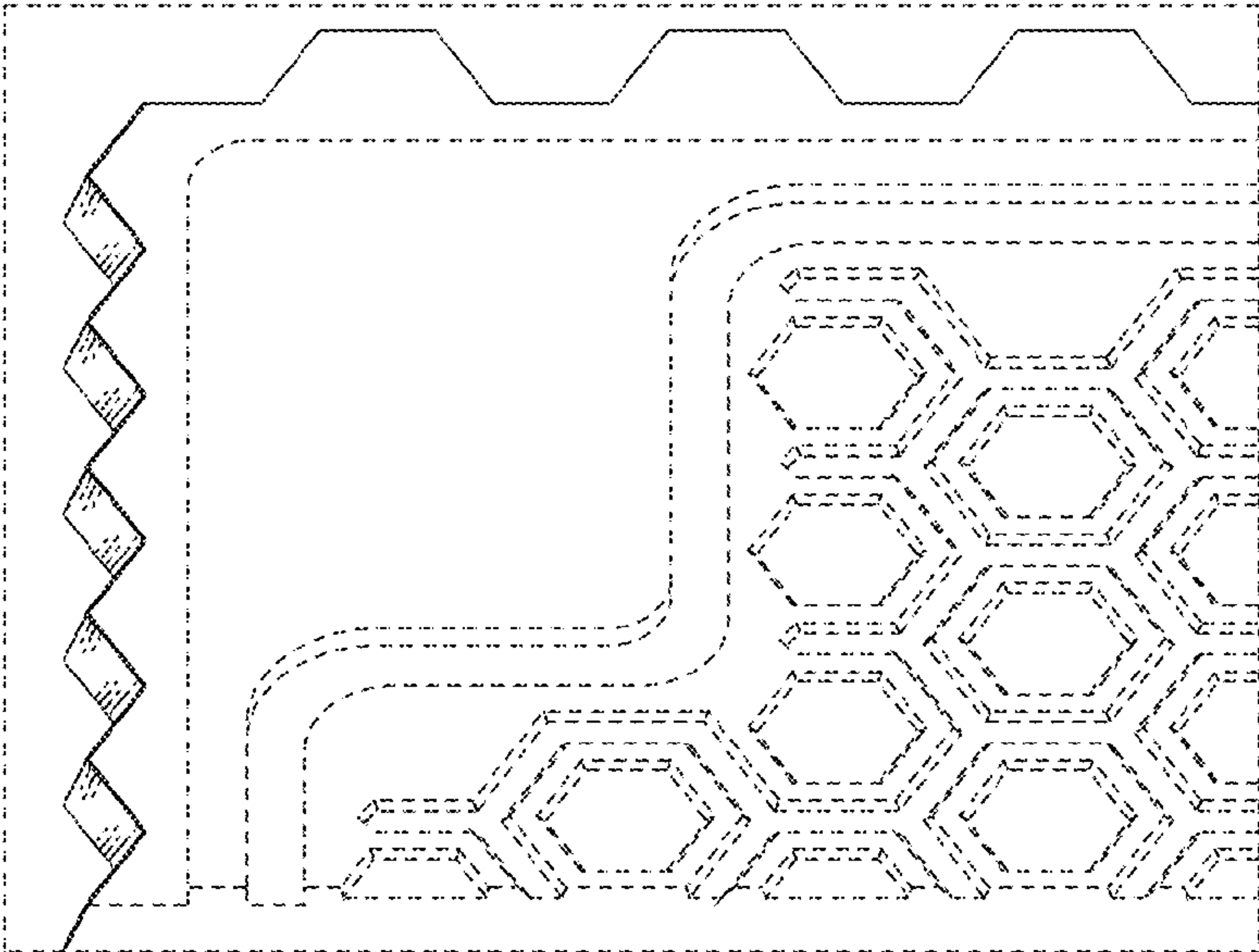




FIG. 8

