



US00D737229S

(12) **United States Design Patent**
Masuda

(10) **Patent No.:** **US D737,229 S**
(45) **Date of Patent:** **** Aug. 25, 2015**

(54) **SEMICONDUCTOR DEVICE**

(71) Applicant: **Sumitomo Electric Industries, Ltd.**,
Osaka (JP)

(72) Inventor: **Takeyoshi Masuda**, Osaka (JP)

(73) Assignee: **Sumitomo Electric Industries, Ltd.**,
Osaka-shi (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/481,535**

(22) Filed: **Feb. 6, 2014**

Related U.S. Application Data

(62) Division of application No. 29/389,545, filed on Apr. 13, 2011, now Pat. No. Des. 701,843.

(30) **Foreign Application Priority Data**

Dec. 28, 2010 (JP) D.2010-031446
Dec. 28, 2010 (JP) D.2010-031447
Dec. 28, 2010 (JP) D.2010-031448

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182
CPC . H05K 1/0228; H05K 1/0245; H05K 1/0236;
H05K 1/0263; H01L 21/02433; H01L 29/04
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,447,876 A * 9/1995 Moyer et al. 438/105
5,852,315 A * 12/1998 Ker et al. 257/355
6,184,478 B1 * 2/2001 Imano et al. 174/261
6,388,292 B1 * 5/2002 Lin 257/356

6,713,823 B1 * 3/2004 Nickel 257/401
6,897,561 B2 * 5/2005 Nemtsev et al. 257/758
6,903,460 B2 * 6/2005 Fukuda et al. 257/758
7,166,898 B2 * 1/2007 Briere 257/401
D574,339 S 8/2008 Honjo et al.
7,663,063 B2 * 2/2010 Lin et al. 174/255
7,981,709 B2 7/2011 Masuda
8,203,151 B2 6/2012 Masuda
8,487,377 B2 * 7/2013 Yu et al. 257/342
D692,843 S * 11/2013 Masuda D13/182
D701,843 S * 4/2014 Masuda D13/182
8,791,508 B2 * 7/2014 Roberts et al. 257/206
8,941,012 B2 * 1/2015 Pai 174/254
2003/0136984 A1 * 7/2003 Masuda et al. 257/247
2005/0274977 A1 * 12/2005 Saito et al. 257/192
2006/0267030 A1 11/2006 Yamazaki et al.
2010/0000765 A1 1/2010 Hirakata et al.

(Continued)

Primary Examiner — Selina Sikder

(74) *Attorney, Agent, or Firm* — Venable LLP; Michael A. Sartori; Tamatane J. Aga

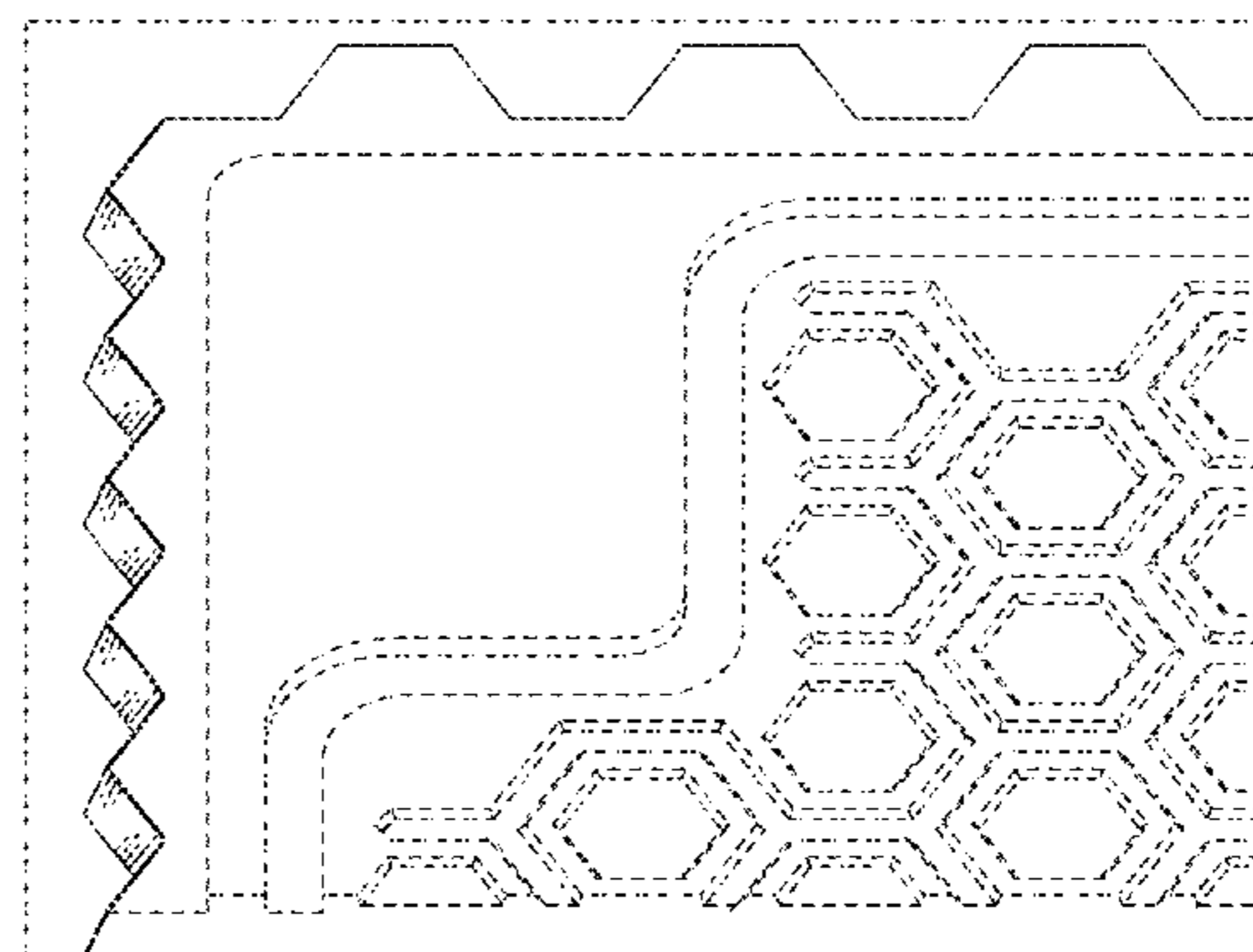
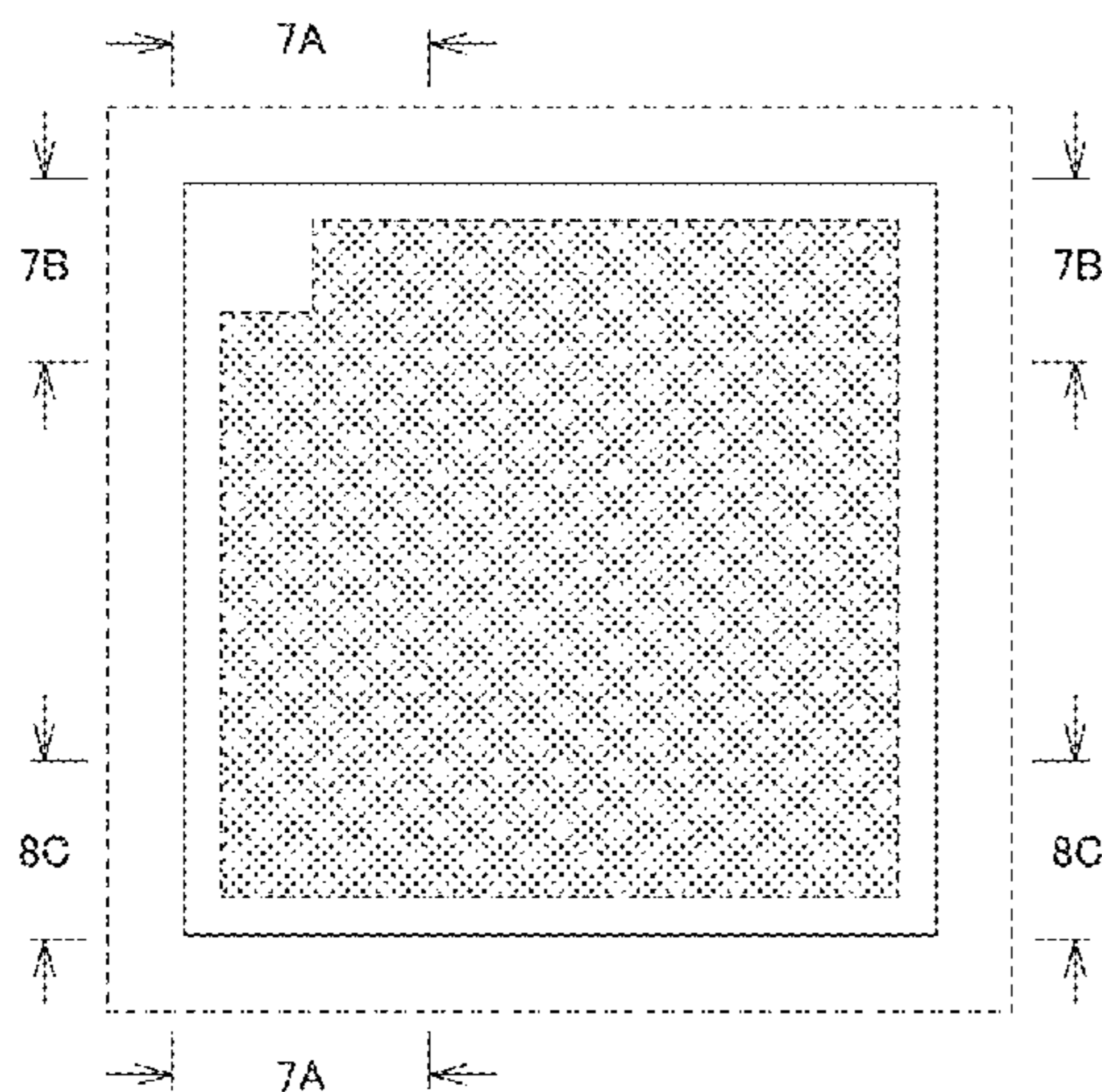
(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. 1 is a front view of a semiconductor device showing my new design;
FIG. 2 is a rear view thereof;
FIG. 3 is a top plan view thereof;
FIG. 4 is a bottom plan view thereof;
FIG. 5 is a right side view thereof;
FIG. 6 is a left side view thereof;
FIG. 7 is an enlarged perspective view showing the area defined by indicia 7A and 7B of FIG. 1 thereof; and,
FIG. 8 is an enlarged perspective view showing the area defined by indicia 7A and 8C of FIG. 1 thereof.
The broken line showing is for illustrative purpose only and forms no part of the claimed design.

1 Claim, 4 Drawing Sheets



(56)

References Cited

U.S. PATENT DOCUMENTS

2010/0132981 A1 6/2010 Muro et al.
2010/0163282 A1 7/2010 Tagi et al.
2010/0175912 A1 7/2010 Shih
2010/0200276 A1 8/2010 Karikalan

2011/0186858 A1* 8/2011 Roberts et al. 257/76
2011/0203834 A1* 8/2011 Yoneya et al. 174/250
2012/0118614 A1 5/2012 Kuriki
2012/0186855 A1 7/2012 Lin
2012/0205141 A1 8/2012 Ogawa et al.

* cited by examiner

FIG.1

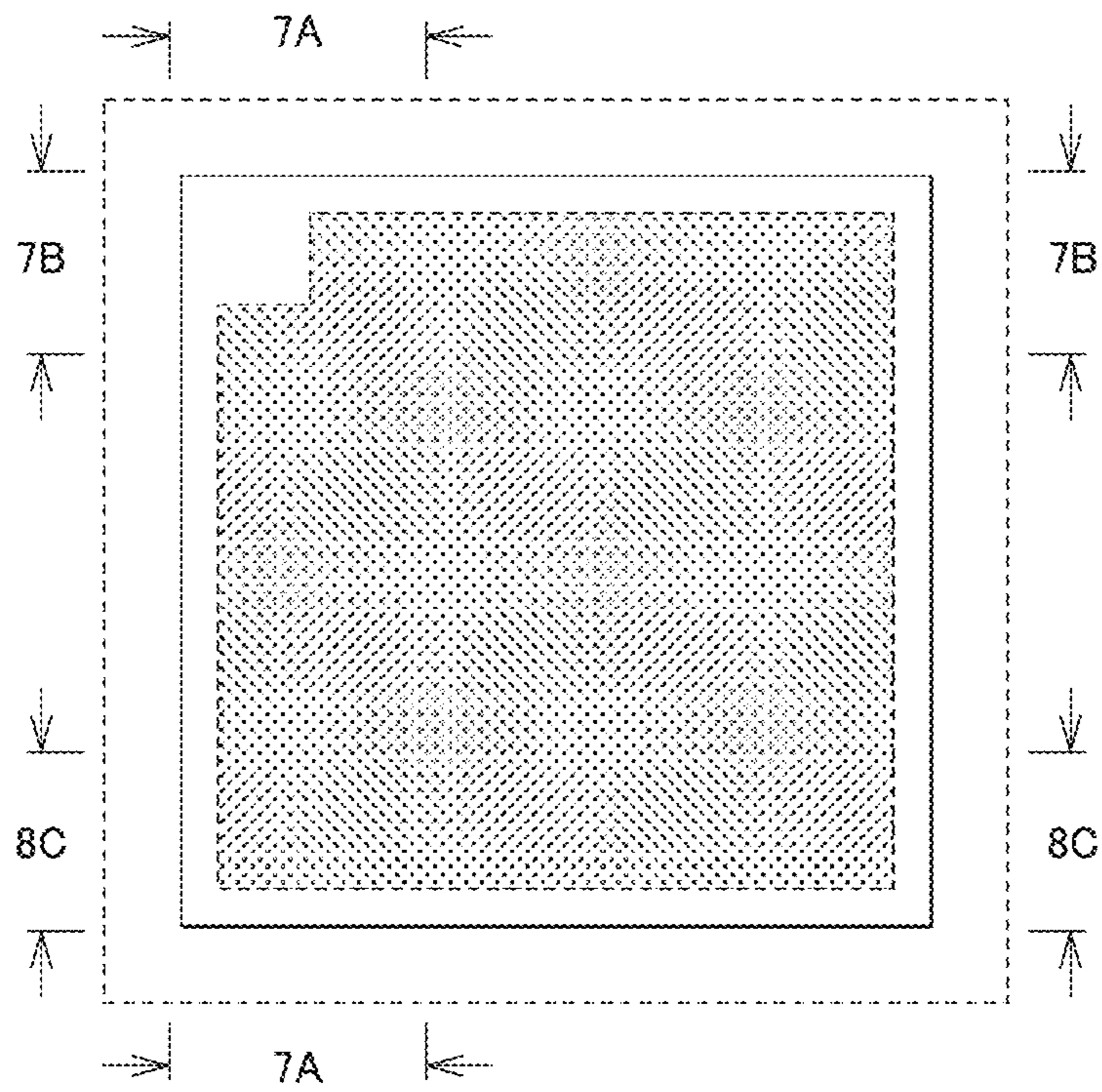


FIG.2

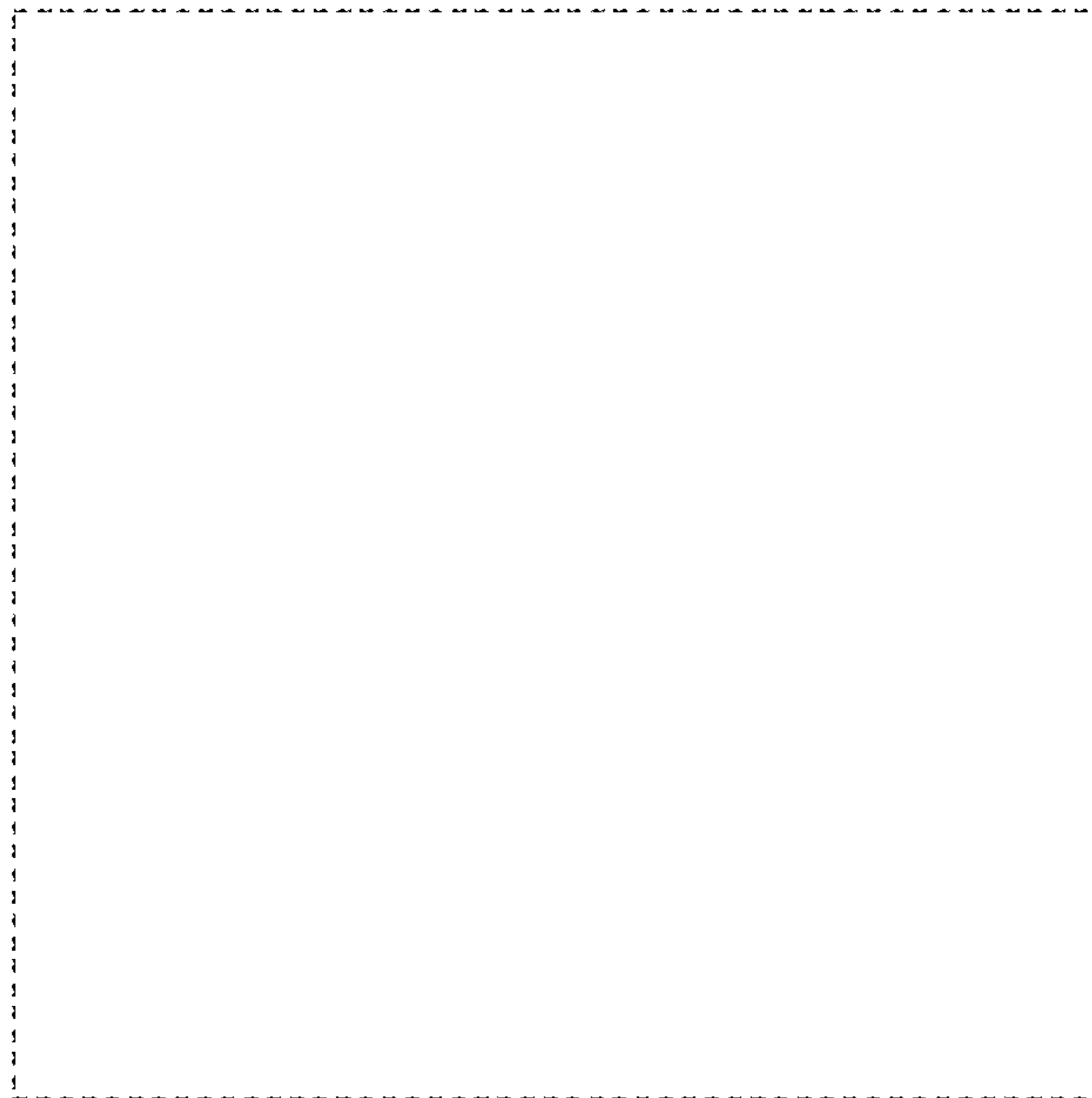


FIG.3



FIG.4



FIG.5

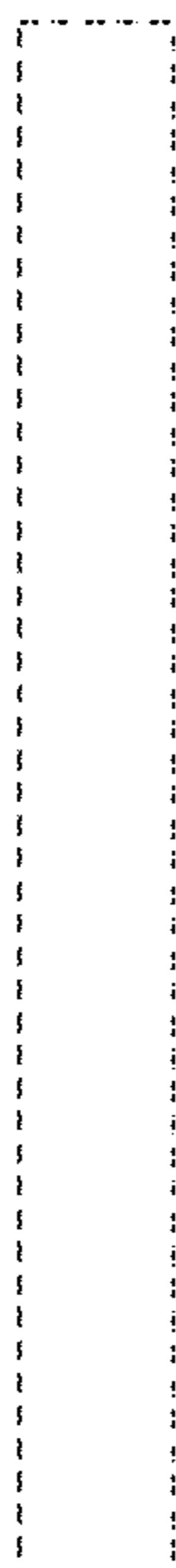


FIG.6

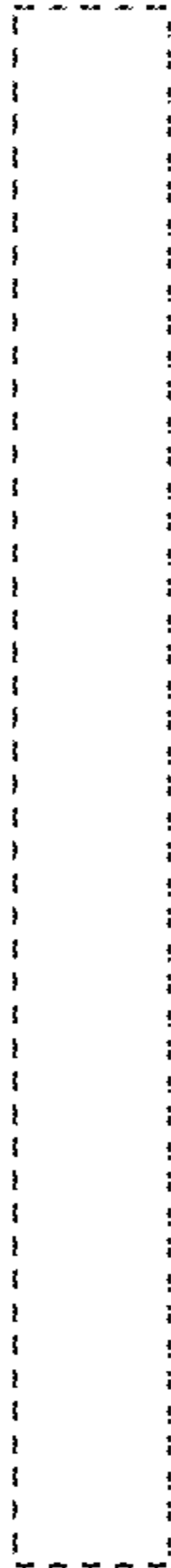


FIG.7

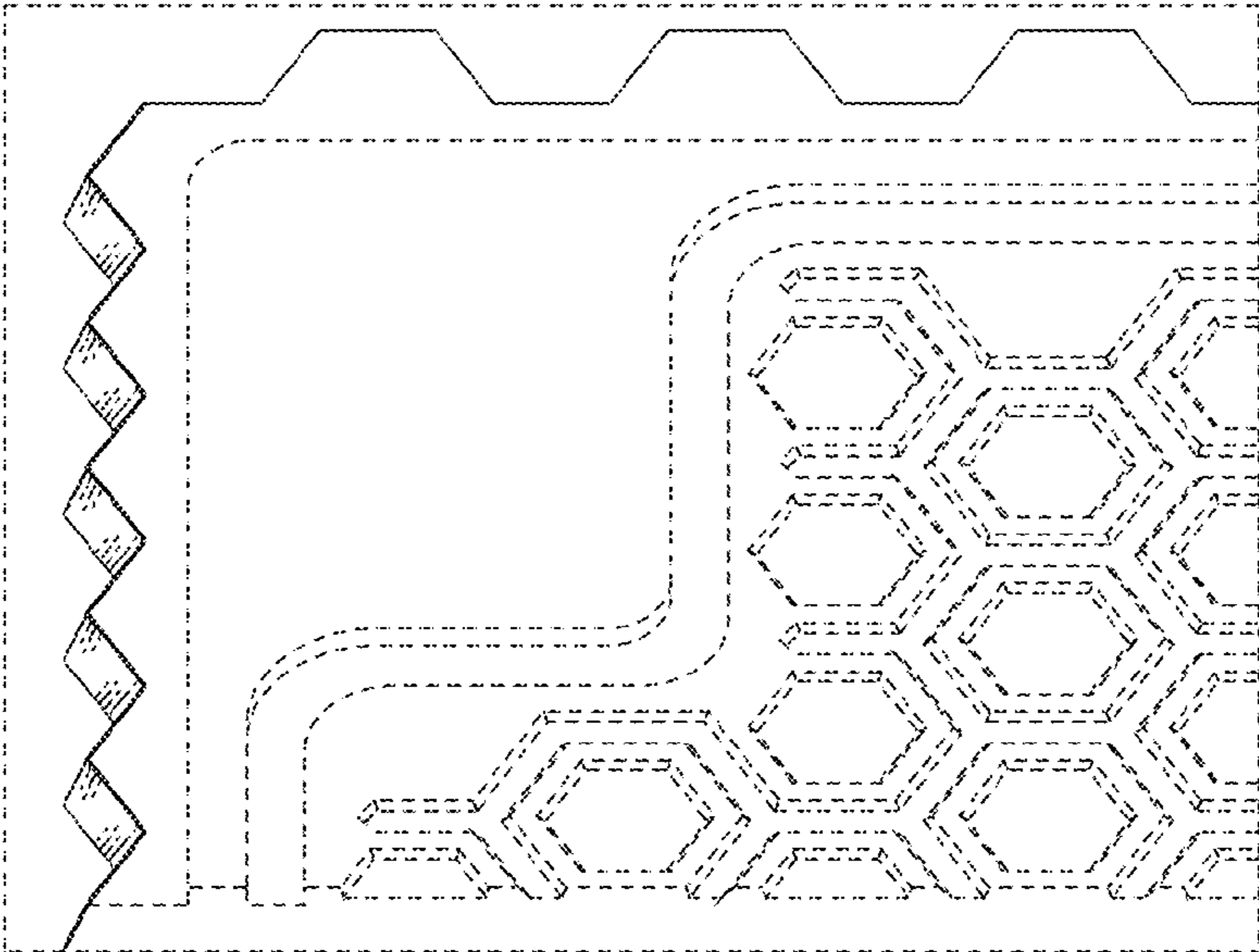


FIG. 8

