US00D730304S

(12) United States Design Patent

Matsumoto et al.

(10) Patent No.: US D730,304 S
(45) Date of Patent: ** May 26, 2015

(54) **SUBSTRATE FOR AN ELECTRONIC CIRCUIT**

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(73) Assignee: **Kabushiki Kaisha Toshiba**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/500,867**

(22) Filed: **Aug. 29, 2014**

(30) **Foreign Application Priority Data**

May 15, 2014 (JP) 2014-010413

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182, 123, 133, 110, 184, 199; 257/177, 666, 684, 686, 689, 775; 361/600, 601, 820; 29/825, 829, 830, 29/831, 832; 174/68.1, 250, 253, 254, 174/260, 261, 268; 216/13; 428/901; D5/4, D5/61
See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a substrate for an electronic circuit, as shown and described.

DESCRIPTION

The patent or application file contains at least one drawing executed in color. Copies of this patent or patent application with color drawings(s) will be provided by the Office upon request and payment of the necessary fee.

FIG. **1** is a perspective view of a substrate for an electronic circuit showing our new design;

FIG. **2** is a rear perspective view thereof;

FIG. **3** is a front elevational view thereof;

FIG. **4** is a rear elevational view thereof;

FIG. **5** is a right side elevational view, a left side elevational view being a mirror image thereof;

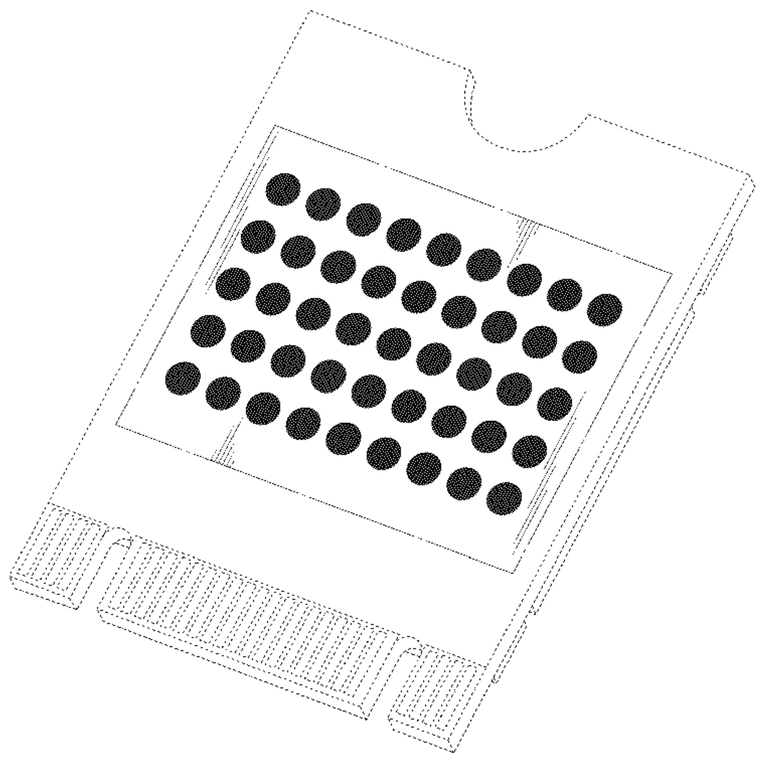
FIG. **6** is a top plan view thereof; and,

FIG. **7** is a bottom plan view thereof.

The black circles shown in FIGS. **2** and **4** are flat on the surface of the electronic circuit.

The even dashed broken lines shown in the drawings represent portions of the substrate for an electronic circuit that form no part of the claimed design. The dashed-dot-dashed broken lines define the boundaries of the claimed design.

1 Claim, 5 Drawing Sheets
(2 of 5 Drawing Sheet(s) Filed in Color)



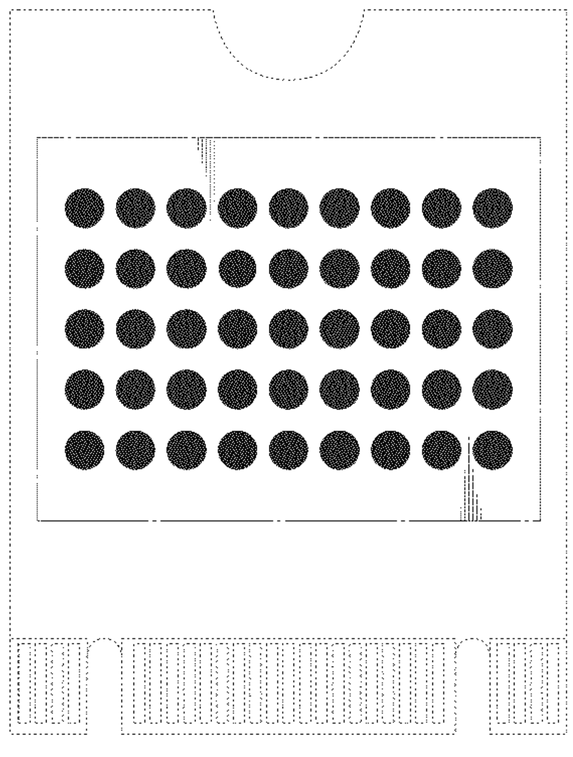


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Fig. 1

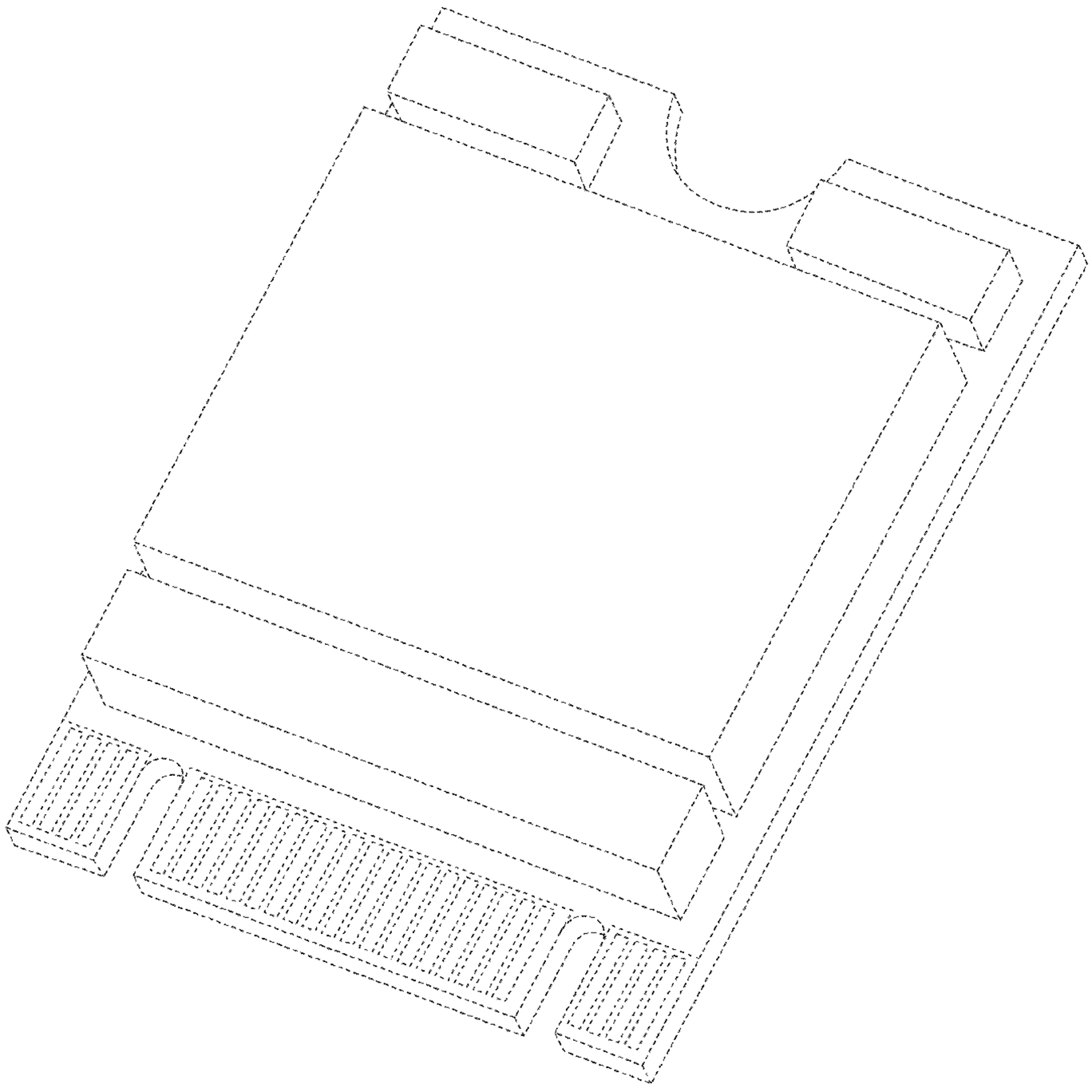


Fig. 2

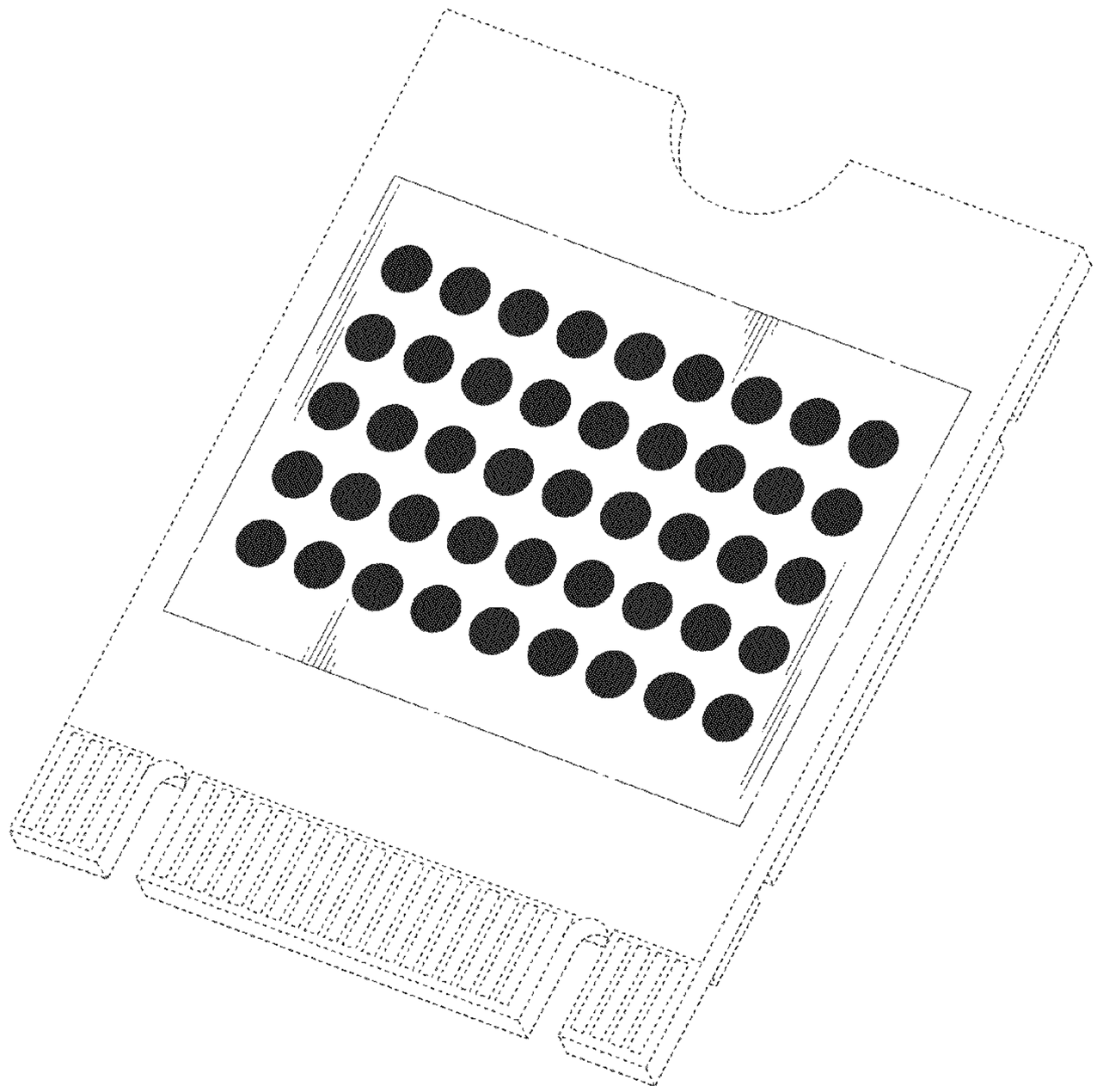


Fig. 3

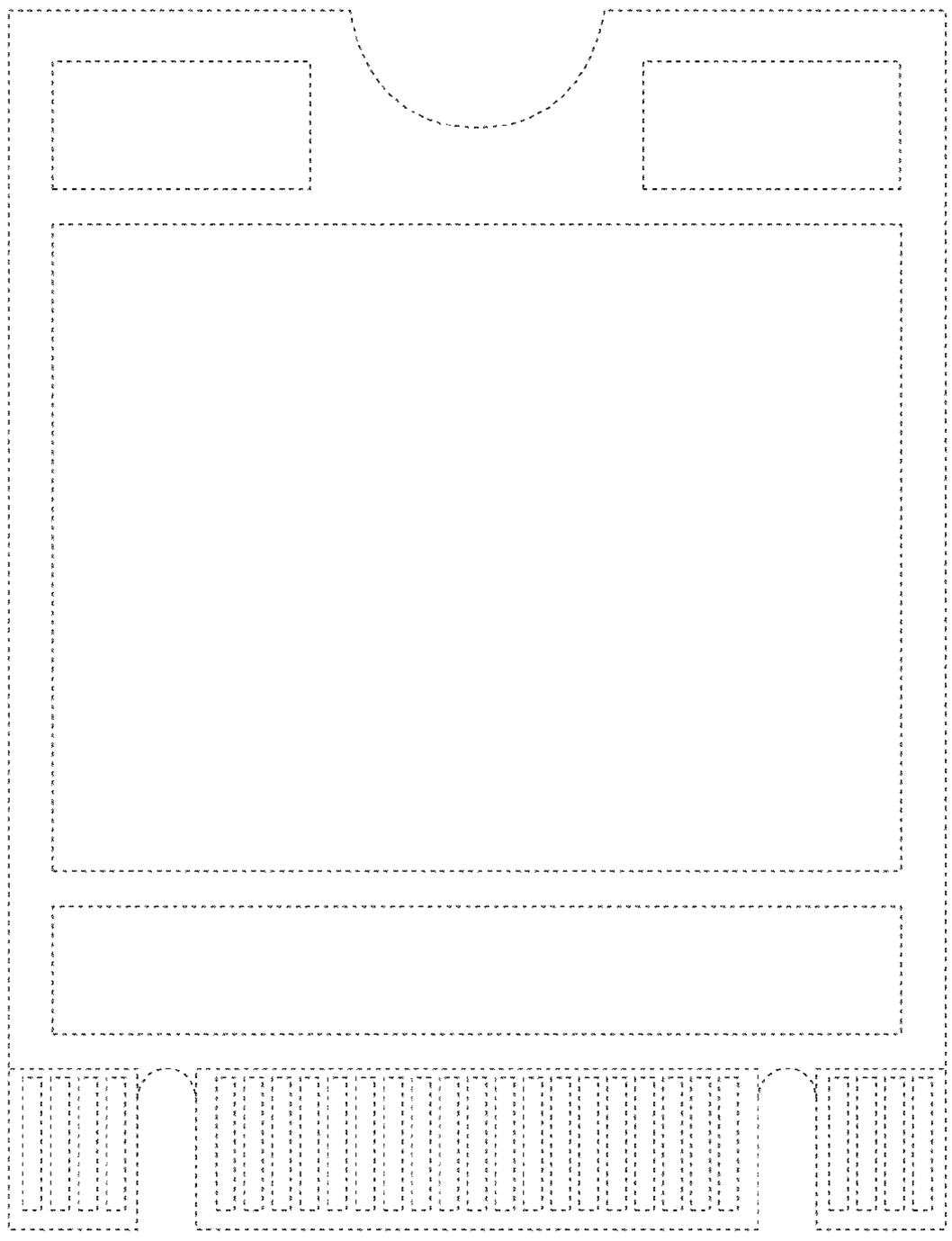


Fig. 4

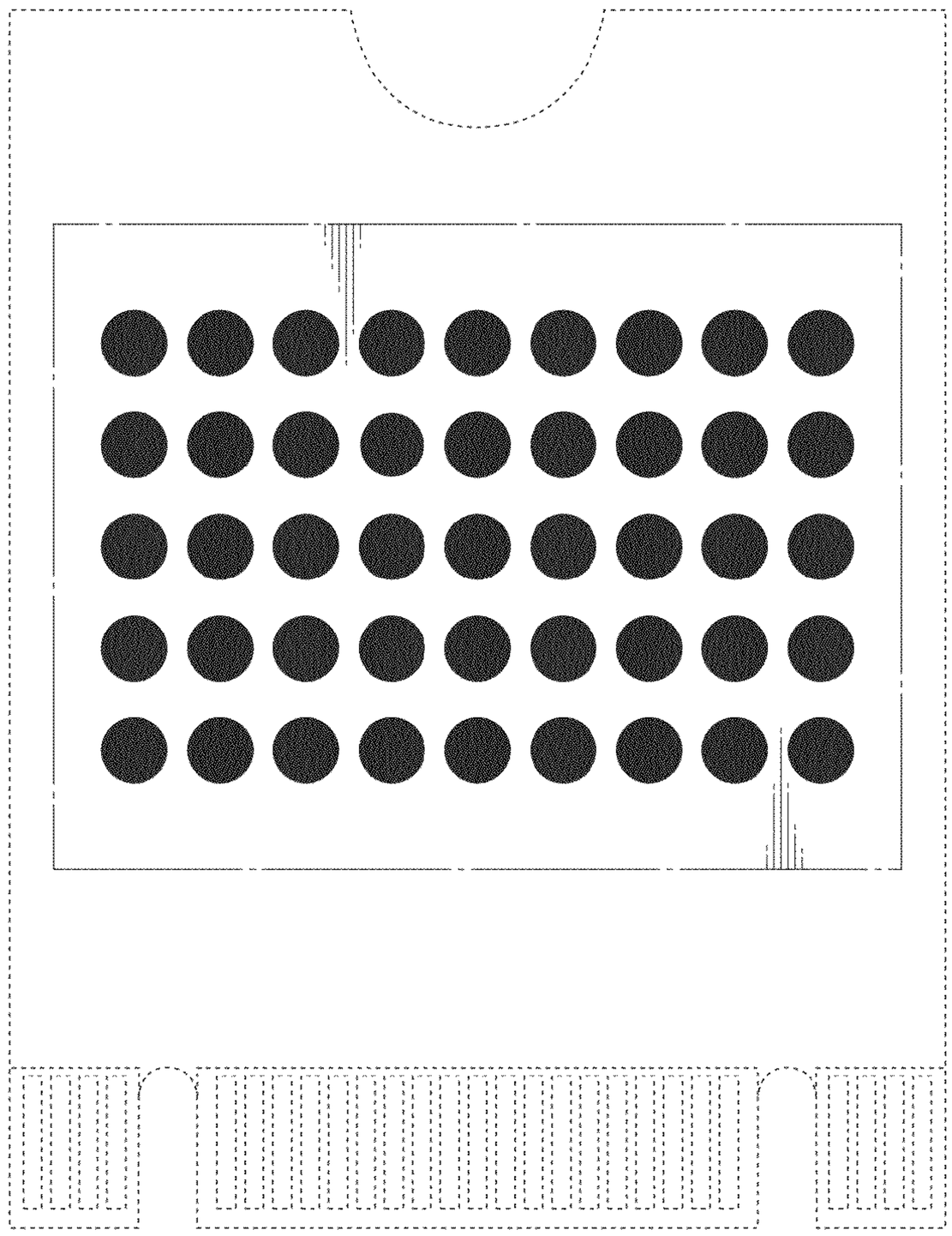


Fig. 5

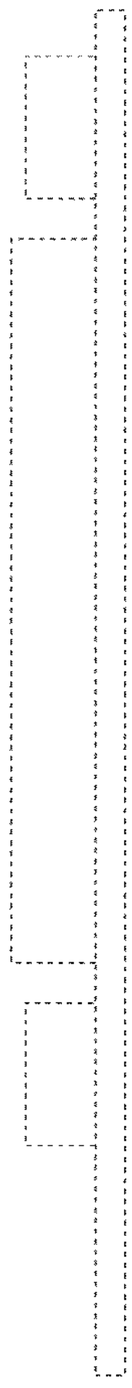


Fig. 6

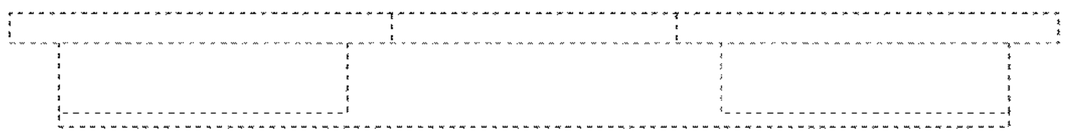
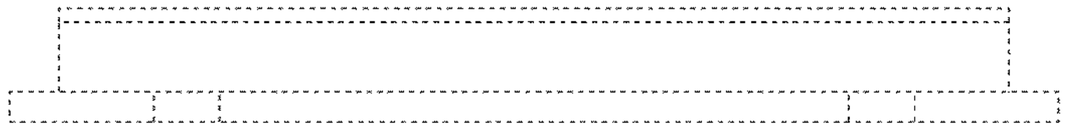


Fig. 7



UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : D730,304 S
APPLICATION NO. : 29/500867
DATED : May 26, 2015
INVENTOR(S) : Manabu Matsumoto et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title page, Under Inventors:

Please delete "Manabu Matsumoto, Yokosuka (JP); Isao Ozama, Yokosuka (JP)" and replace with -- Manabu Matsumoto, Yokohama (JP); Isao Ozama, Chigasaki (JP) --

Signed and Sealed this
Twenty-ninth Day of December, 2015

Michelle K. Lee

Michelle K. Lee
Director of the United States Patent and Trademark Office