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(12) United States Design Patent

Kaneko et al.

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(54) **OUTER TUBE FOR PROCESS TUBE FOR MANUFACTURING SEMICONDUCTOR WAFERS**

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(73) Assignee: **Tokyo Electron Limited**, Minato-Ku (JP)

(**) Term: **14 Years**

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(22) Filed: **May 10, 2012**

(30) **Foreign Application Priority Data**

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182; D23/266; D7/600.1, 600.2; 118/715, 722, 724, 725; 219/385, 390, 219/486, 520, 523; 83/35, 39; 138/118, 138/118.1, 121, 177, 178; 206/454, 711; 211/41.18; 414/935; 432/247, 253
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,950,870	A *	8/1990	Mitsuhashi et al.	219/390
5,037,502	A *	8/1991	Suzuki et al.	117/89
5,352,293	A *	10/1994	Yang et al.	118/715
5,618,349	A *	4/1997	Yuuki	118/715
D404,368	S *	1/1999	Shimazu	D13/182
D405,062	S *	2/1999	Shimazu	D13/182
D405,429	S *	2/1999	Hanagata et al.	D13/182
D405,431	S *	2/1999	Shimazu	D13/182
D406,113	S *	2/1999	Hanagata et al.	D13/182
5,897,311	A *	4/1999	Nishi	432/239
5,948,300	A *	9/1999	Gero et al.	219/390
5,968,593	A *	10/1999	Sakamoto et al.	427/248.1
D417,438	S *	12/1999	Matsushima	D13/182
D423,463	S *	4/2000	Hanagata et al.	D13/182
D424,024	S *	5/2000	Hanagata et al.	D13/182
6,251,189	B1 *	6/2001	Odake et al.	118/715
D521,464	S *	5/2006	Ishii et al.	D13/182
D521,465	S *	5/2006	Ishii et al.	D13/182
D556,704	S *	12/2007	Nakamura et al.	D13/182
7,311,520	B2 *	12/2007	Saito et al.	432/247
D586,768	S *	2/2009	Inoue et al.	D13/182
D590,359	S *	4/2009	Kaneko	D13/182
D600,659	S *	9/2009	Matsuura et al.	D13/182
D611,013	S *	3/2010	Takahashi	D13/182
D616,396	S *	5/2010	Sato	D13/182
D618,638	S *	6/2010	Nakashima	D13/182
D619,630	S *	7/2010	Kaneko	D15/138
2002/0014483	A1 *	2/2002	Suzuki et al.	219/486
2003/0221779	A1 *	12/2003	Okuda et al.	156/345.26
2008/0083372	A1 *	4/2008	Inoue et al.	118/725
2008/0132079	A1 *	6/2008	Okada et al.	438/734

* cited by examiner

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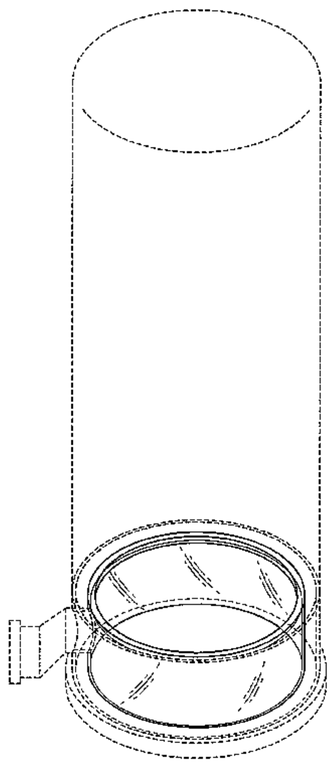
(57) **CLAIM**

The ornamental design for an outer tube for process tube for manufacturing semiconductor wafers, as shown and described.

DESCRIPTION

FIG. **1** is perspective view of an outer tube for process tube for manufacturing semiconductor wafers showing our new design;
FIG. **2** is a front view thereof;
FIG. **3** is a rear view thereof;
FIG. **4** is a right side thereof;
FIG. **5** is a left side view thereof;
FIG. **6** is a top plan view thereof;
FIG. **7** is a bottom plan view thereof; and,
FIG. **8** is a cross-sectional view taken along line **8-8** of FIG. **6**.
The broken lines shown in the drawings represent portions of the outer tube for process tube for manufacturing semiconductor wafers that form no part of the claimed design.

1 Claim, 7 Drawing Sheets



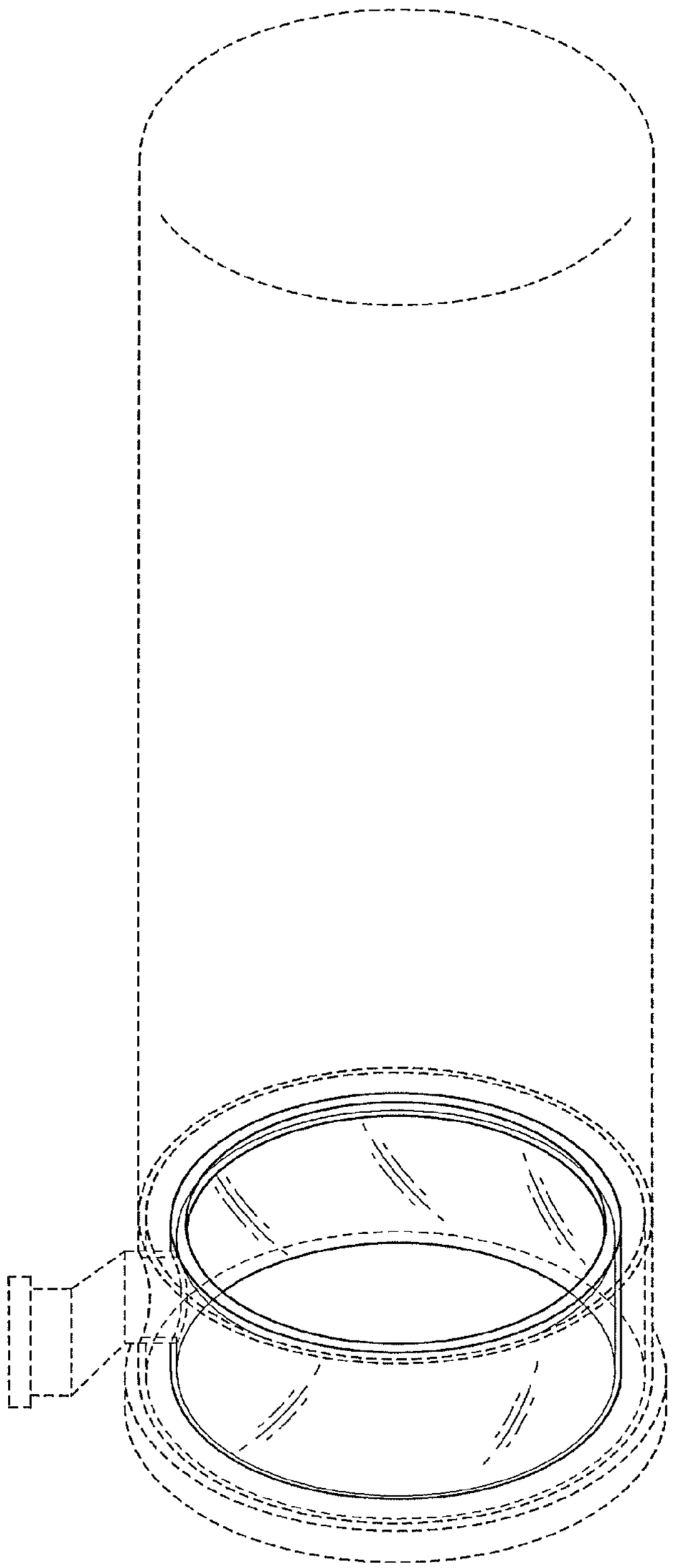


FIG. 1

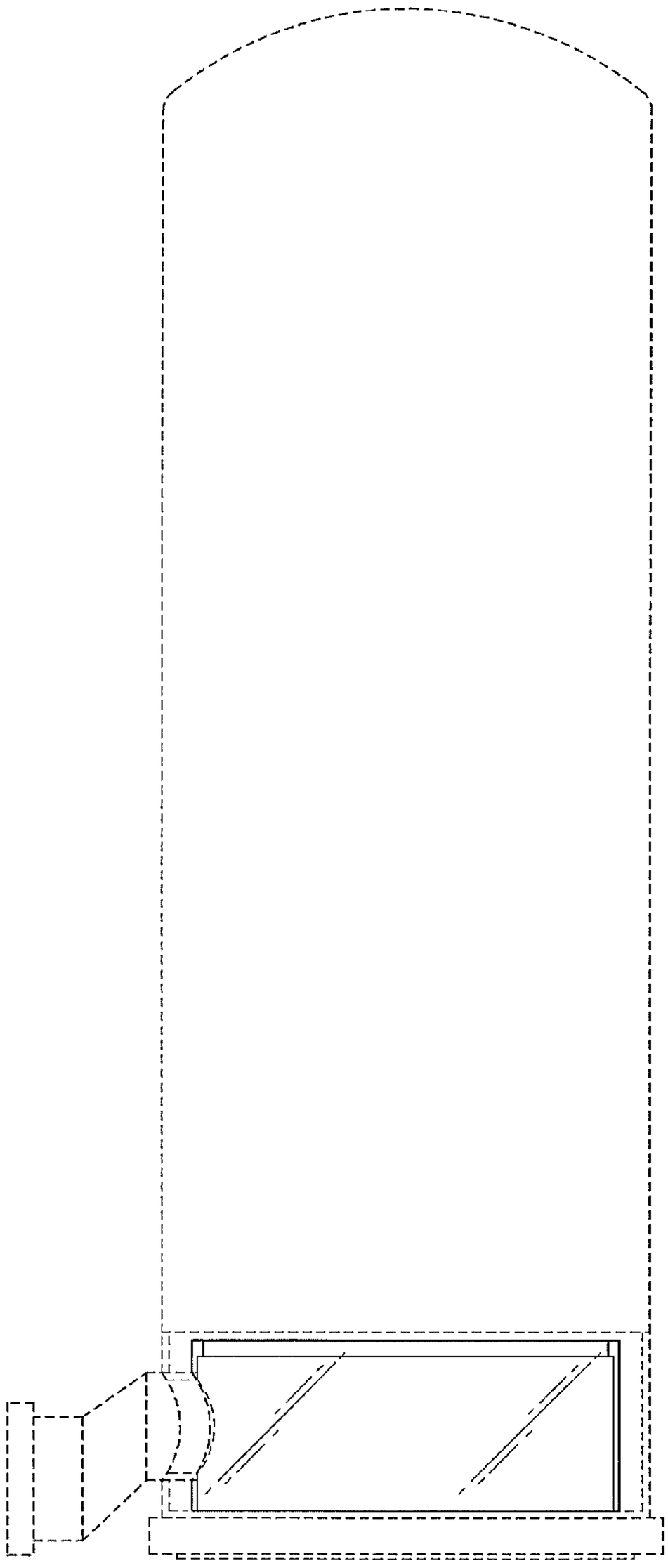


FIG. 2

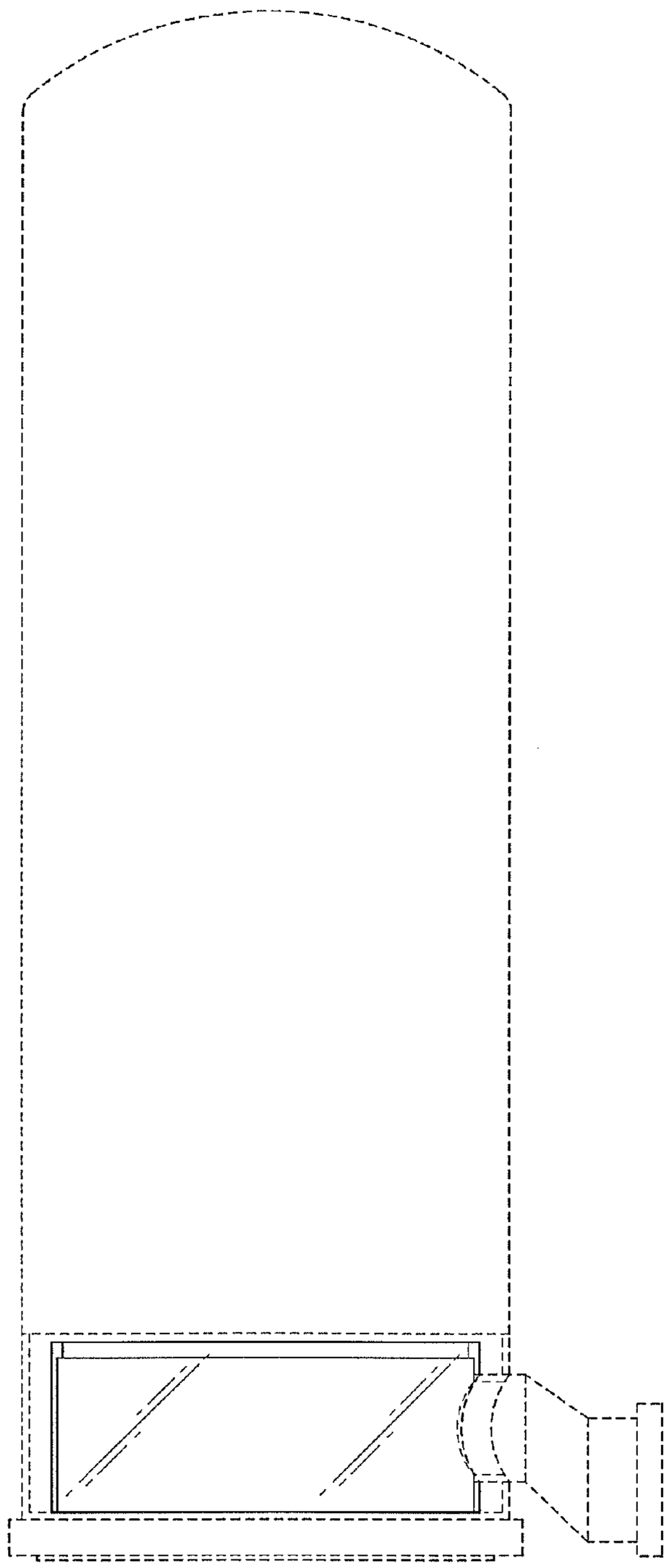


FIG. 3

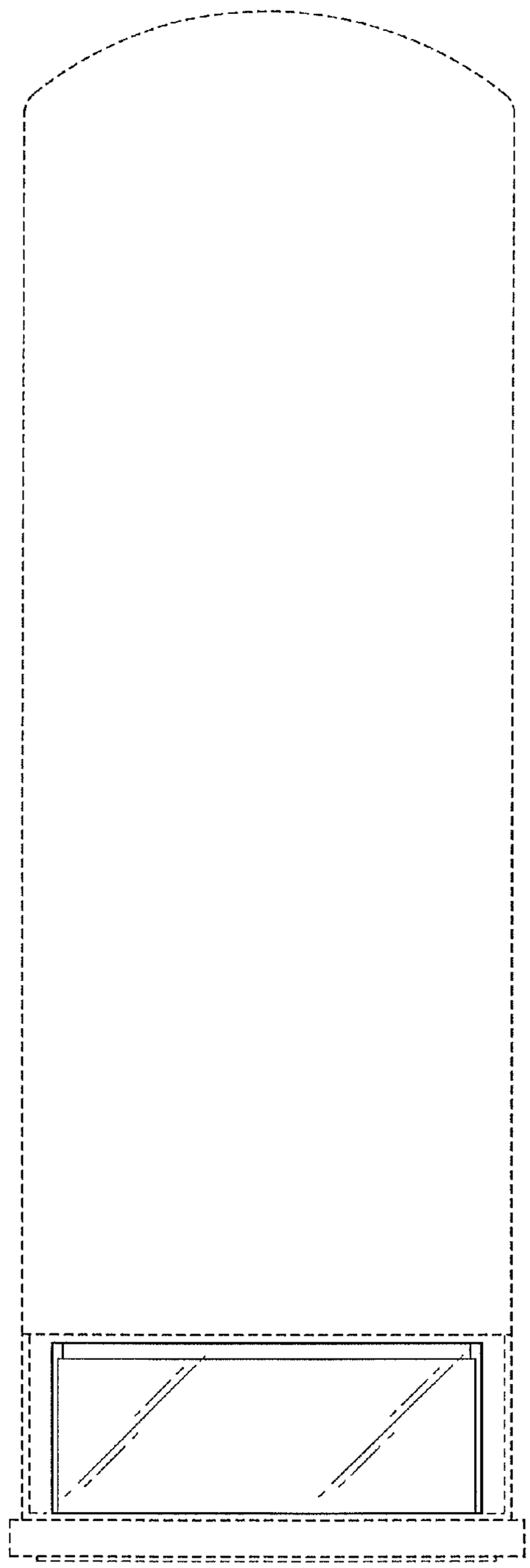


FIG. 4

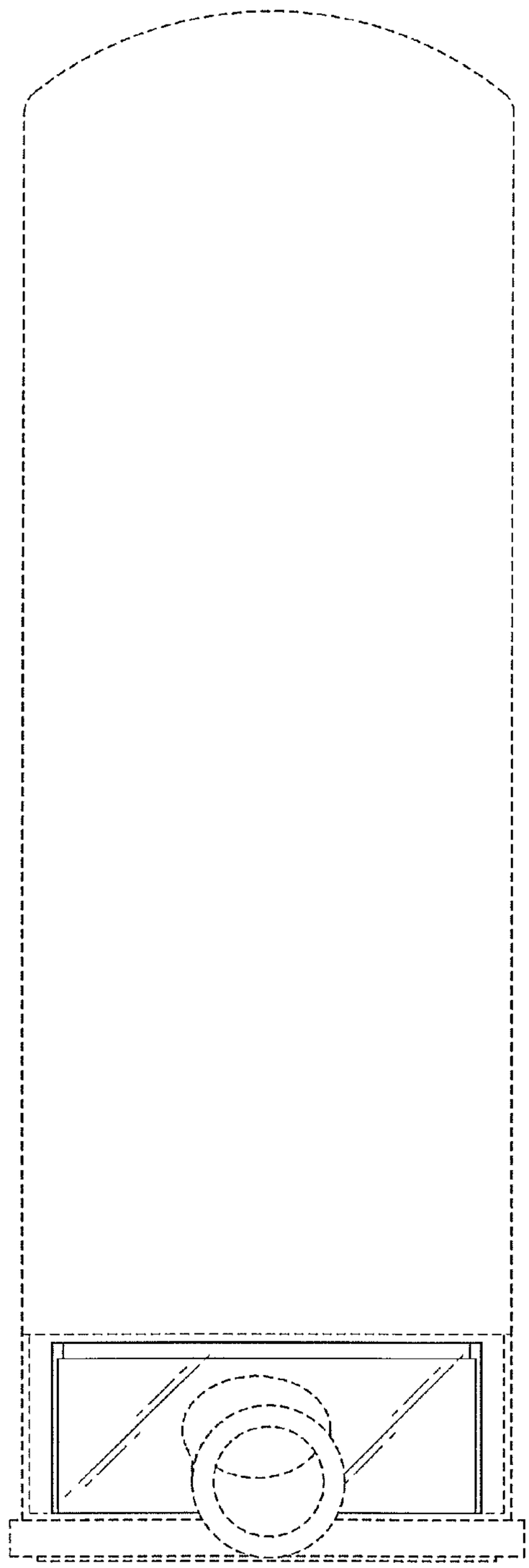


FIG. 5

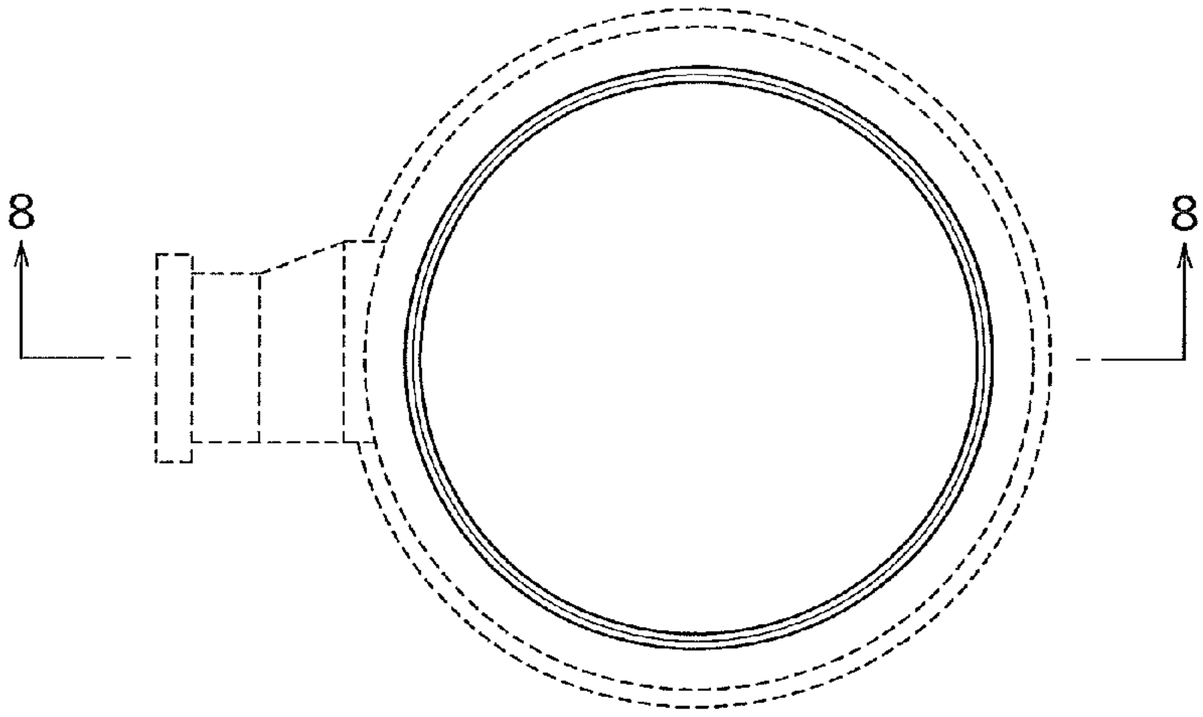


FIG. 6

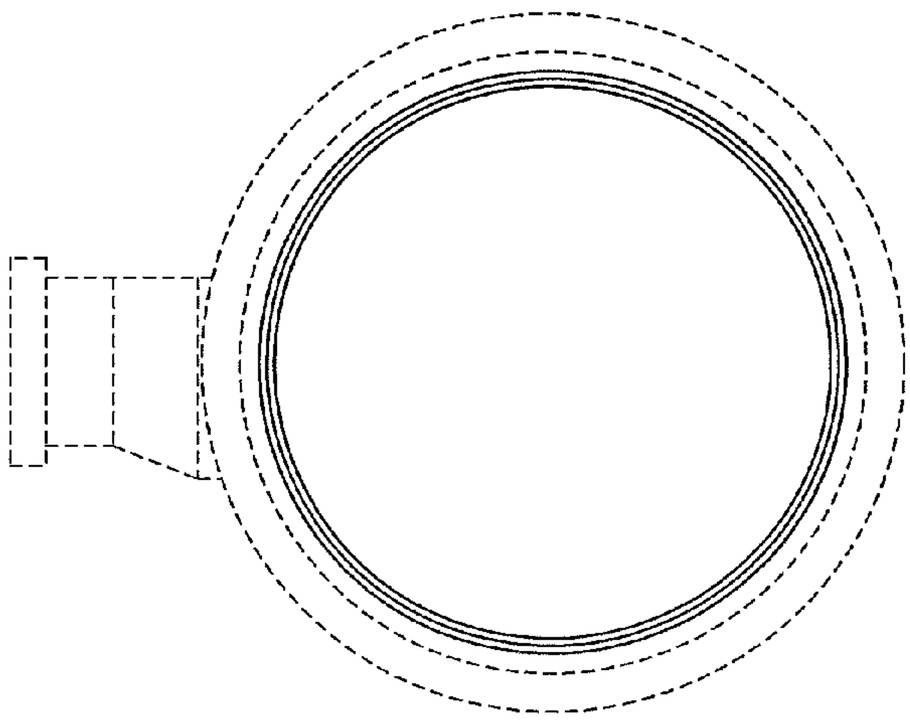


FIG. 7

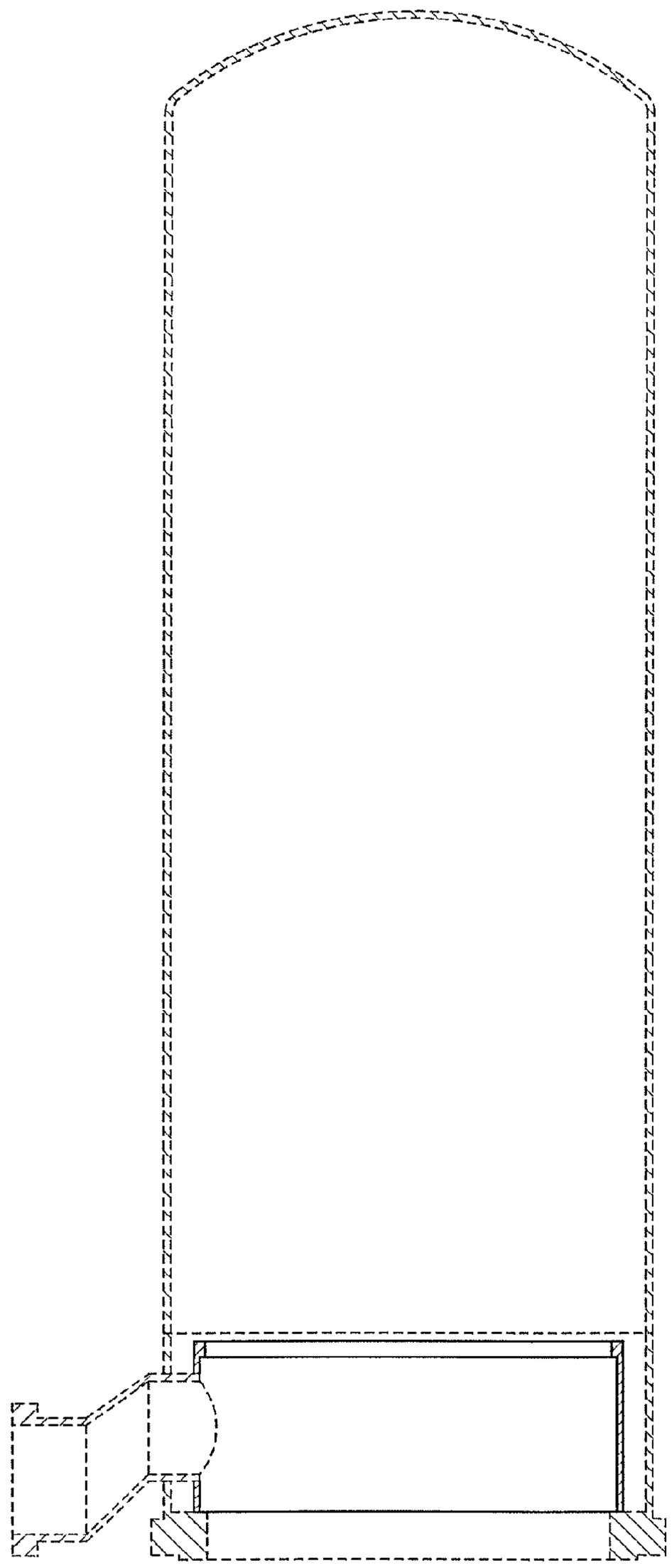


FIG. 8