US00D721340S

(12) **United States Design Patent**
Nakamura

(10) **Patent No.: US D721,340 S**
(45) **Date of Patent: ** Jan. 20, 2015**

(54) **SEMICONDUCTOR MODULE**

(71) Applicant: **Fuji Electric Co., Ltd.**, Kawasaki (JP)

(72) Inventor: **Hideyo Nakamura**, Kawasaki (JP)

(73) Assignee: **Fuji Electric Co., Ltd.**, Kawasaki-shi, Kanagawa (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/458,667**

(22) Filed: **Jun. 21, 2013**

(30) **Foreign Application Priority Data**

Dec. 21, 2012 (JP) D2012-031249

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
CPC . H01L 21/00; H01L 2224/42; H01L 2224/43; H01L 2021/00; H01L 2021/02; H01L 2021/04; H01L 21/4814; H01L 21/4846; H01L 21/4871; H01L 21/67144; H01L 23/12; H01L 23/13; H01L 23/14; H01L 23/147; H01L 2924/171; H01L 2924/1711; H01L 2924/1715; H01L 2924/17151; H01L 2924/181; H01L 2924/1811; H01L 2924/1815; H01L 2924/19042; H01L 2924/1905; H01L 2224/08054; H01L 23/58; H05B 41/14; G02B 6/4201; G02B 6/4256; G02B 6/4257; G02B 6/4261; G02B 6/4262; G02B 6/428; G02B 6/4281; H05K 1/14; H05K 1/141; H05K 1/142; H05K 1/144; H05K 1/18; H05K 1/181; H05K 1/182; H05K 1/026
USPC D13/110, 182; 257/678, 684, 690, 691; 361/679.01, 713, 728, 736, 760, 761, 361/772, 775, 783, 820; 174/250, 253; 438/15, 25, 26, 51, 55, 63, 64, 106
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,408,128	A *	4/1995	Furnival	....	257/690
5,410,450	A *	4/1995	Iida et al.	....	361/736
D364,383	S *	11/1995	Yamada et al.	....	D13/182
D364,384	S *	11/1995	Shimizu et al.	....	D13/182
D364,385	S *	11/1995	Shimizu et al.	....	D13/182
6,078,501	A *	6/2000	Catrambone et al.	....	361/704
D441,726	S *	5/2001	Sofue et al.	....	D13/182
D441,727	S *	5/2001	Sekimoto	....	D13/182
6,521,983	B1 *	2/2003	Yoshimatsu et al.	....	257/678
D476,959	S *	7/2003	Yamada et al.	....	D13/182
D525,215	S *	7/2006	Hisaishi et al.	....	D13/182
D539,761	S *	4/2007	Takahashi et al.	....	D13/182
D548,202	S *	8/2007	Takahashi et al.	....	D13/182
D548,203	S *	8/2007	Takahashi et al.	....	D13/182
D587,662	S *	3/2009	Soutome et al.	....	D13/182

(Continued)

Primary Examiner — Elizabeth J Oswecki

(74) *Attorney, Agent, or Firm* — Young Basile Hanlon & MacFarlane P.C.

(57) **CLAIM**

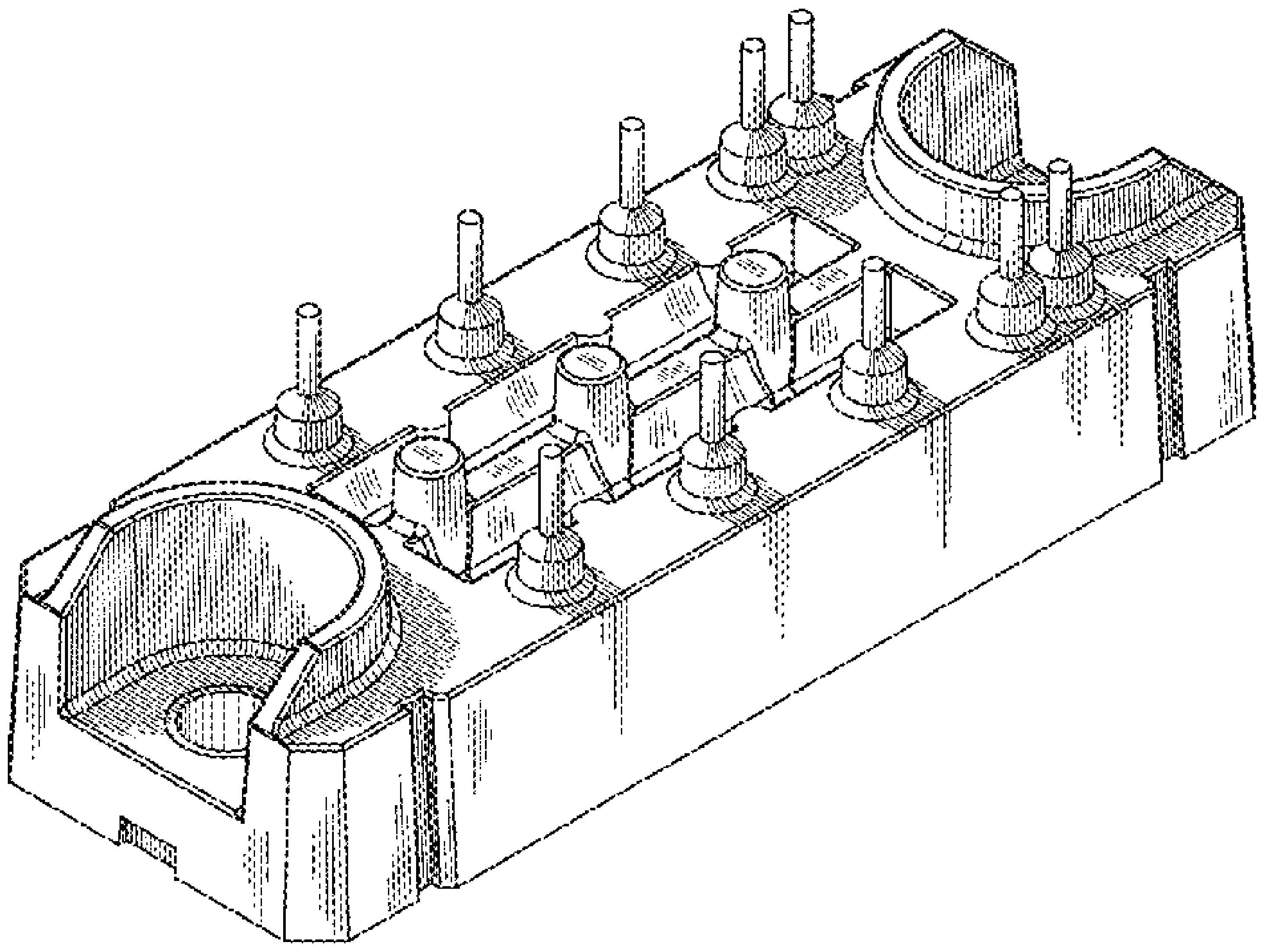
The ornamental design for a semiconductor module, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a semiconductor module showing my new design;
FIG. **2** is a rear view thereof;
FIG. **3** is a left side view thereof;
FIG. **4** is a right side view thereof;
FIG. **5** is a top plan view thereof;
FIG. **6** is a bottom plan view thereof;
FIG. **7** is a perspective view thereof; and,
FIG. **8** is a cross-sectional view thereof taken along line **8-8** of FIG. **5**.

The ornamental design of the present disclosure is a semiconductor module on which power semiconductor elements and the like may be mounted. A plurality of pin-shaped terminals protrudes from the top surface. Each end in a longitudinal direction includes a mounting hole.

1 Claim, 8 Drawing Sheets



(56) References Cited

U.S. PATENT DOCUMENTS

D589,012	S	*	3/2009	Soyano et al.	D13/182
D606,951	S	*	12/2009	Soyano et al.	D13/182
D653,633	S	*	2/2012	Soyano	D13/182
D653,634	S	*	2/2012	Soyano	D13/182
D674,760	S	*	1/2013	Mochizuki et al.	D13/182
D686,174	S	*	7/2013	Soyano	D13/182
D689,446	S	*	9/2013	Soyano	D13/180
8,526,199	B2	*	9/2013	Matsumoto et al.	361/820
D699,693	S	*	2/2014	Otsuka et al.	D13/182
D703,625	S	*	4/2014	Lim et al.	D13/182
D704,670	S	*	5/2014	Chen et al.	D13/182
D704,671	S	*	5/2014	Chen et al.	D13/182
D705,184	S	*	5/2014	Takahashi et al.	D13/182
D706,232	S	*	6/2014	Nakamura	D13/182
D710,317	S	*	8/2014	Chen et al.	D13/182
D710,318	S	*	8/2014	Chen et al.	D13/182
D710,319	S	*	8/2014	Chen et al.	D13/182

* cited by examiner

Fig.1

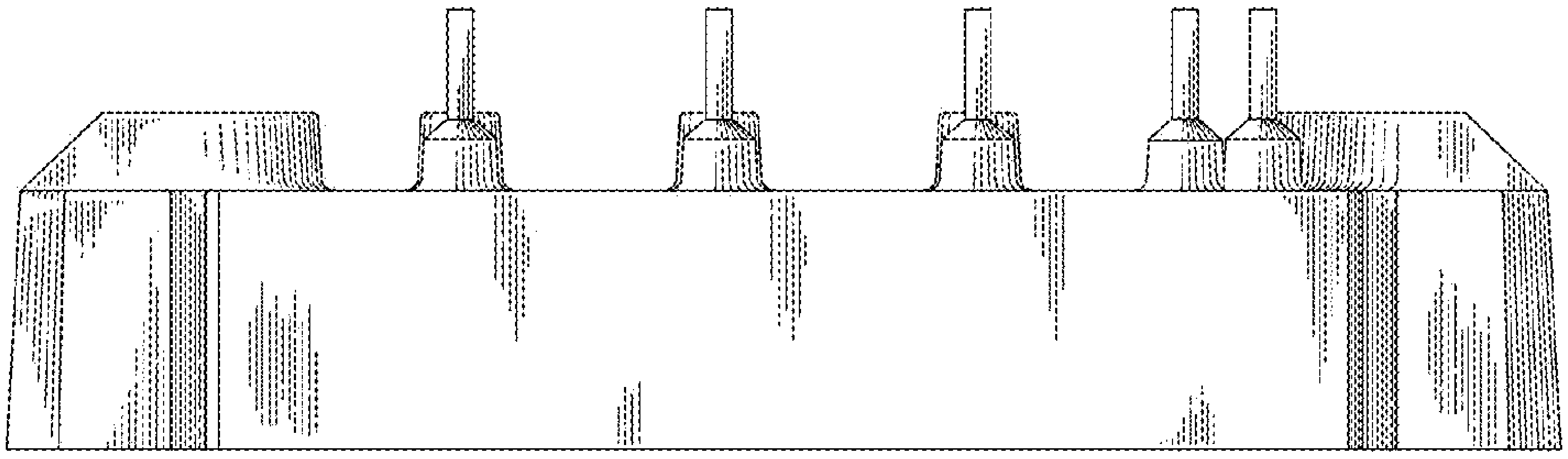


Fig.2

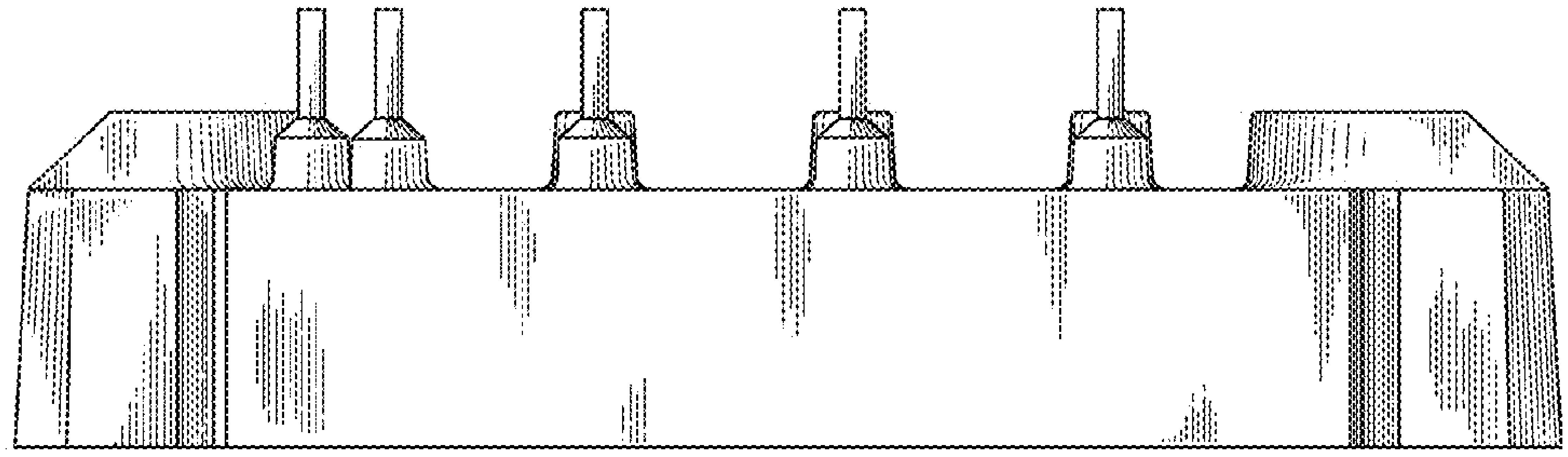


Fig.3

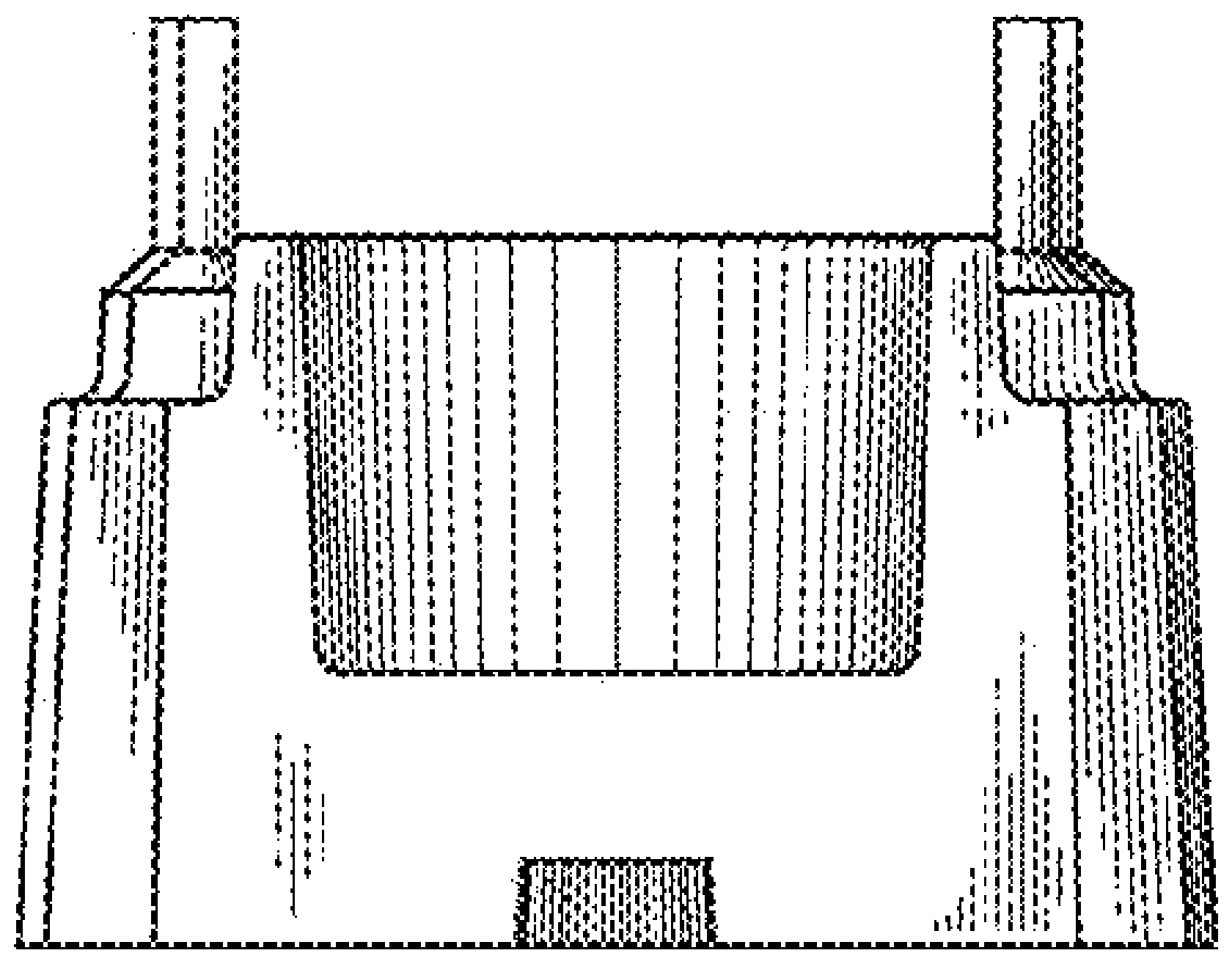


Fig.4

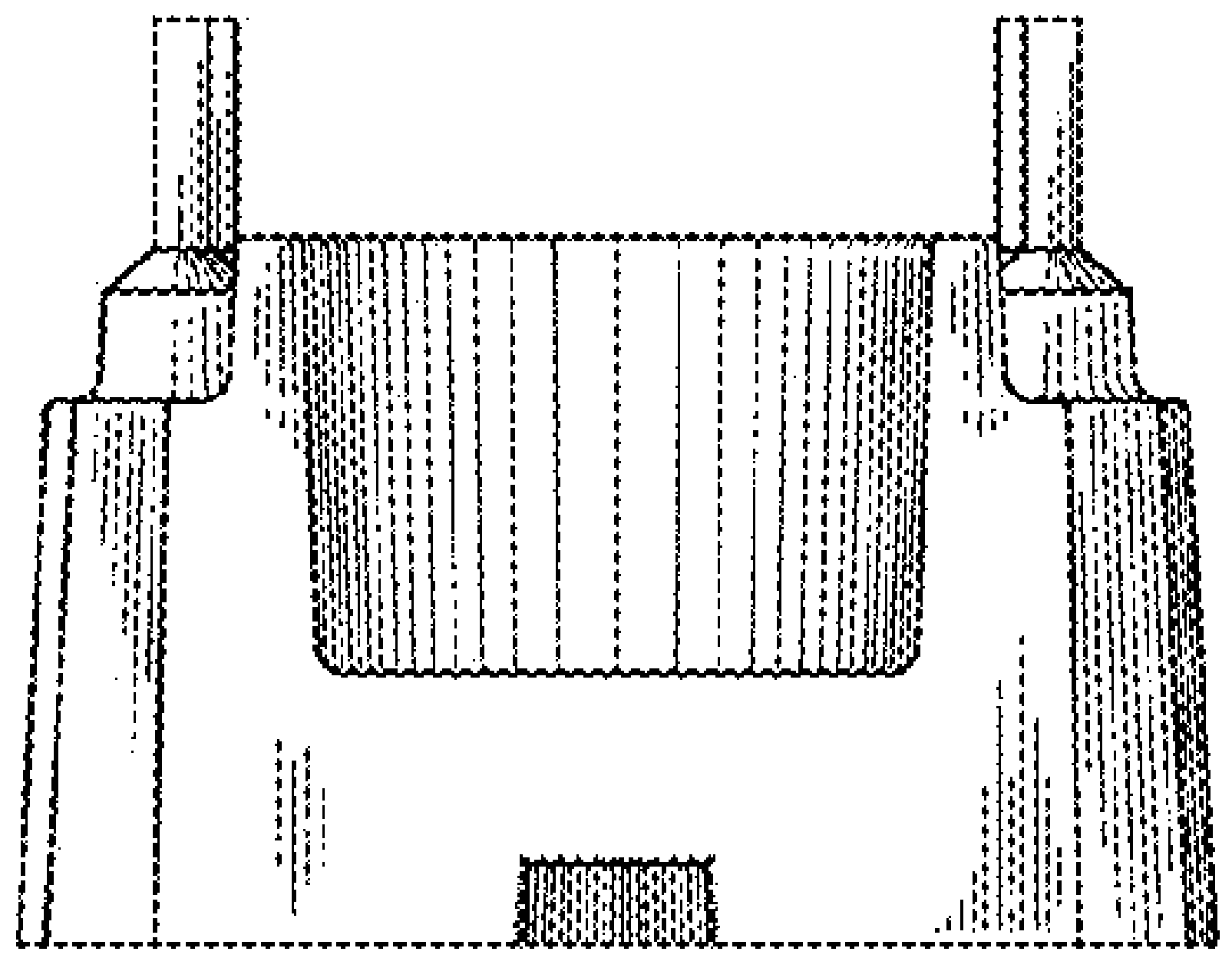


Fig.5

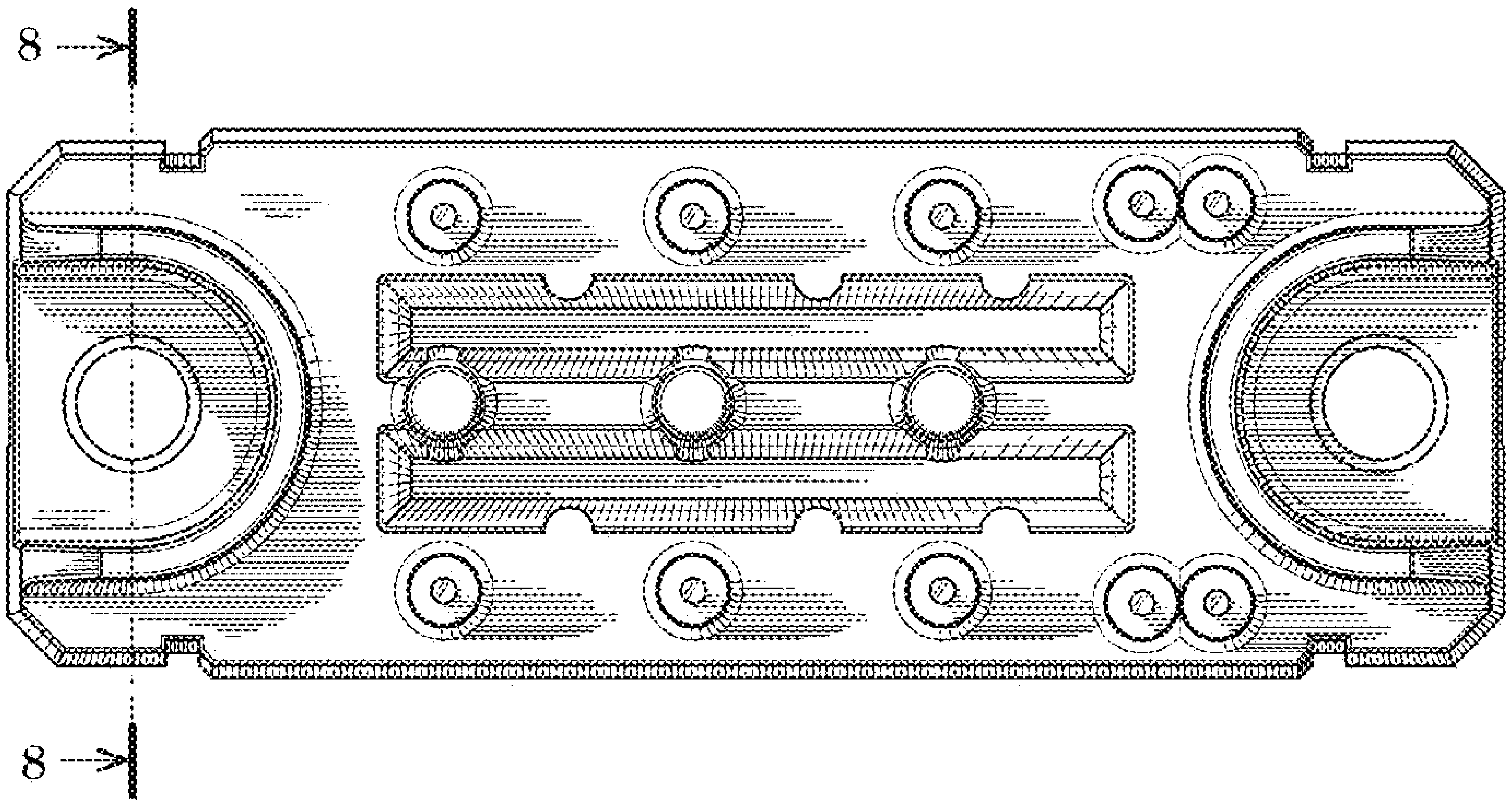


Fig.6

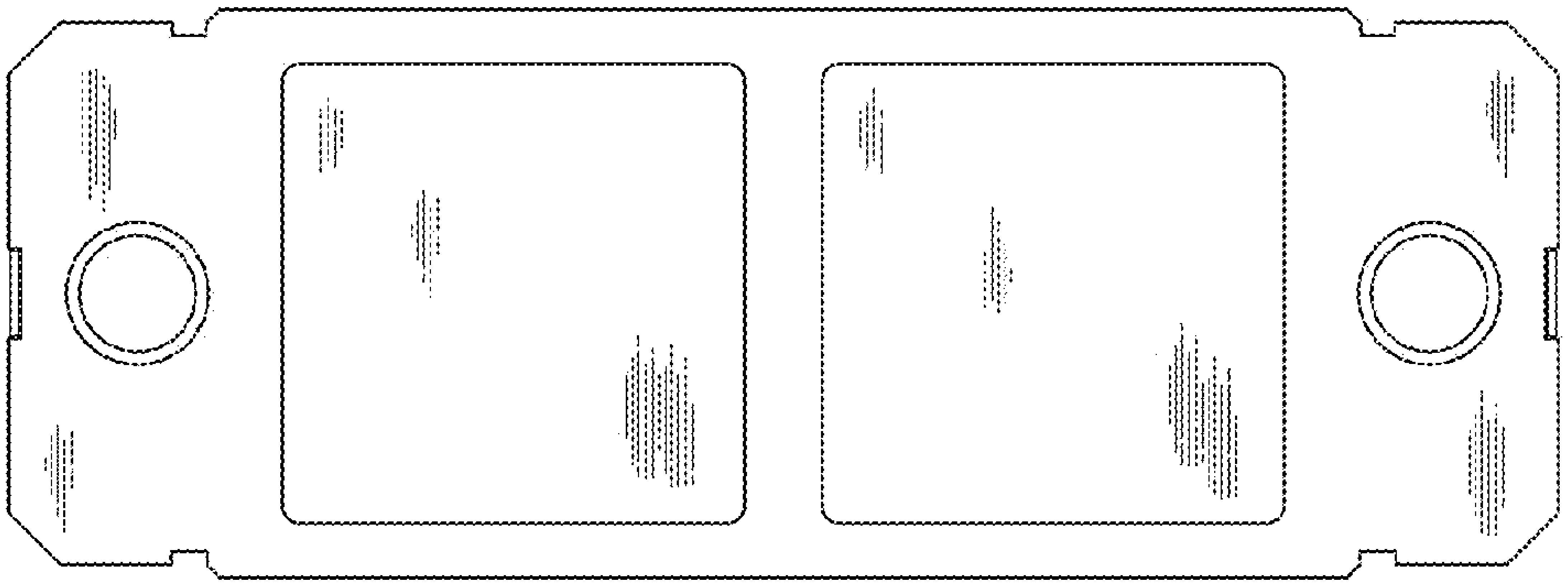


Fig. 7

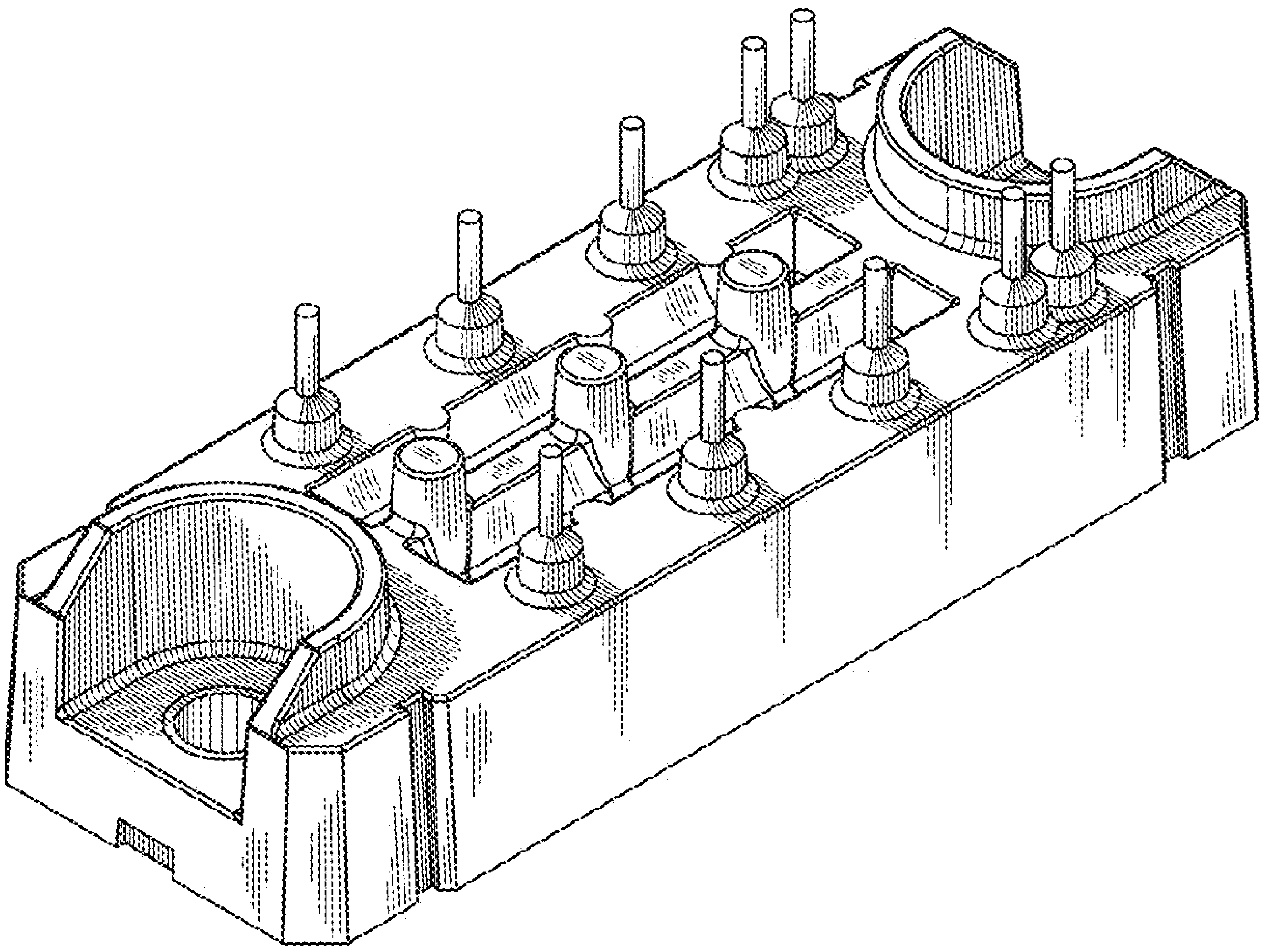


Fig.8