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Nakamura

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(54) **SEMICONDUCTOR MODULE**

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(52) **U.S. Cl.**
USPC **D13/182**

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CPC . H01L 21/00; H01L 2224/42; H01L 2224/43; H01L 2021/00; H01L 2021/02; H01L 2021/04; H01L 21/4814; H01L 21/4846; H01L 21/4871; H01L 21/67144; H01L 23/12; H01L 23/13; H01L 23/14; H01L 23/147; H01L 2924/171; H01L 2924/1711; H01L 2924/1715; H01L 2924/17151; H01L 2924/181; H01L 2924/1811; H01L 2924/1815; H01L 2924/19042; H01L 2924/1905; H01L 2224/08054; H01L 23/58; H05B 41/14; G02B 6/4201; G02B 6/4256; G02B 6/4257; G02B 6/4261; G02B 6/4262; G02B 6/428; G02B 6/4281; H05K 1/14; H05K 1/141; H05K 1/142; H05K 1/144; H05K 1/18; H05K 1/181; H05K 1/182; H05K 1/026
USPC D13/110, 182; 257/678, 684, 690, 691; 361/679.01, 713, 728, 736, 760, 761, 361/772, 775, 783, 820; 174/250, 253; 438/15, 25, 26, 51, 55, 63, 64, 106
See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a semiconductor module, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a semiconductor module showing my new design;

FIG. **2** is a rear view thereof;

FIG. **3** is a left side view thereof;

FIG. **4** is a right side view thereof;

FIG. **5** is a top plan view thereof;

FIG. **6** is a bottom plan view thereof;

FIG. **7** is a perspective view thereof; and,

FIG. **8** is a cross-sectional view thereof taken along line **8**-**8** of FIG. **5**.

The ornamental design of the present disclosure is a semiconductor module on which power semiconductor elements and the like may be mounted. A plurality of pin-shaped terminals protrudes from the top surface. Each end in a longitudinal direction includes a mounting hole.

1 Claim, 8 Drawing Sheets

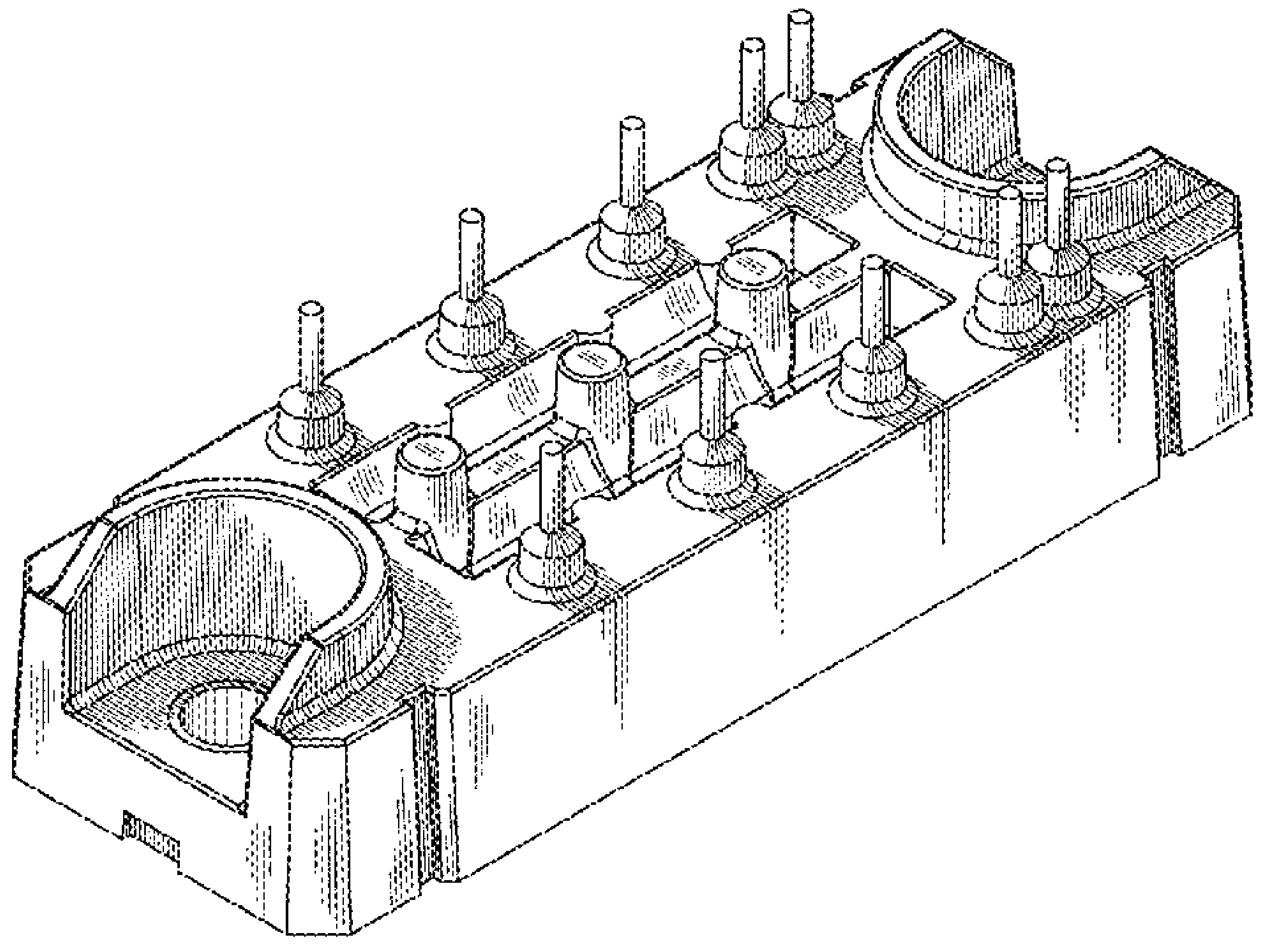

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Fig. 1

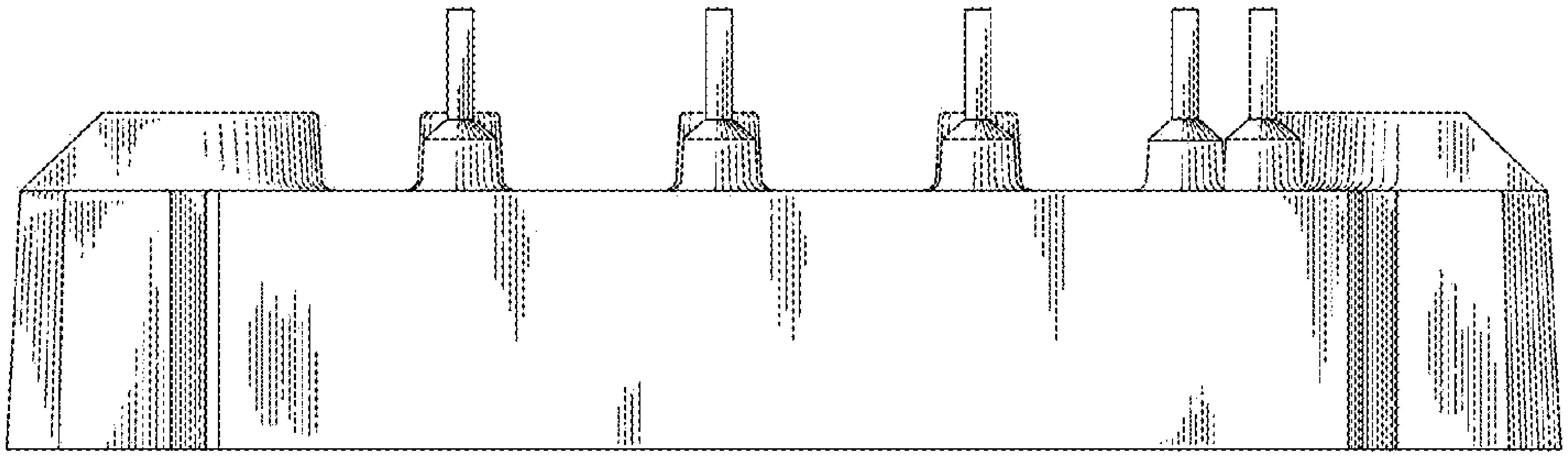

Fig.2

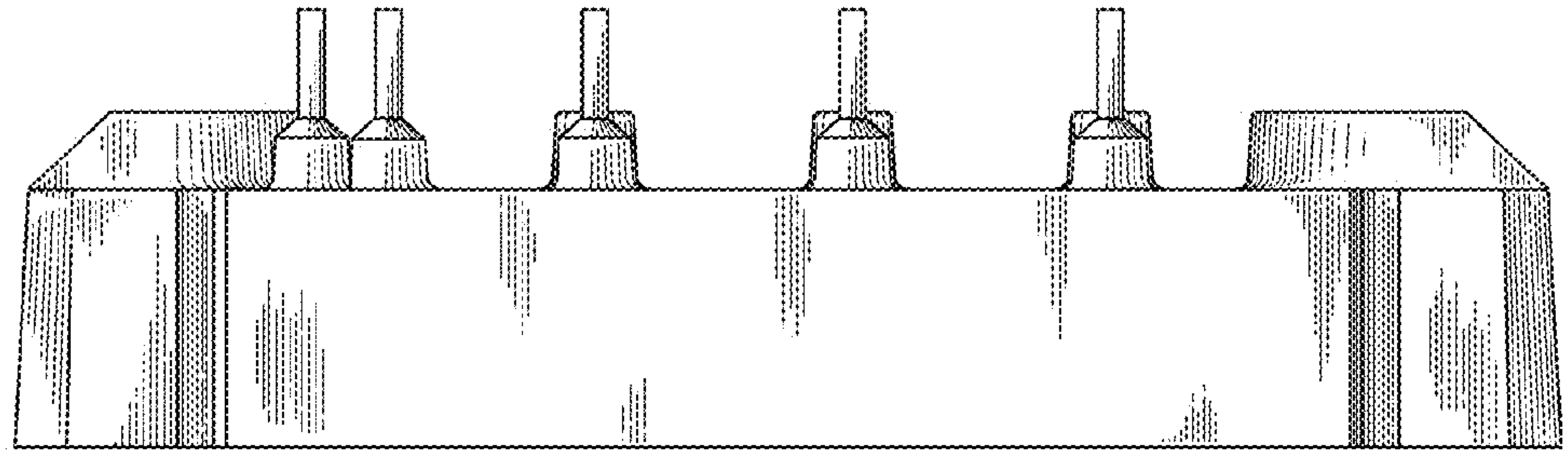

Fig.3

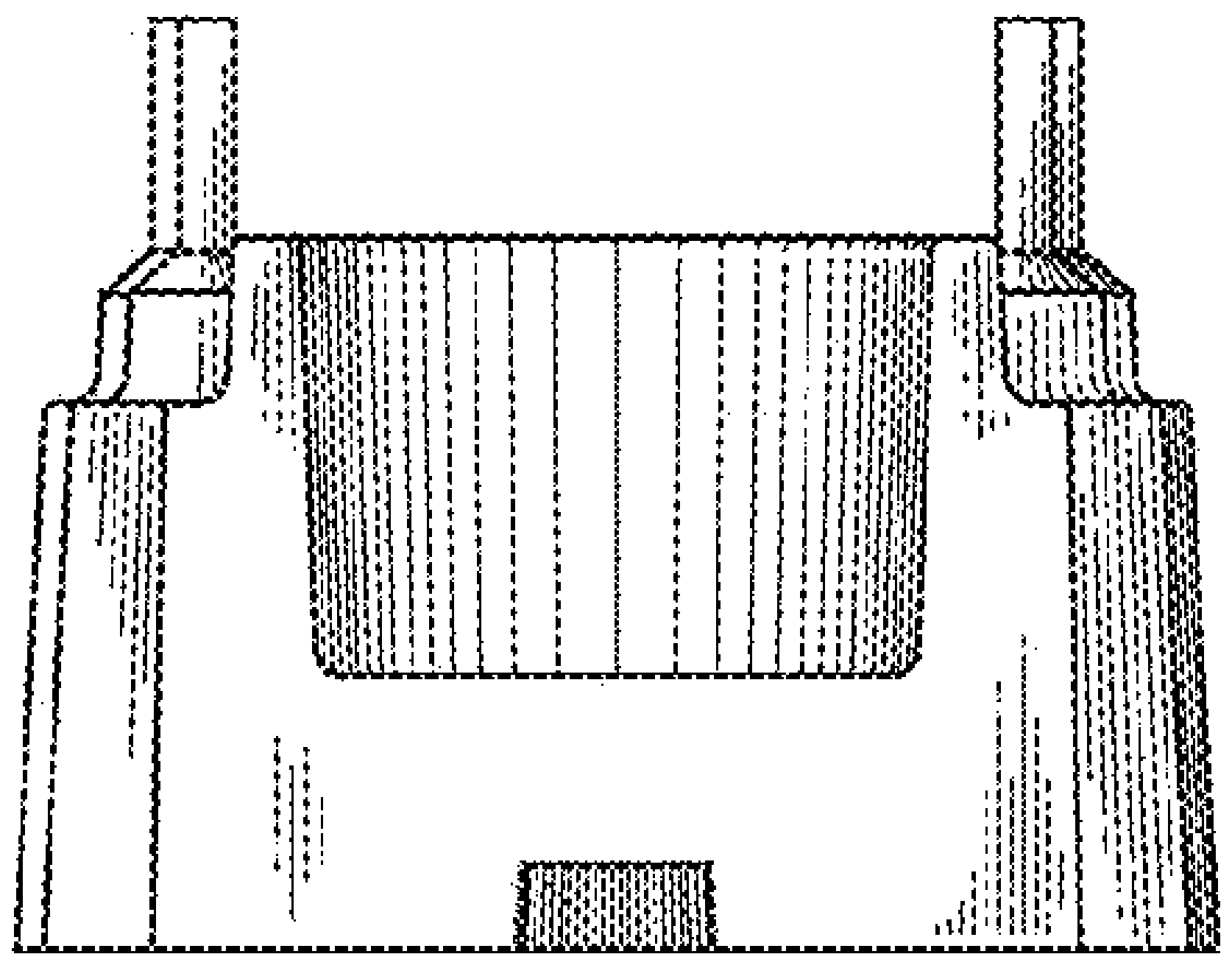

Fig.4

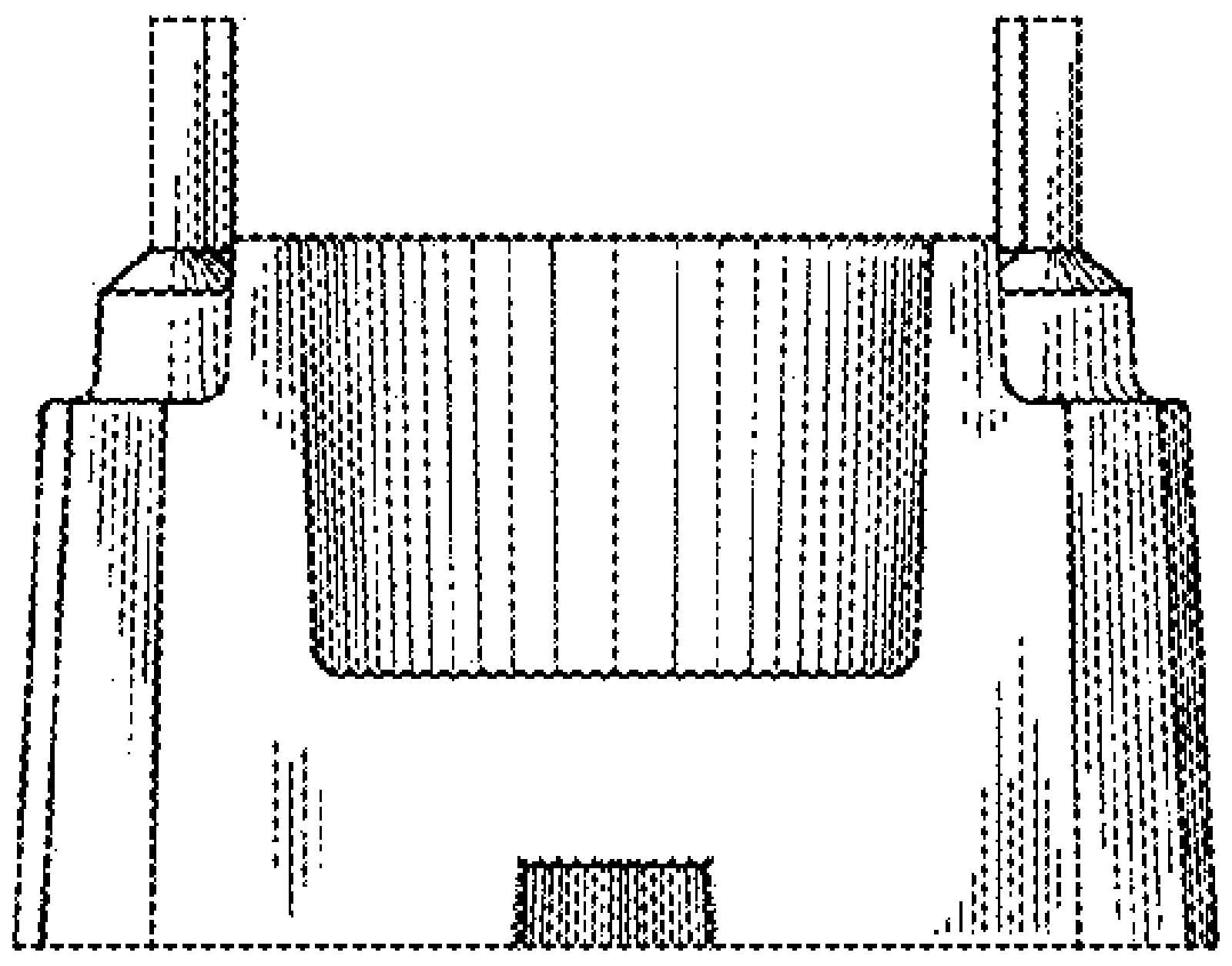

Fig.5

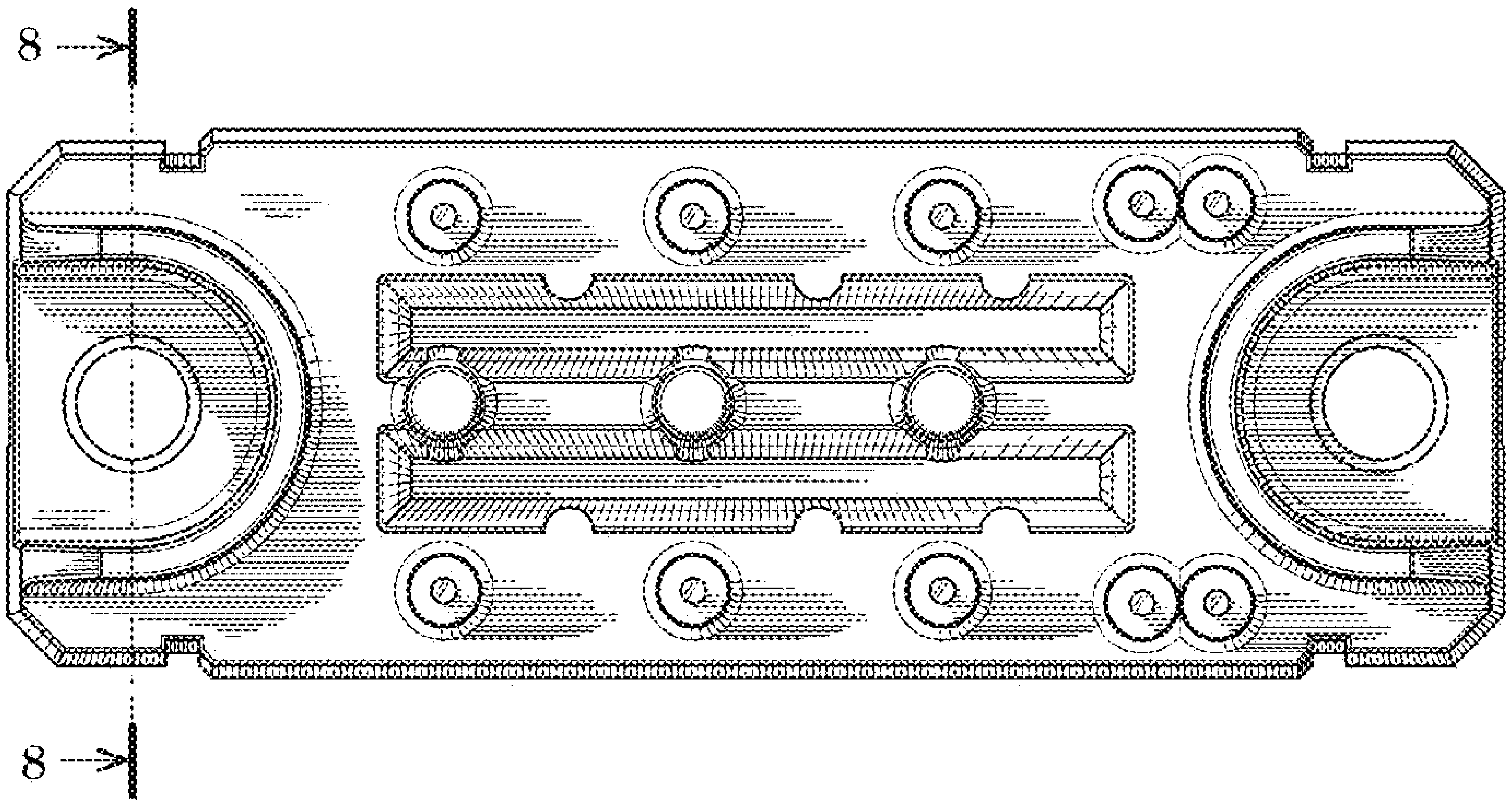

Fig.6

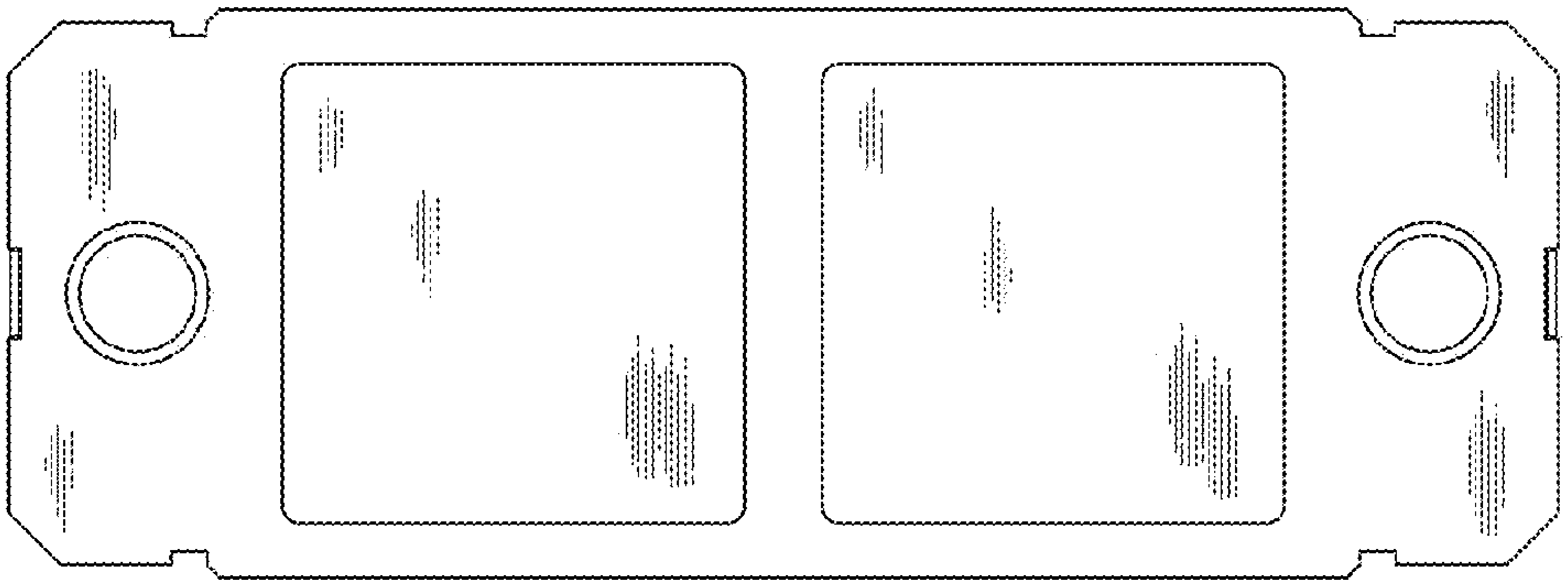

Fig.7

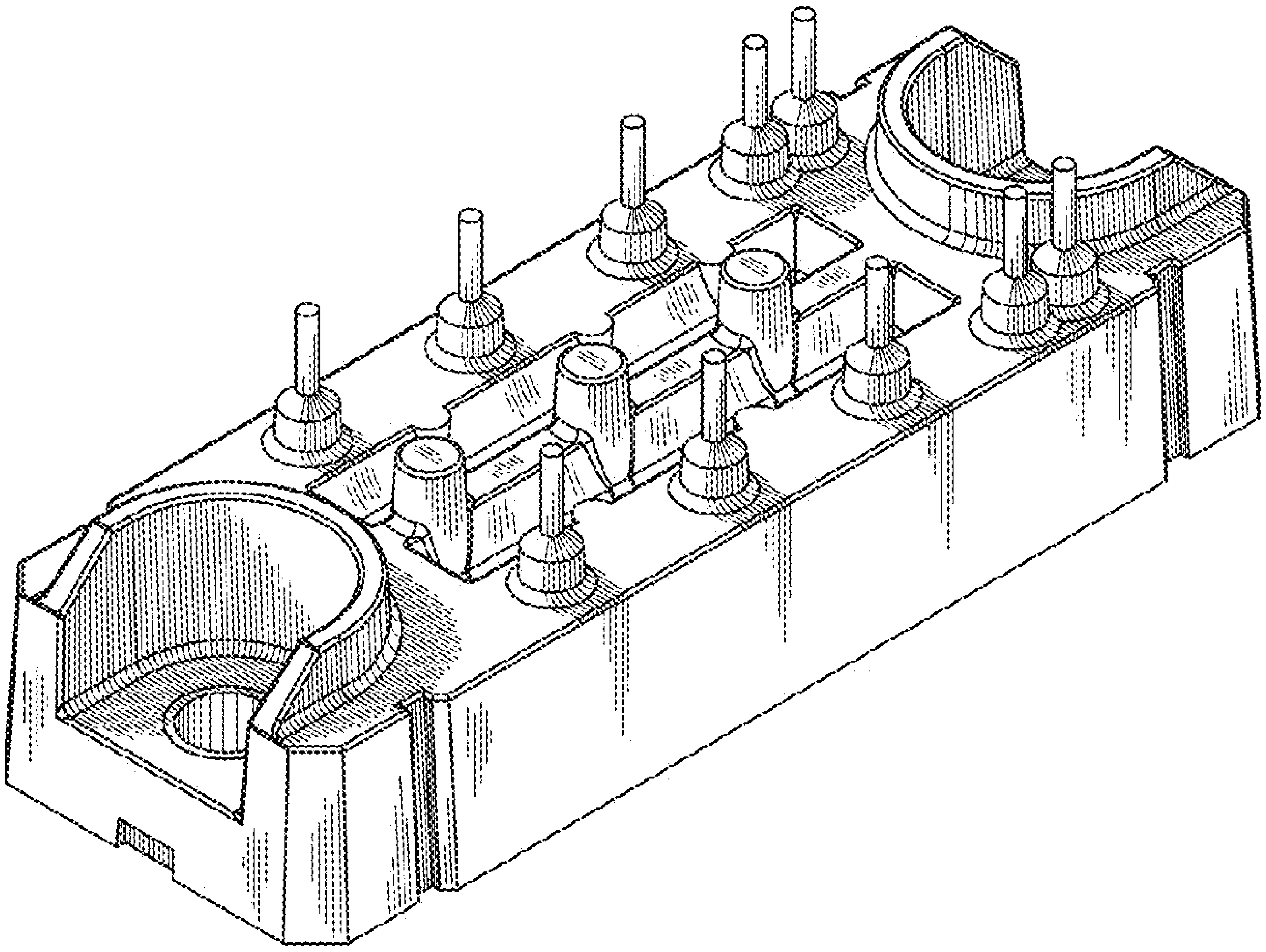

Fig.8