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(12) **United States Design Patent**  
**Nakamura**

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(54) **SEMICONDUCTOR MODULE**  
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H01L 21/4871; H01L 21/67144; H01L 23/12;  
H01L 23/13; H01L 23/14; H01L 23/147;  
H01L 2924/171; H01L 2924/1711; H01L  
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2924/181; H01L 2924/1811; H01L 2924/1815;  
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2224/08054; H01L 23/58; H05B 41/14;  
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G02B 6/4261; G02B 6/4262; G02B 6/428;  
G02B 6/4281; H05K 1/14; H05K 1/141;  
H05K 1/142; H05K 1/144; H05K 1/18;  
H05K 1/181; H05K 1/182; H05K 1/026  
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361/679.01, 713, 728, 736, 760, 761,  
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See application file for complete search history.

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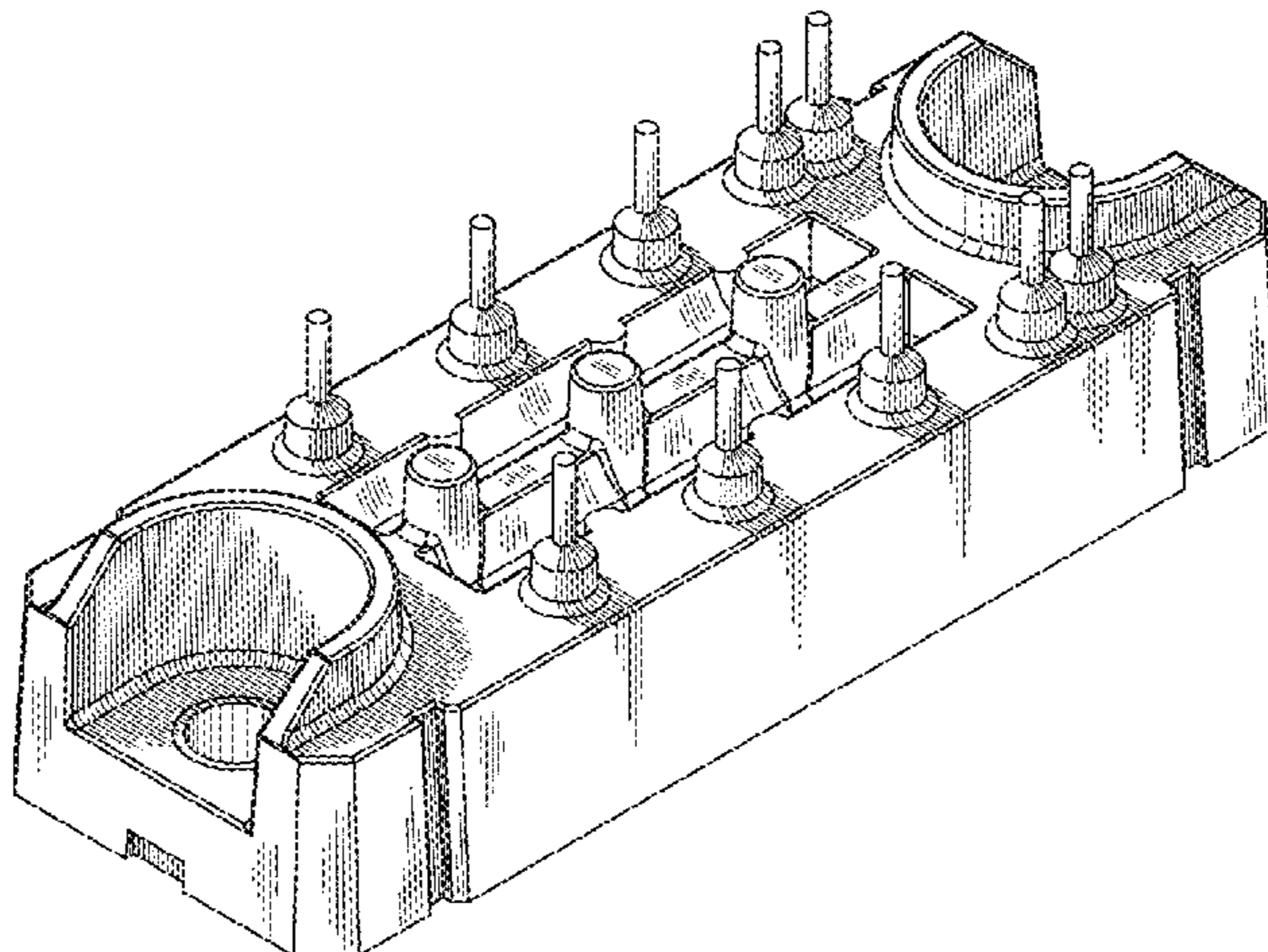
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(57) **CLAIM**  
The ornamental design for a semiconductor module, as shown and described.

**DESCRIPTION**

FIG. 1 is a front view of a semiconductor module showing my new design;  
FIG. 2 is a rear view thereof;  
FIG. 3 is a left side view thereof;  
FIG. 4 is a right side view thereof;  
FIG. 5 is a top plan view thereof;  
FIG. 6 is a bottom plan view thereof;  
FIG. 7 is a perspective view thereof; and,  
FIG. 8 is a cross-sectional view thereof taken along line 8-8 of FIG. 5.  
The ornamental design of the present disclosure is a semiconductor module on which power semiconductor elements and the like may be mounted. A plurality of pin-shaped terminals protrudes from the top surface. Each end in a longitudinal direction includes a mounting hole.

**1 Claim, 8 Drawing Sheets**



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Fig. 1

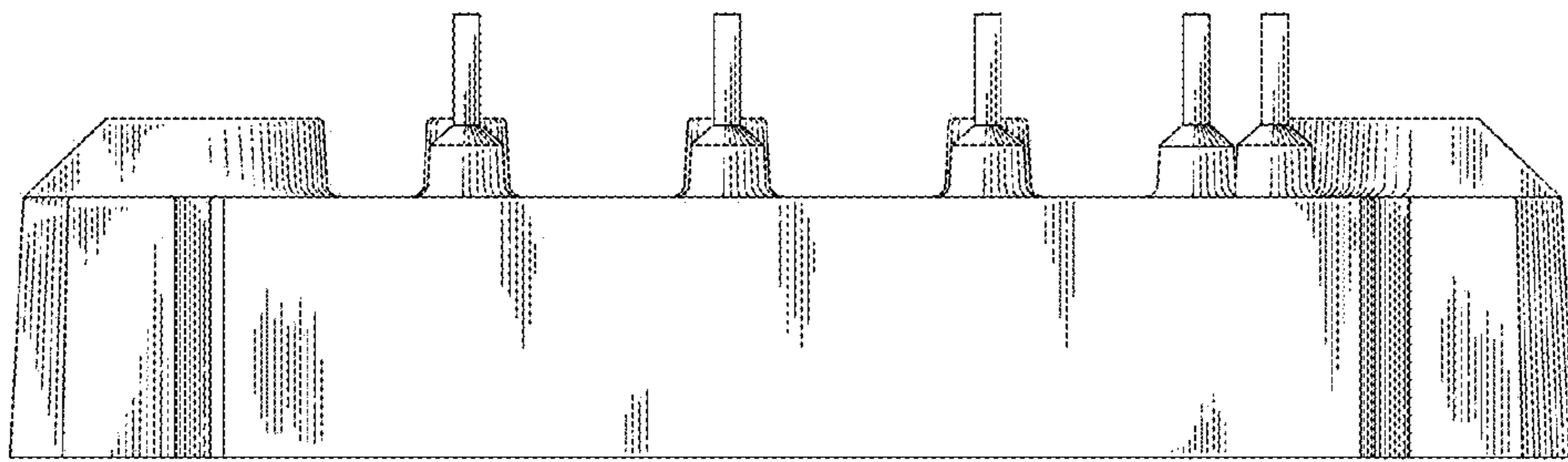


Fig. 2

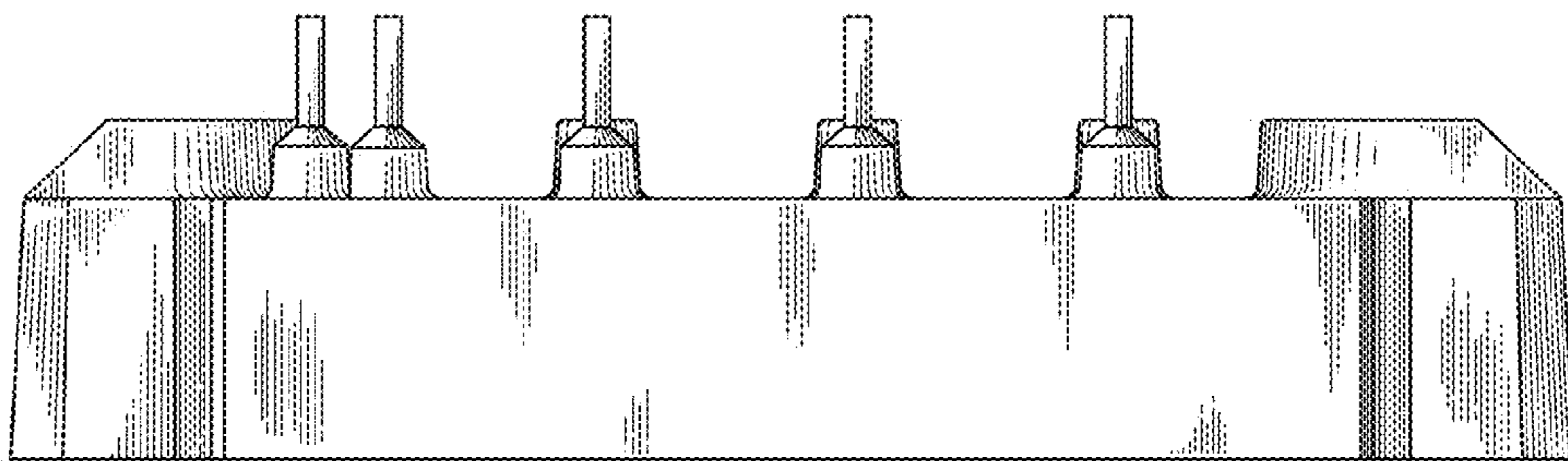


Fig. 3

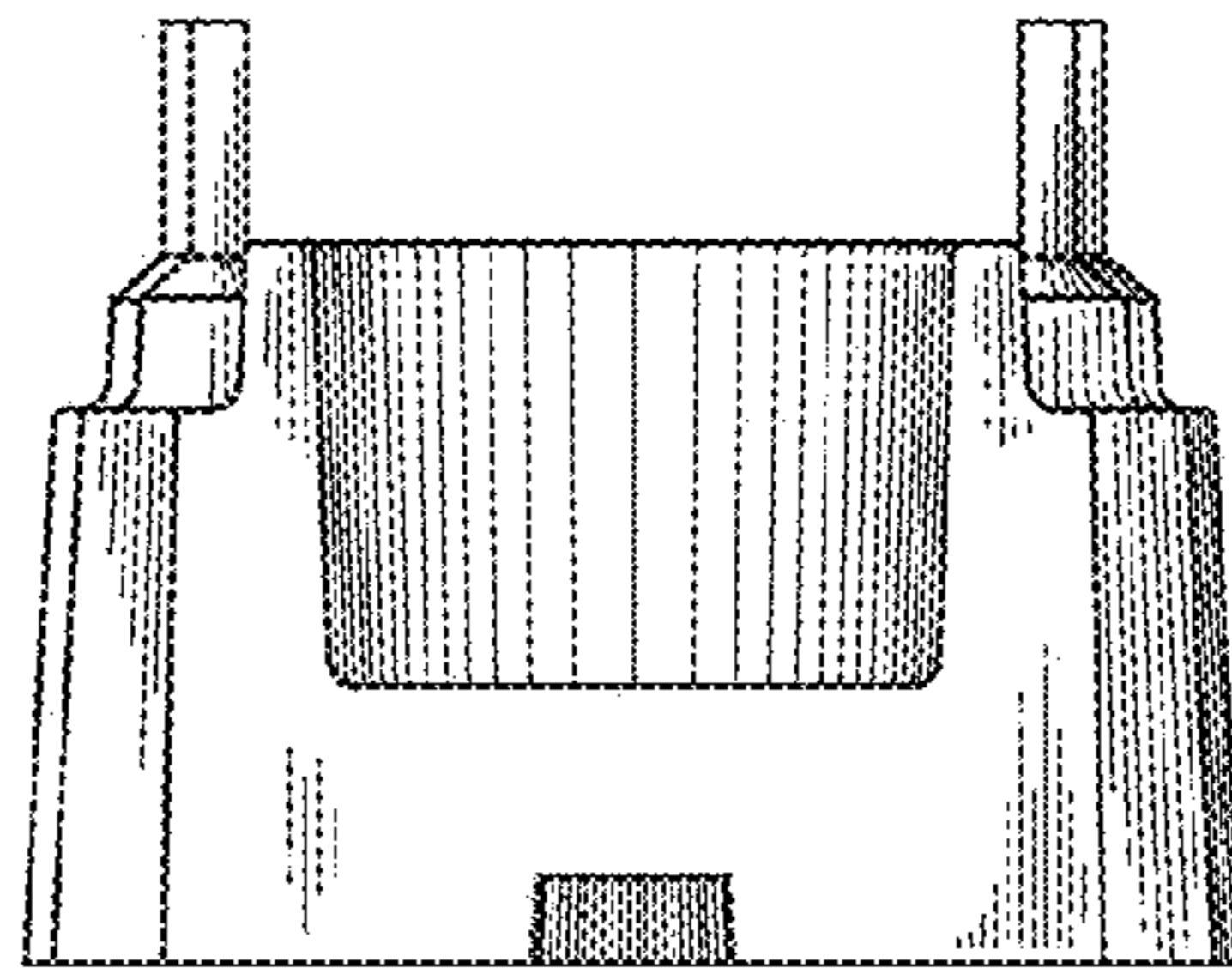


Fig. 4

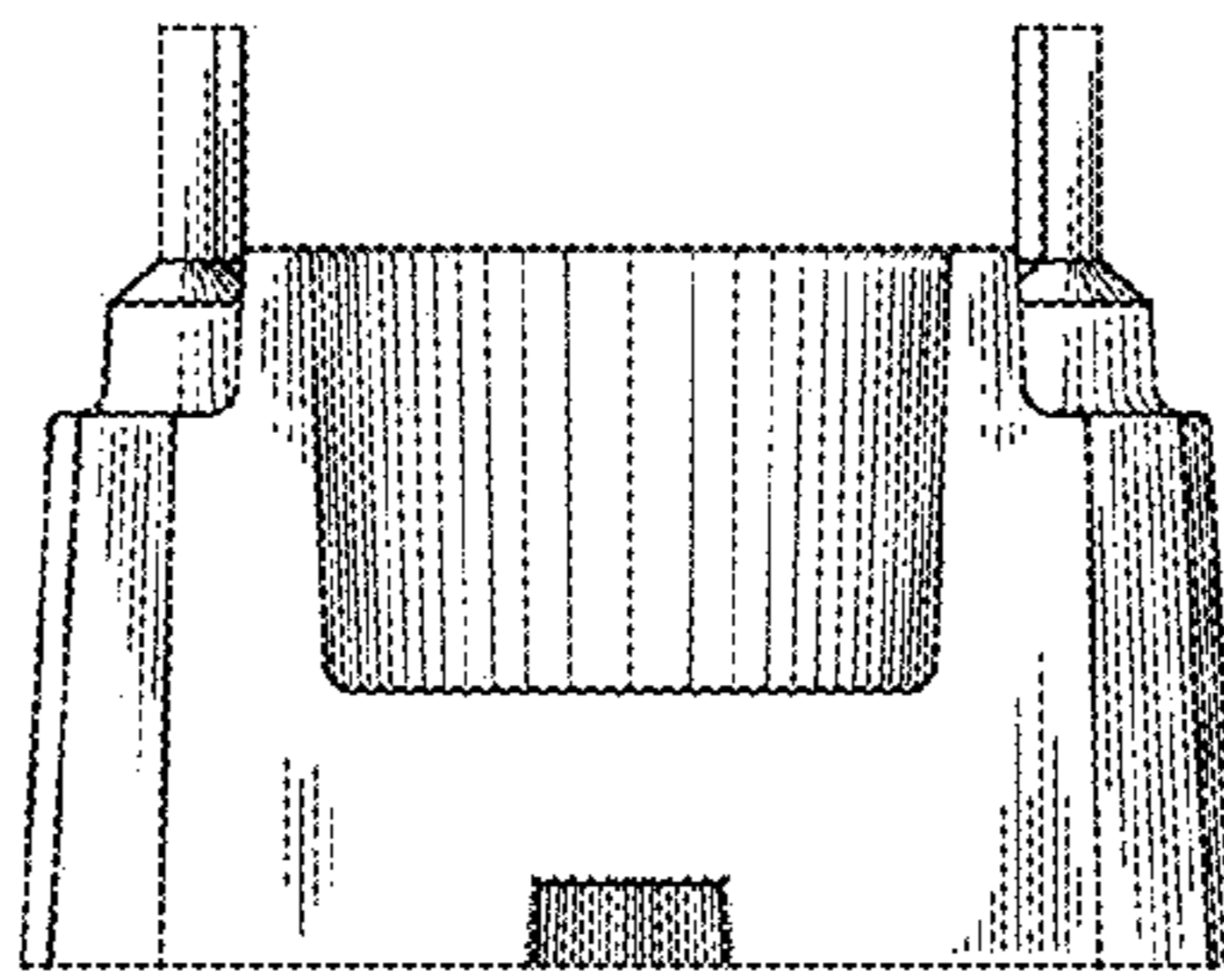


Fig.5

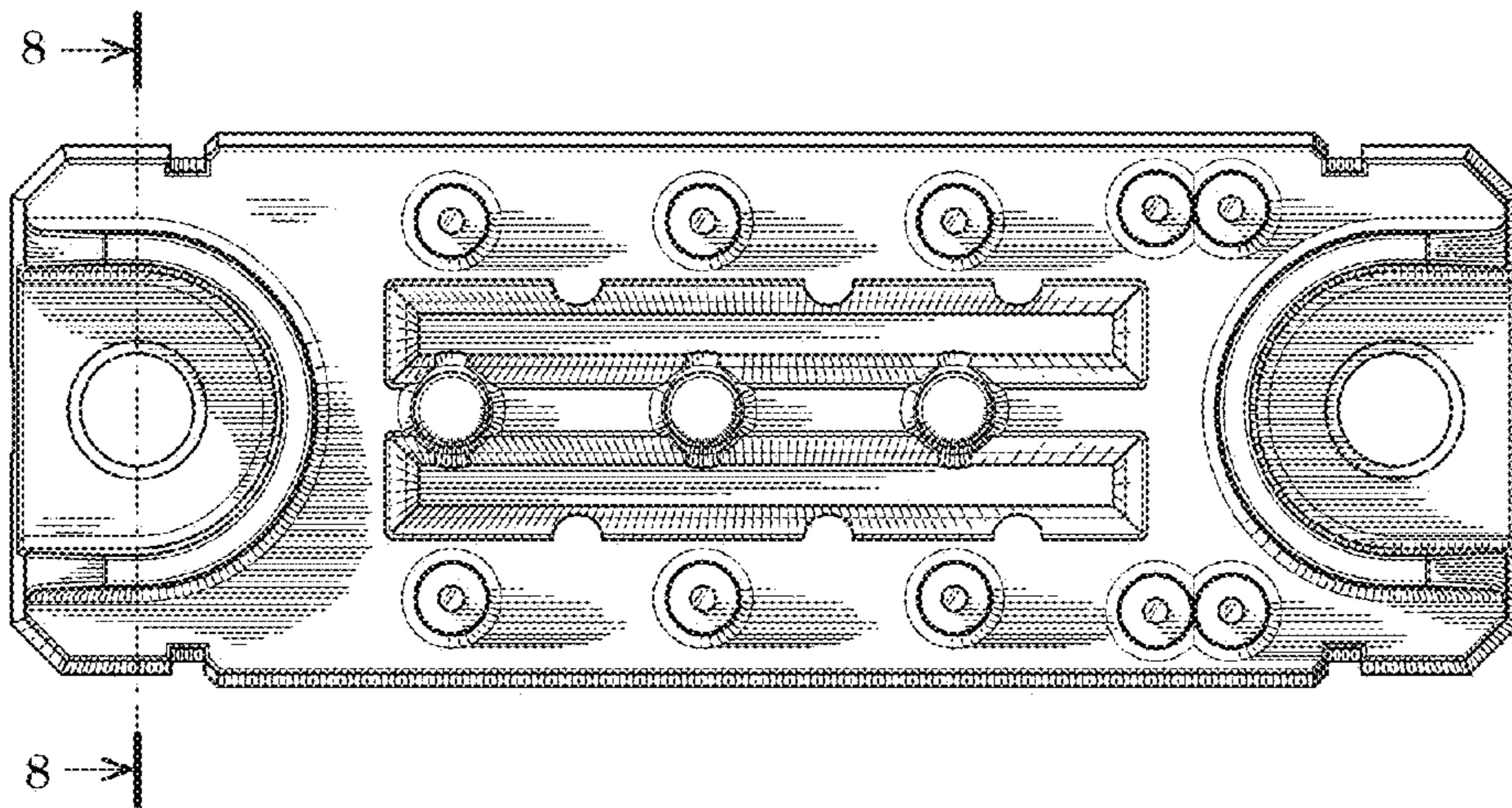


Fig. 6

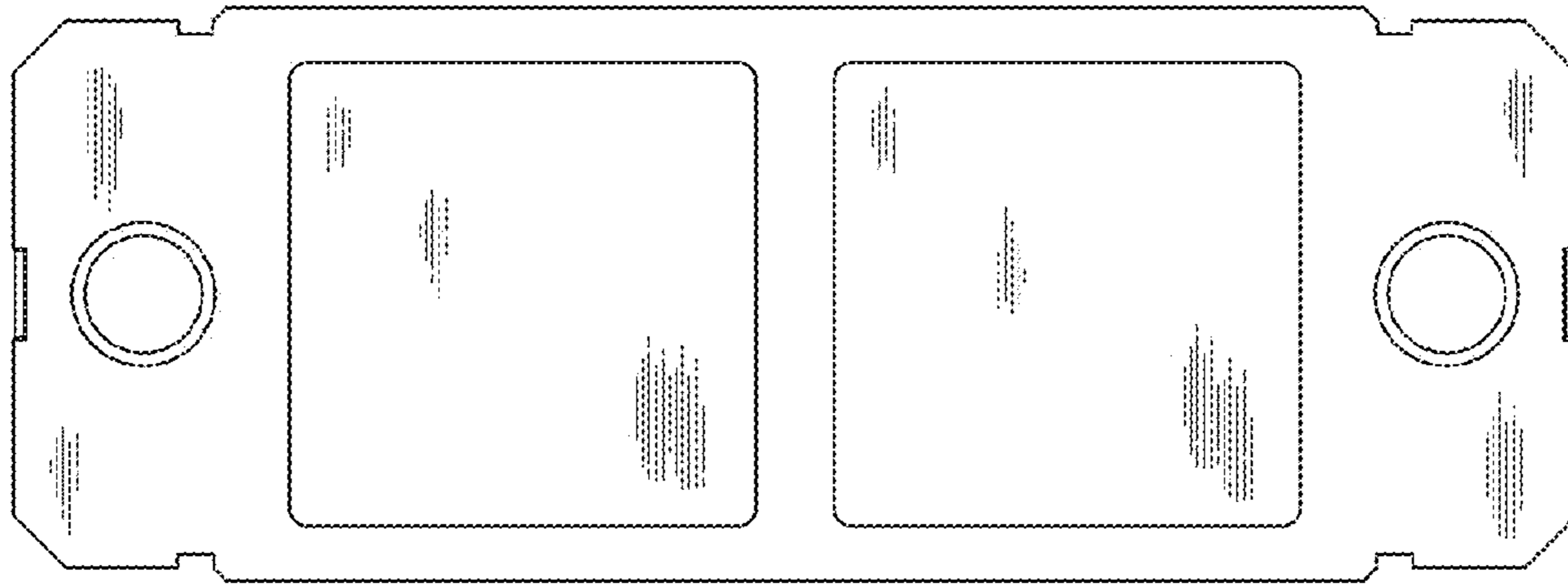




Fig. 7

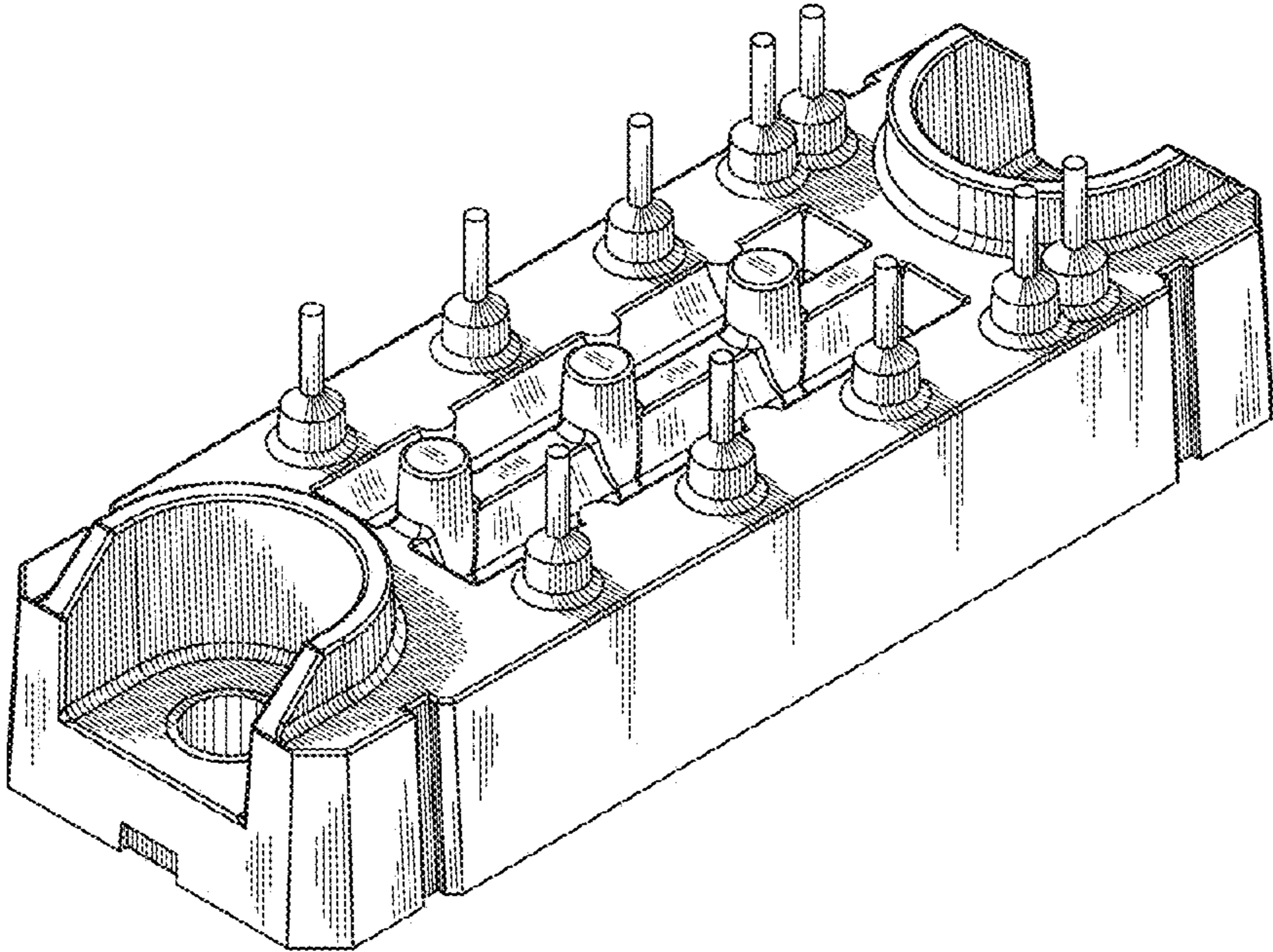


Fig.8

