



US00D721047S

(12) **United States Design Patent**
Vinciarelli et al.

(10) **Patent No.:** **US D721,047 S**
(45) **Date of Patent:** **** Jan. 13, 2015**

- (54) **SEMICONDUCTOR DEVICE**
- (71) Applicant: **VLT, Inc.**, Sunnyvale, CA (US)
- (72) Inventors: **Patrizio Vinciarelli**, Boston, MA (US);
Sergey Luzanov, Pelham, NH (US)
- (73) Assignee: **VLT, Inc.**, Sunnyvale, CA (US)
- (**) Term: **14 Years**
- (21) Appl. No.: **29/448,057**
- (22) Filed: **Mar. 8, 2013**

Related U.S. Application Data

- (63) Continuation-in-part of application No. 13/789,065, filed on Mar. 7, 2013.
- (51) **LOC (10) Cl.** **13-03**
- (52) **U.S. Cl.**
USPC **D13/182**
- (58) **Field of Classification Search**
USPC D13/110, 182; 257/668, 678, 690;
361/679.01, 713, 728, 736, 760, 761,
361/775, 820; 324/71.5, 252; 174/250, 253;
438/64, 65, 66
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,152,714	A	5/1979	Hendrickson et al.	
4,891,686	A	1/1990	Krausse, III	
D328,599	S *	8/1992	Gloton	D14/437
5,187,552	A	2/1993	Hendrickson et al.	
5,401,910	A *	3/1995	Mandai et al.	174/250
5,585,670	A *	12/1996	Isshiki et al.	257/691
D396,846	S *	8/1998	Nakayama et al.	D13/182
D396,847	S *	8/1998	Nakayama et al.	D13/182
5,844,307	A *	12/1998	Suzuki et al.	257/690
6,238,953	B1 *	5/2001	Tanaka et al.	438/112
D444,132	S *	6/2001	Iwanishi et al.	D13/182
6,353,258	B1	3/2002	Inoue et al.	
D456,367	S *	4/2002	Matteson	D13/182

D466,093	S *	11/2002	Ebihara et al.	D13/182
D473,199	S *	4/2003	Sako et al.	D13/182
D476,959	S *	7/2003	Yamada et al.	D13/182
D476,962	S *	7/2003	Yoshihira et al.	D13/182
D480,371	S *	10/2003	Sako et al.	D13/182

(Continued)

OTHER PUBLICATIONS

Efficient Power Conversion Corporation, "EPC1012—Enhancement Mode Power Transistor Datasheet". 2011, www.epc-co.com.

(Continued)

Primary Examiner — Elizabeth J Oswecki

(74) *Attorney, Agent, or Firm* — Foley & Lardner LLP

(57) **CLAIM**

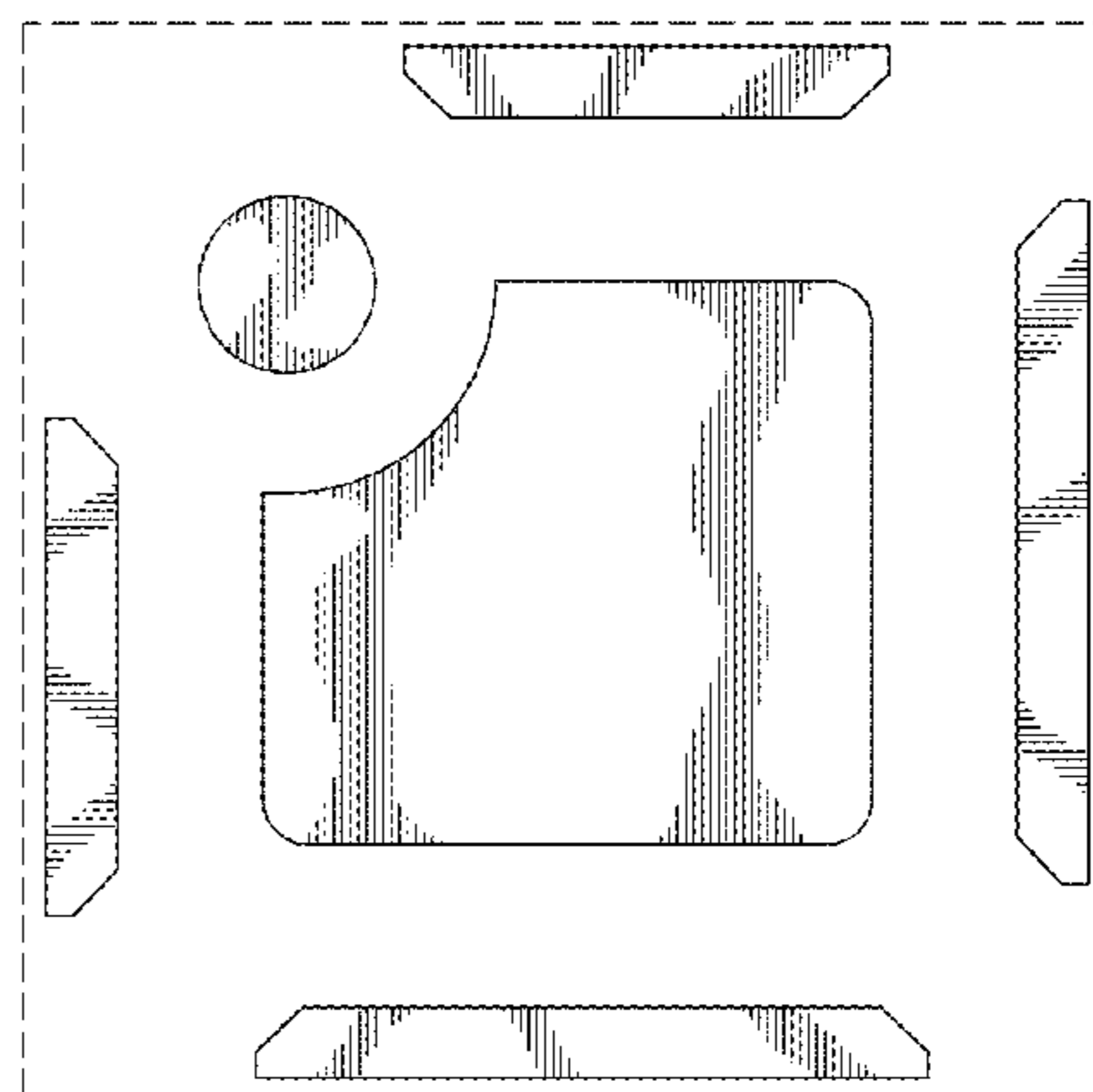
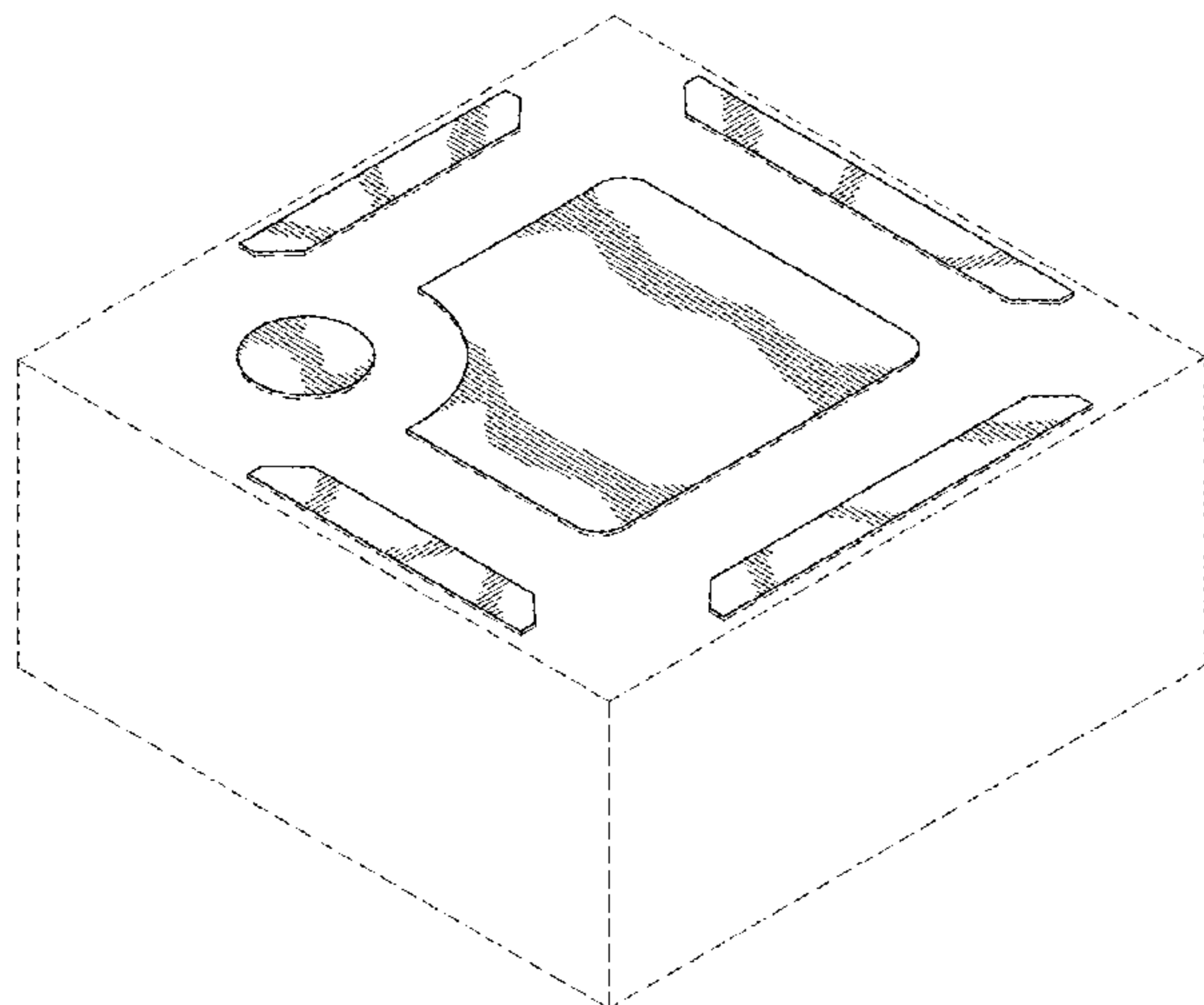
We claim the ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of a first embodiment of a semiconductor device showing our new design;
 FIG. 2 is a top plan view thereof;
 FIG. 3 is a bottom plan view thereof;
 FIG. 4 is a front elevation view thereof;
 FIG. 5 is a rear elevation view thereof;
 FIG. 6 is a right side elevation view thereof;
 FIG. 7 is a left side elevation view thereof;
 FIG. 8 is a perspective view of a second embodiment of a semiconductor device showing our new design;
 FIG. 9 is a top plan view thereof;
 FIG. 10 is a bottom plan view thereof;
 FIG. 11 is a front elevation view thereof;
 FIG. 12 is a rear elevation view thereof;
 FIG. 13 is a right side elevation view thereof; and,
 FIG. 14 is a left side elevation view thereof.

The broken lines shown in the drawings represent portions of the semiconductor device that form no part of the claimed design.

1 Claim, 10 Drawing Sheets



(56)

References Cited

U.S. PATENT DOCUMENTS

6,710,441 B2 3/2004 Eden et al.
D489,338 S * 5/2004 Seddon et al. D13/182
D504,874 S * 5/2005 Celaya et al. D13/182
6,891,223 B2 5/2005 Krumrey et al.
D510,728 S * 10/2005 Celaya et al. D13/182
6,969,909 B2 11/2005 Briere
7,038,917 B2 5/2006 Vinciarelli et al.
7,166,898 B2 1/2007 Briere
8,021,918 B2 9/2011 Lin et al.
RE44,372 E 7/2013 Vinciarelli et al.
D699,201 S * 2/2014 Petsch D13/182

D701,843 S * 4/2014 Masuda D13/182
2004/0004272 A1 1/2004 Luo et al.
2010/0096756 A1 4/2010 Tagami et al.
2012/0299069 A1 11/2012 Kuhn et al.

OTHER PUBLICATIONS

Product Information, ST Dual N-Channel 30 V, Ω typ., 11 a
STripFET™ V Power MOSFET in a PowerFLAT™ 5x6 double
island, Doc ID 18416 Rev 3, Dec. 2012, www.st.com (14 pages).
Notice of Allowance mailed Oct. 31, 2014 in co-pending US Appl.
No. 13/789,065 (18 pgs.).

* cited by examiner

Fig. 1

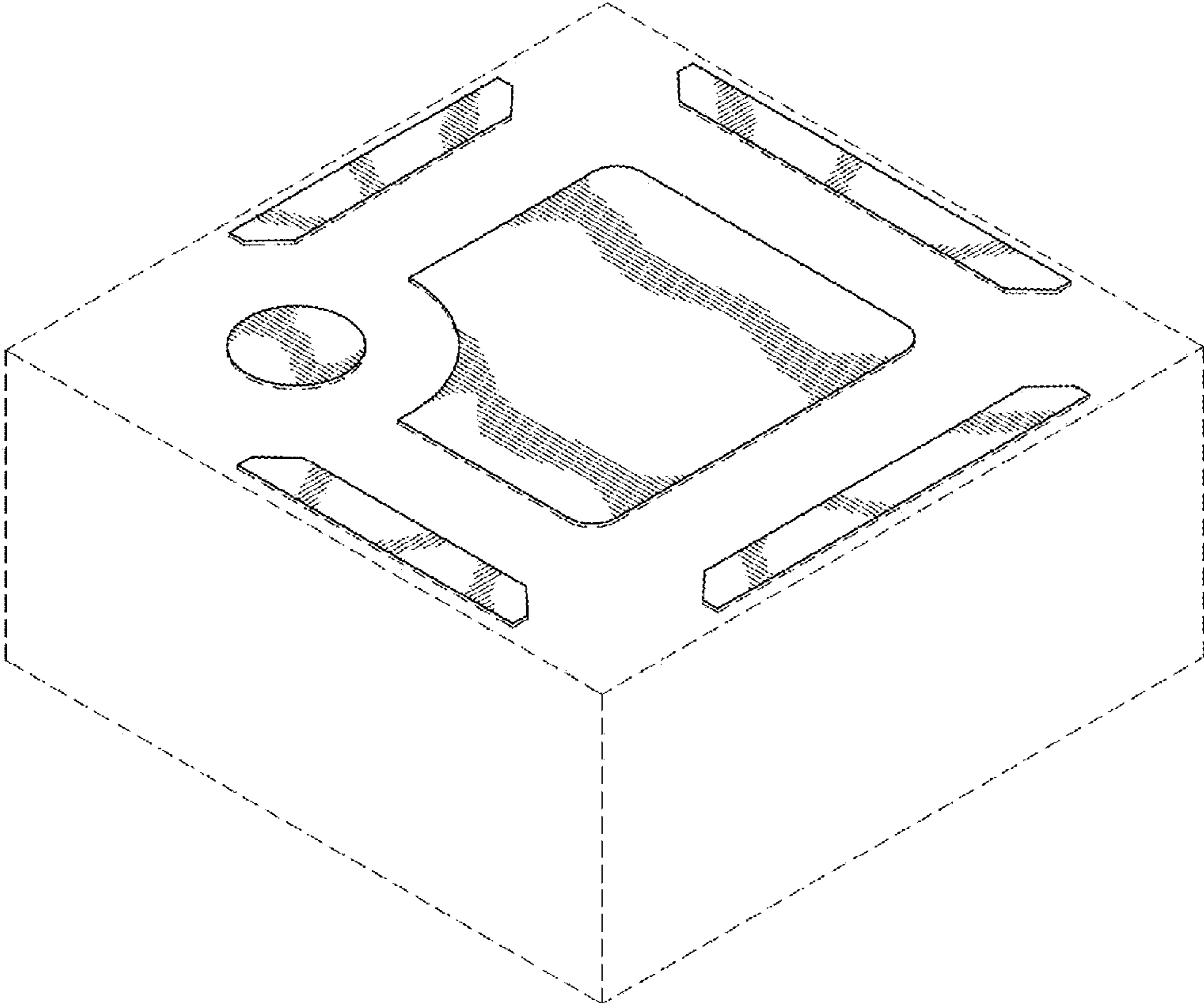


Fig. 2

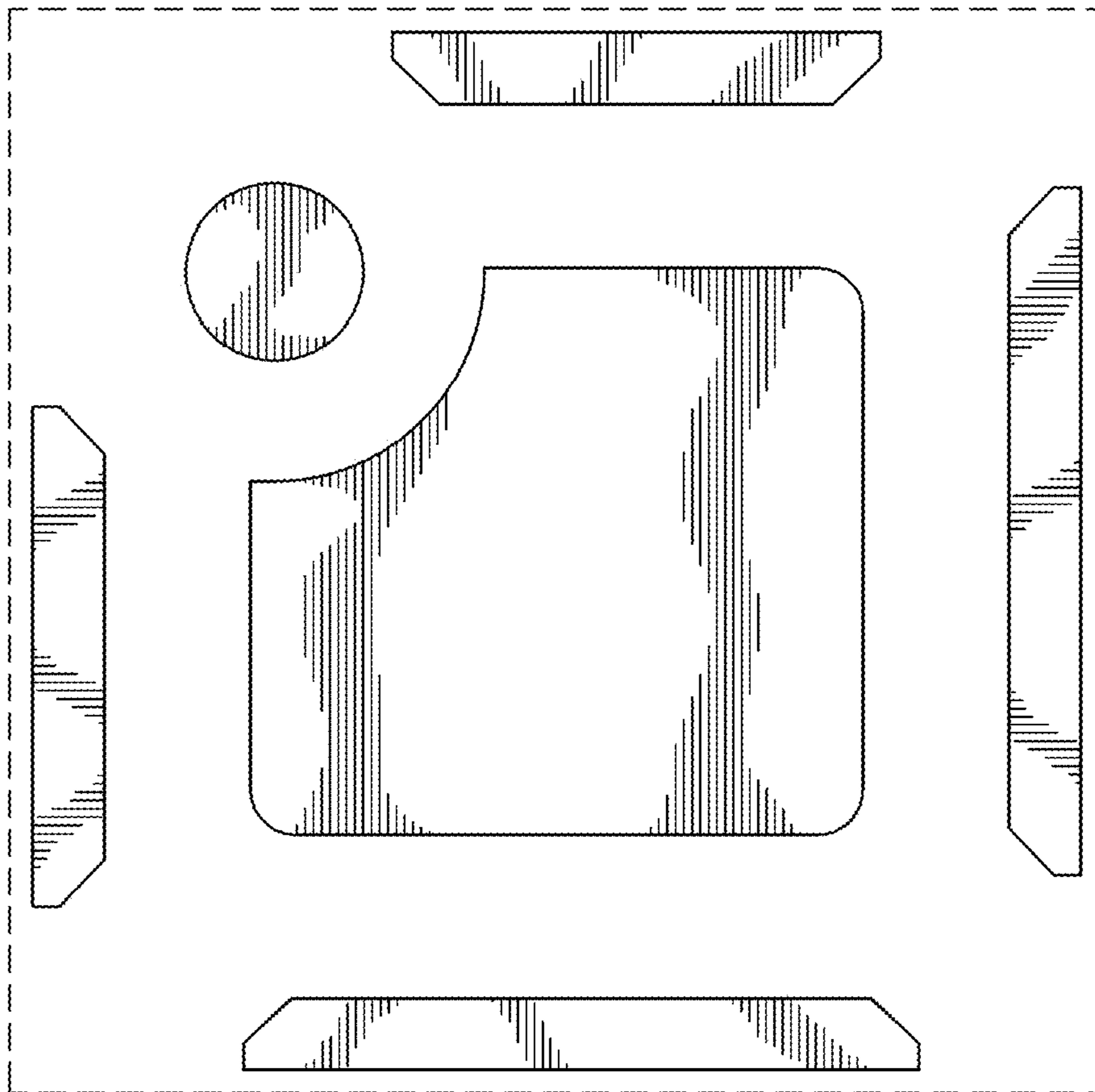


Fig. 3



Fig. 4



Fig. 5



Fig. 6



Fig. 7

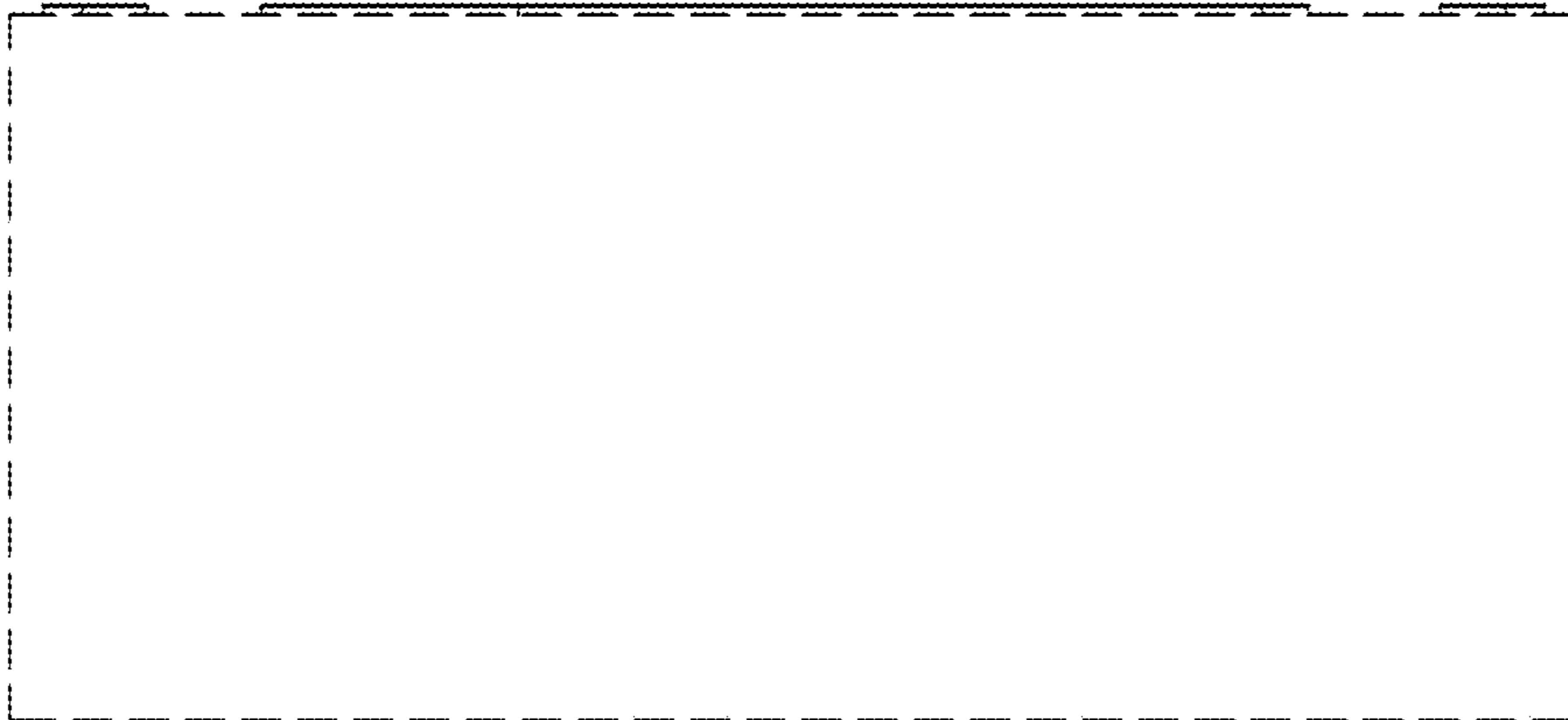


Fig. 8

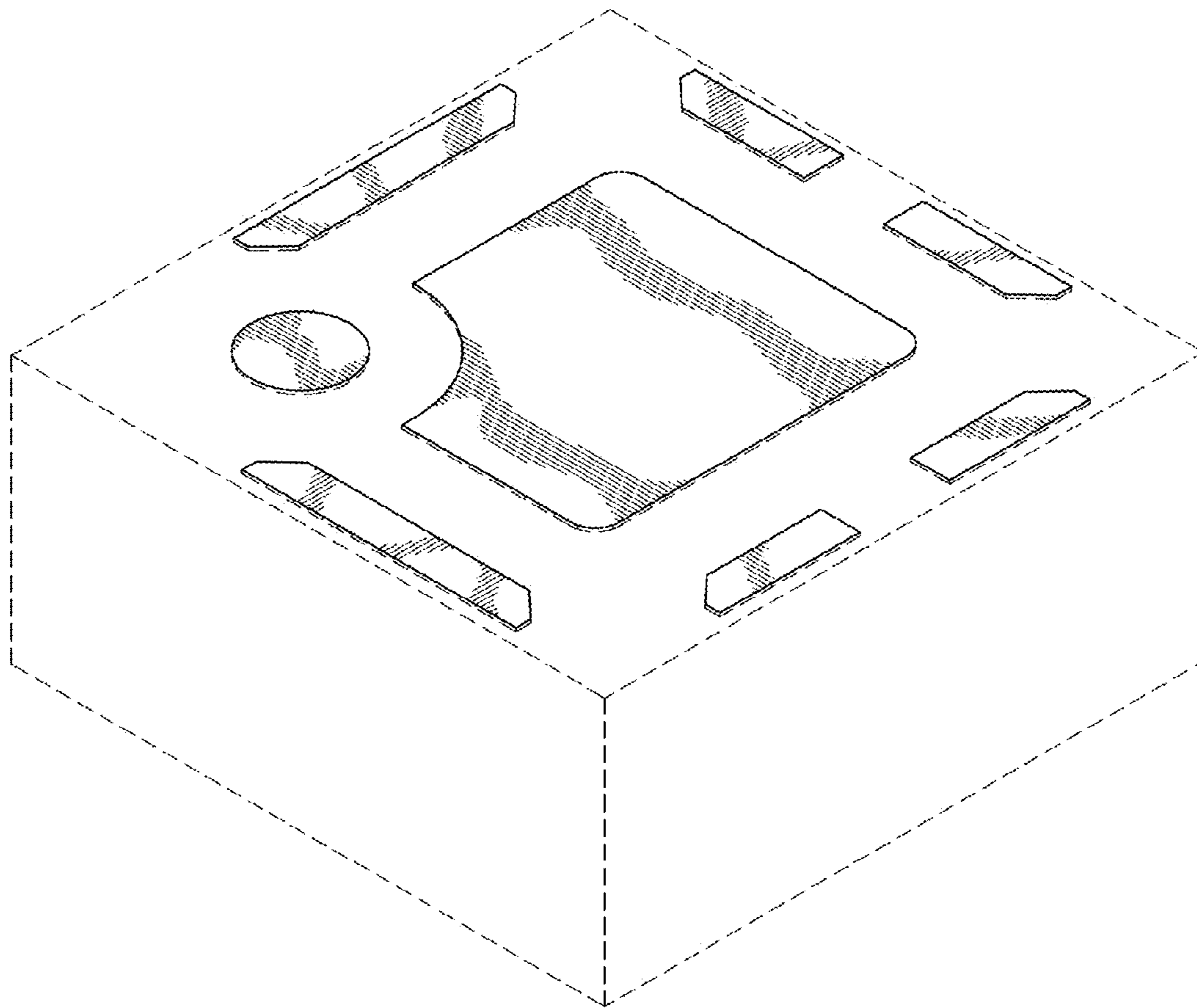


Fig. 9

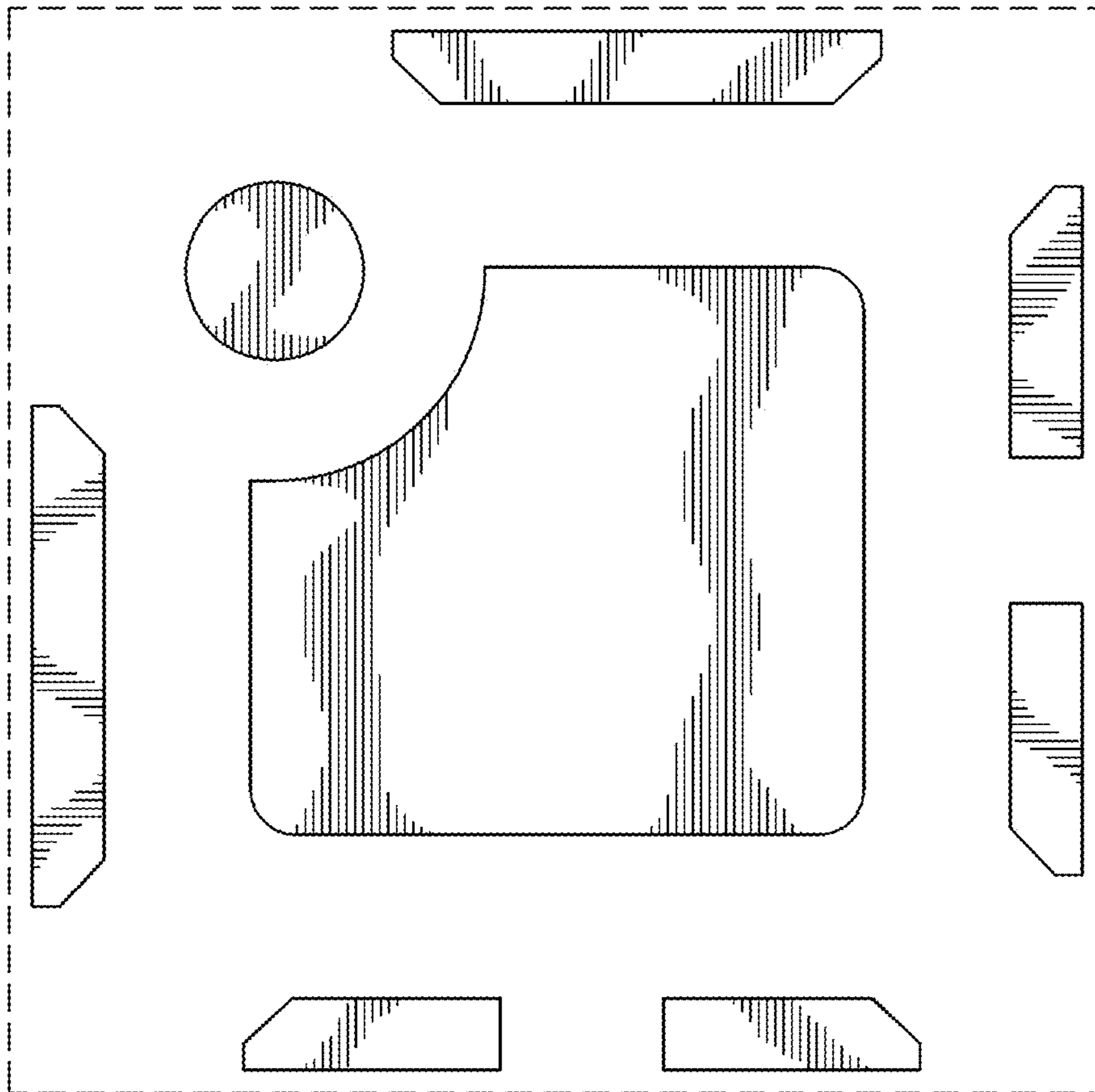


Fig. 10

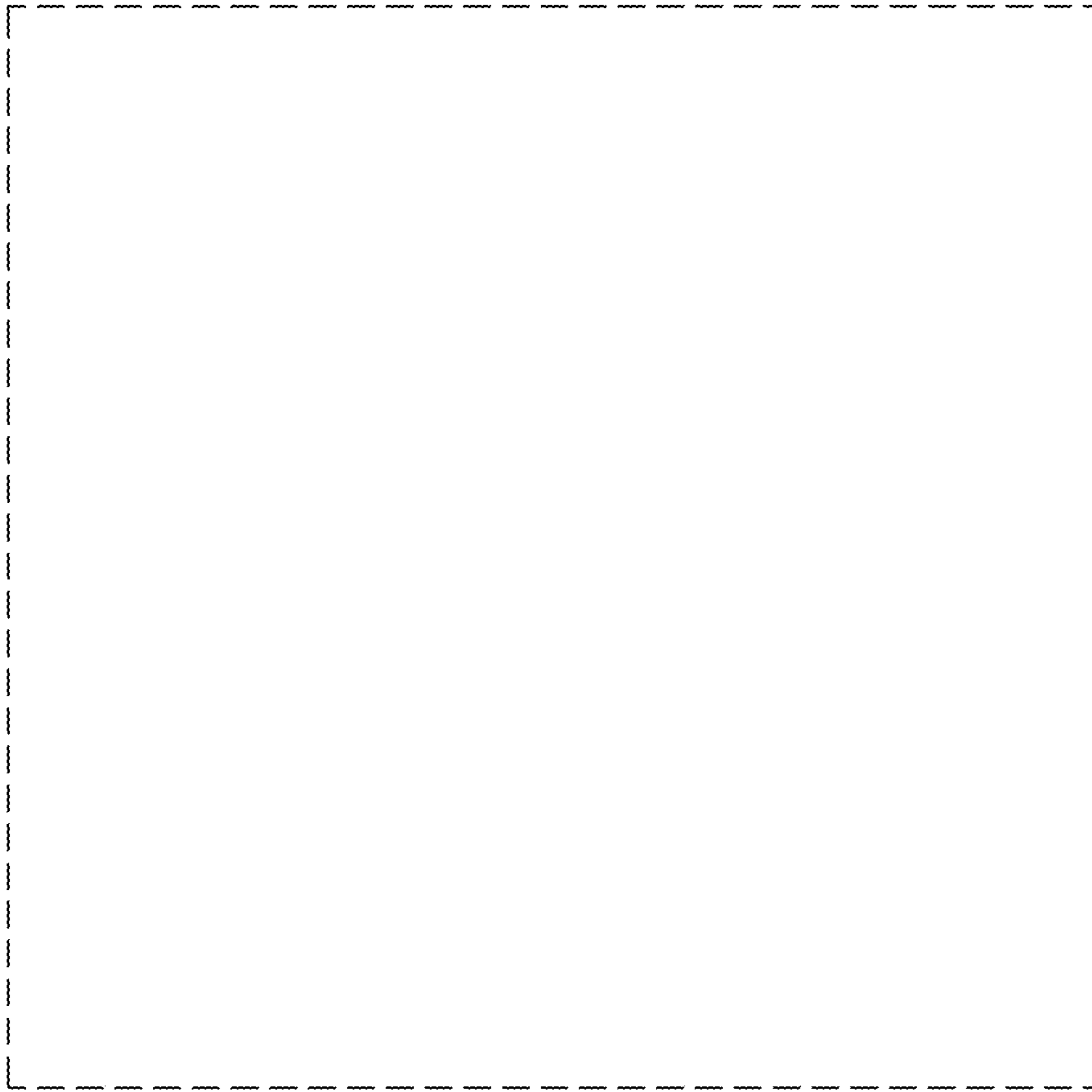


Fig. 11



Fig. 12



Fig. 13

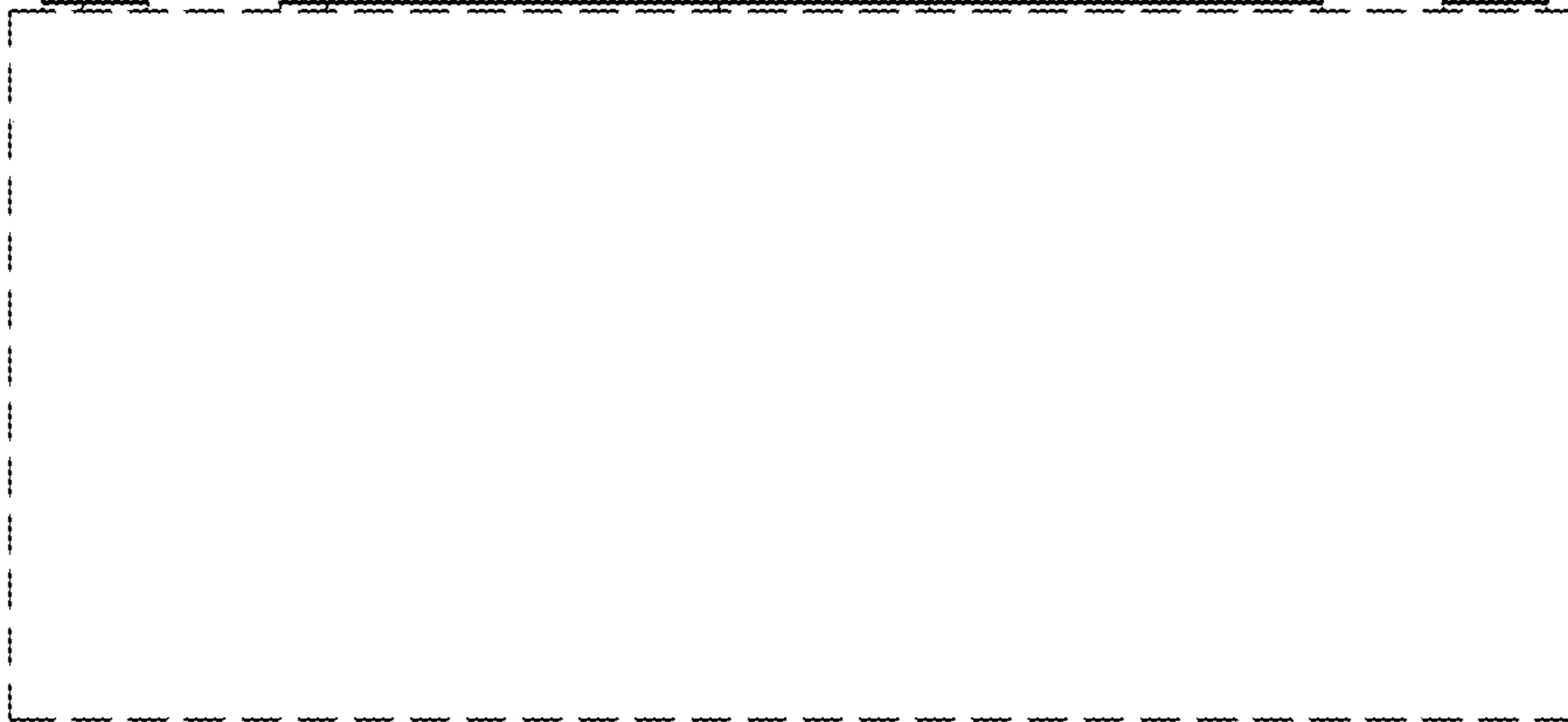


Fig. 14

