



US00D720309S

(12) **United States Design Patent**
Kaneko et al.

(10) **Patent No.:** **US D720,309 S**

(45) **Date of Patent:** **** Dec. 30, 2014**

(54) **INNER TUBE FOR PROCESS TUBE FOR
MANUFACTURING SEMICONDUCTOR
WAFERS**

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(JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/420,537**

(22) Filed: **May 10, 2012**

(30) **Foreign Application Priority Data**

Nov. 18, 2011 (JP) 2011-026686

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182; D23/266; D7/600.1, 600.2;
118/715, 722, 724, 725; 219/385, 390,
219/486, 520, 523; 83/35, 39; 138/118,
138/118.1, 121, 177, 178; 206/454, 711;
211/41.18; 414/935; 432/247, 253
See application file for complete search history.

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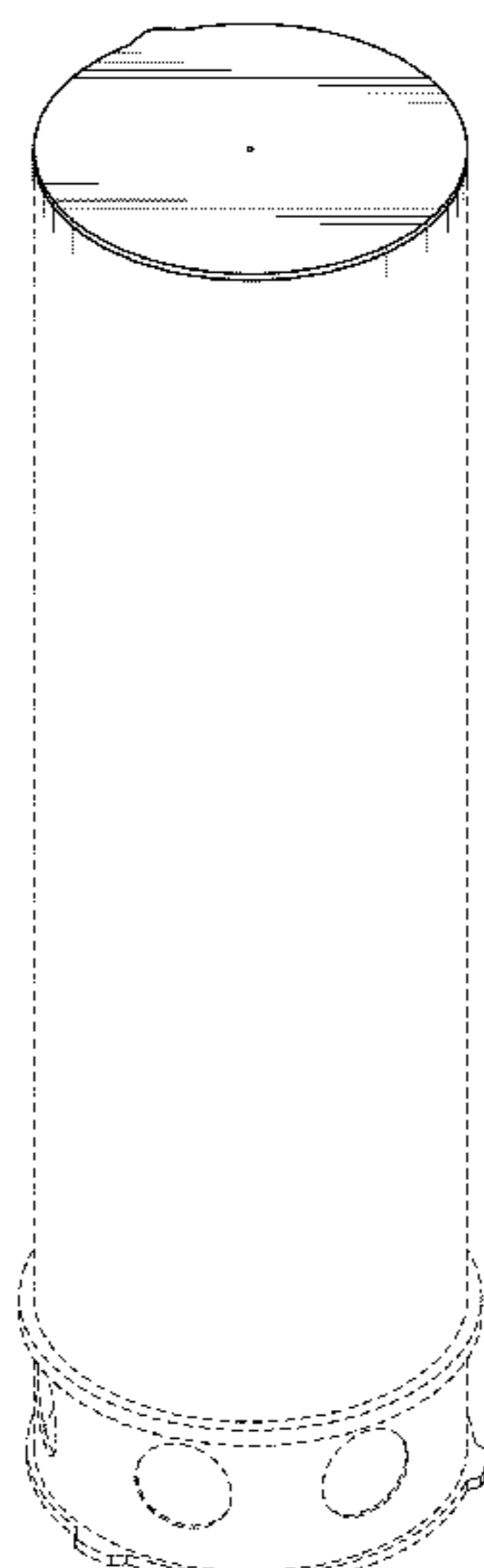
(57) **CLAIM**

The ornamental design for an inner tube for process tube for manufacturing semiconductor wafers, as shown and described.

DESCRIPTION

FIG. 1 is perspective view of an inner tube for process tube for manufacturing semiconductor wafers showing our new design;
FIG. 2 is a front view thereof;
FIG. 3 is a rear view thereof;
FIG. 4 is a right side thereof;
FIG. 5 is a left side view thereof;
FIG. 6 is a top plan view thereof;
FIG. 7 is a bottom plan view thereof;
FIG. 8 is a cross-sectional view taken along line 8-8 of FIG. 6;
FIG. 9 is an enlarged view of portion 9 encircled in FIG. 8;
FIG. 10 is another front view thereof, shown in a used condition; and,
FIG. 11 is an enlarged view of portion 11 encircled in FIG. 5.
The broken lines shown in the drawings represent portions of the inner tube for process tube for manufacturing semiconductor wafers that form no part of the claimed design.

1 Claim, 10 Drawing Sheets



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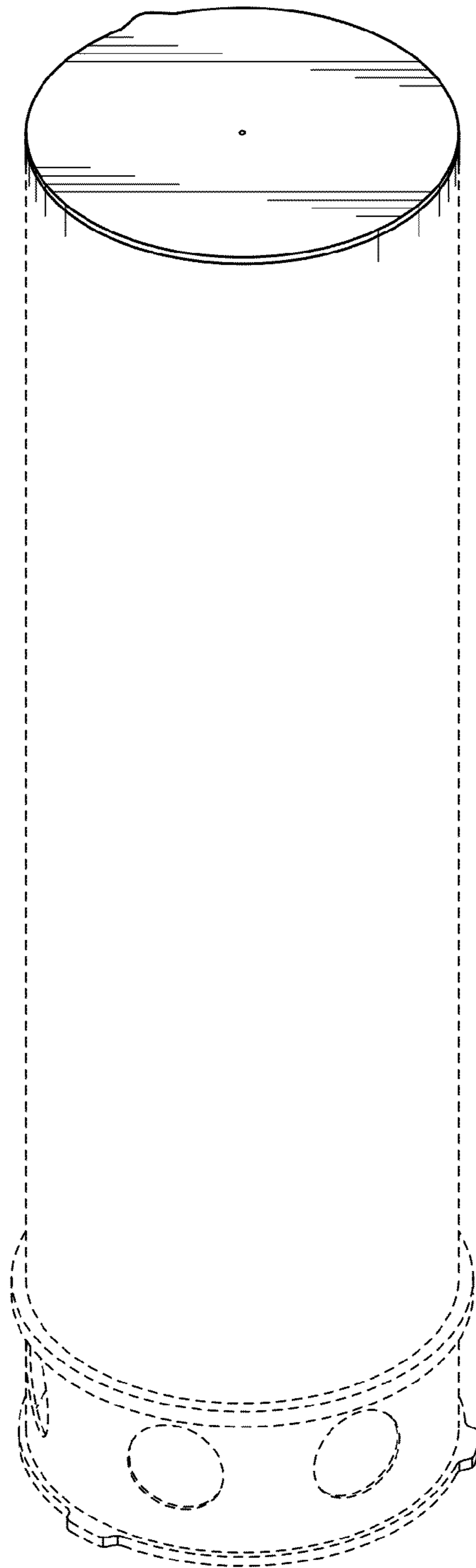


FIG. 1

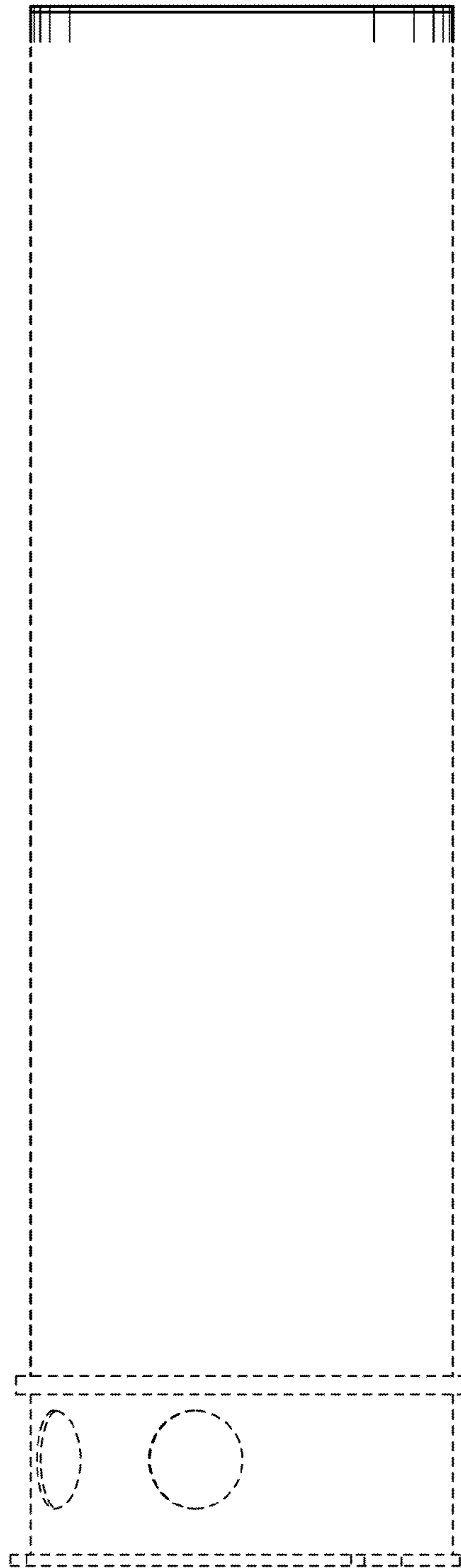


FIG. 2

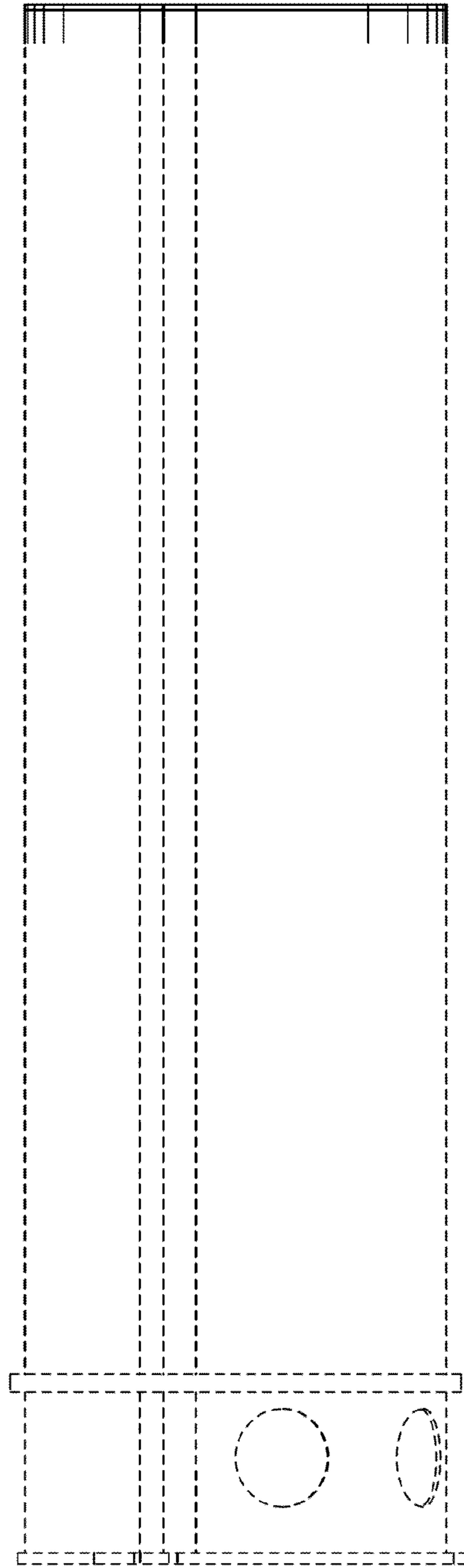


FIG. 3

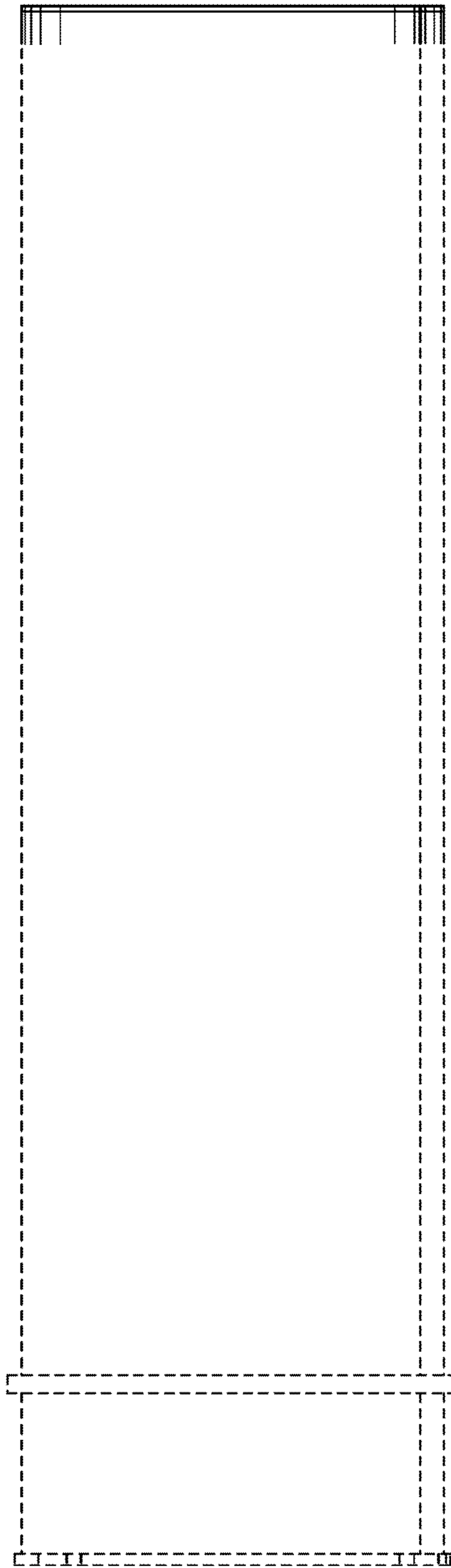


FIG. 4

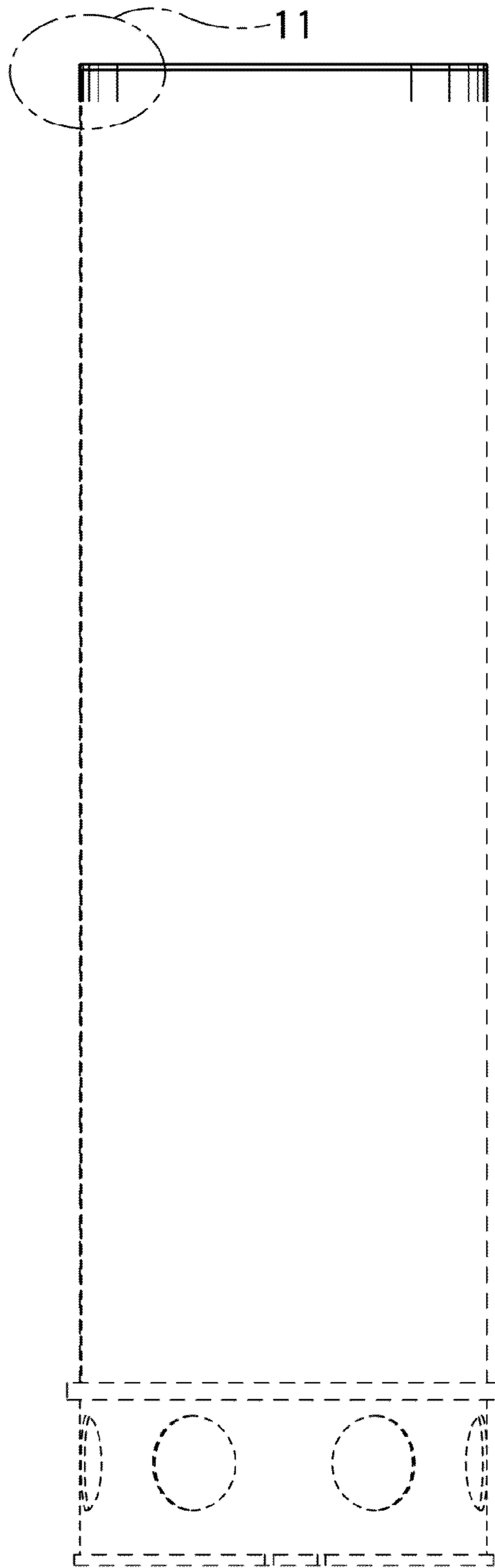


FIG. 5

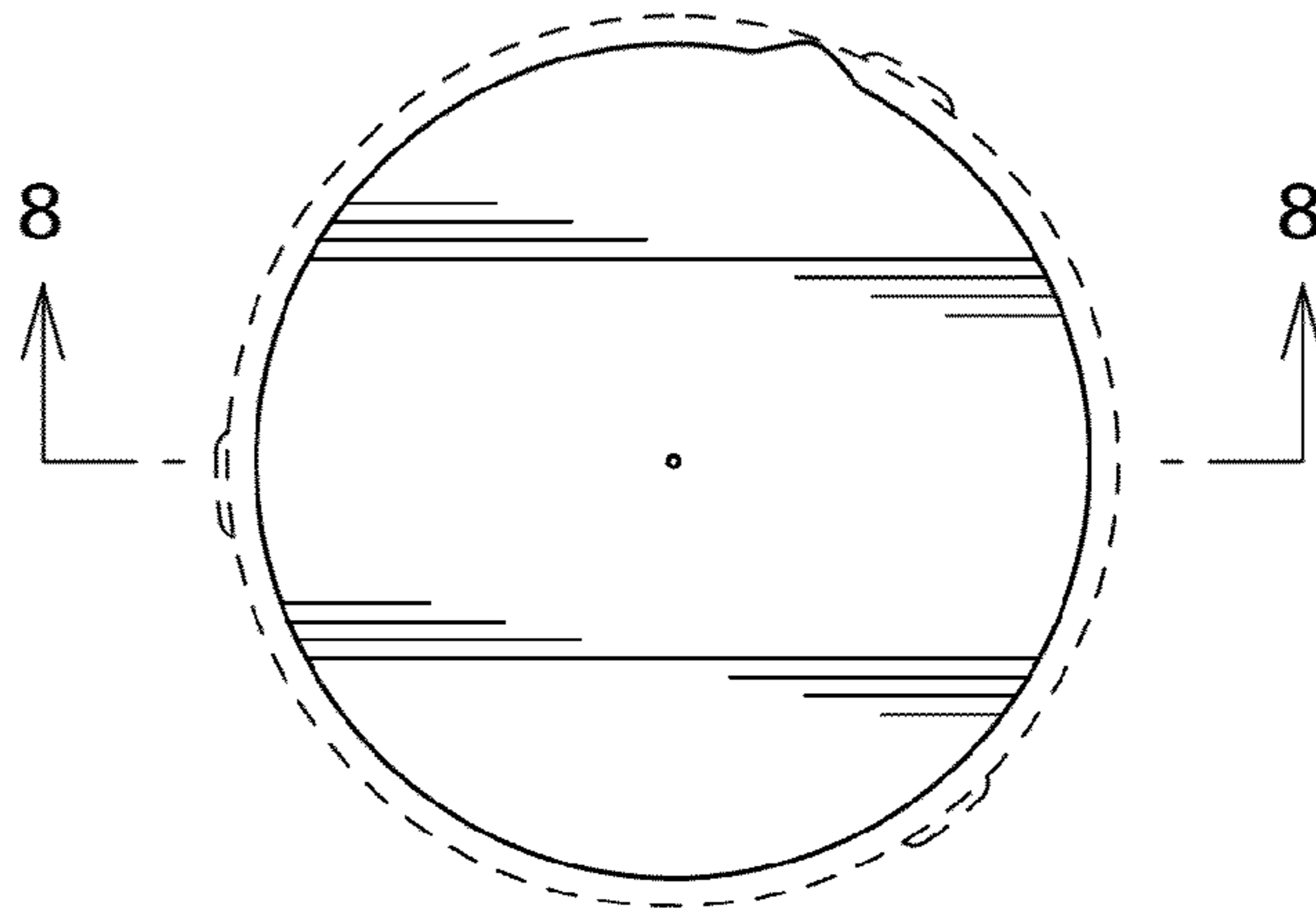


FIG. 6

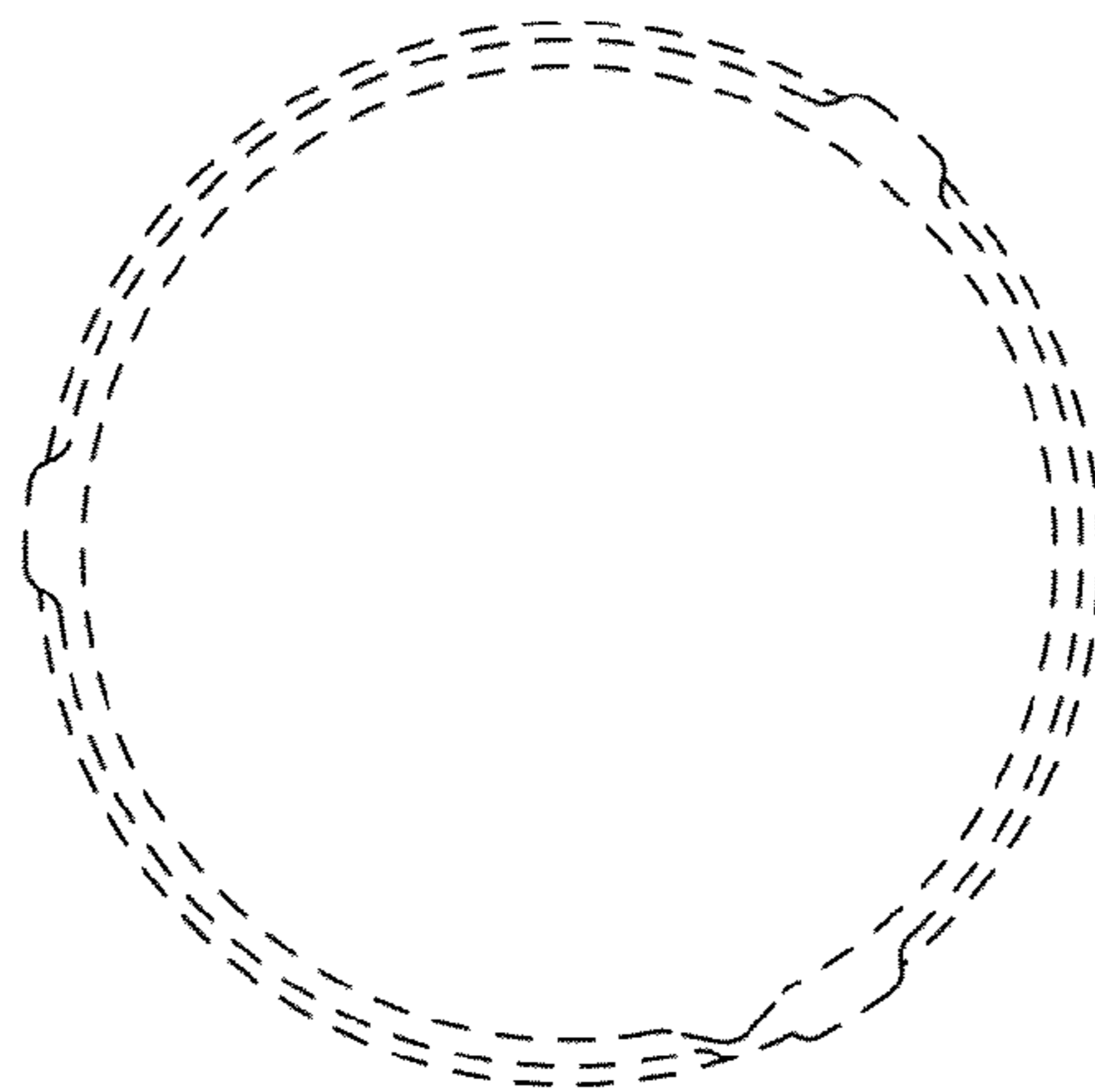


FIG. 7

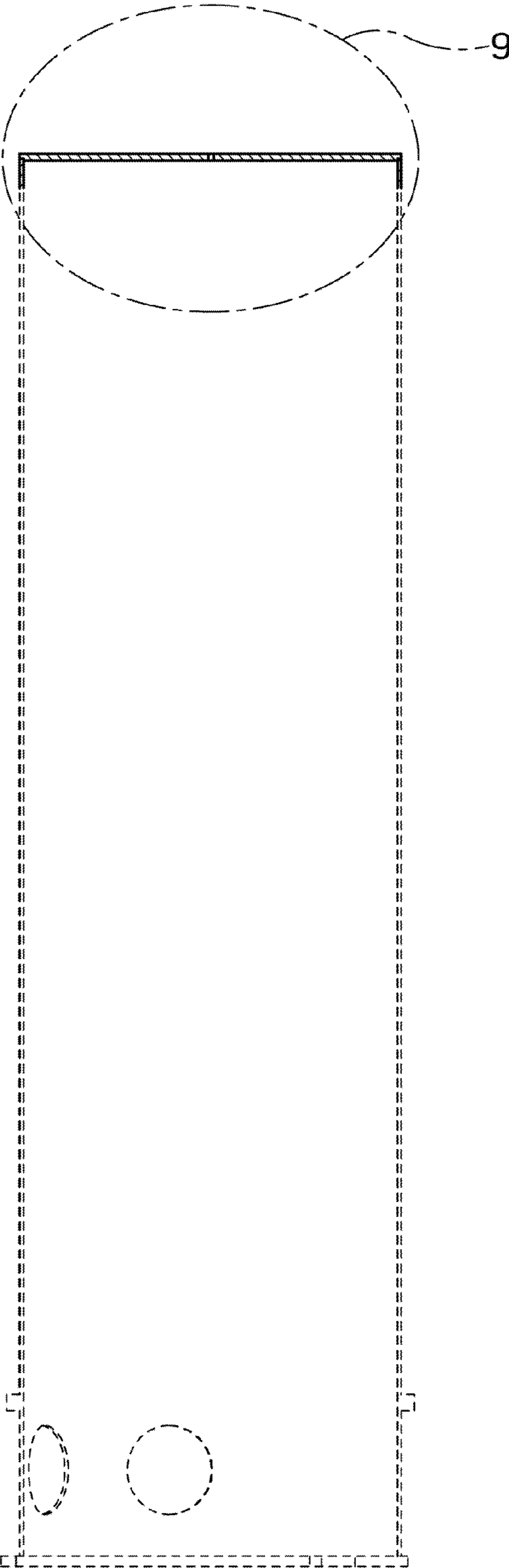


FIG. 8

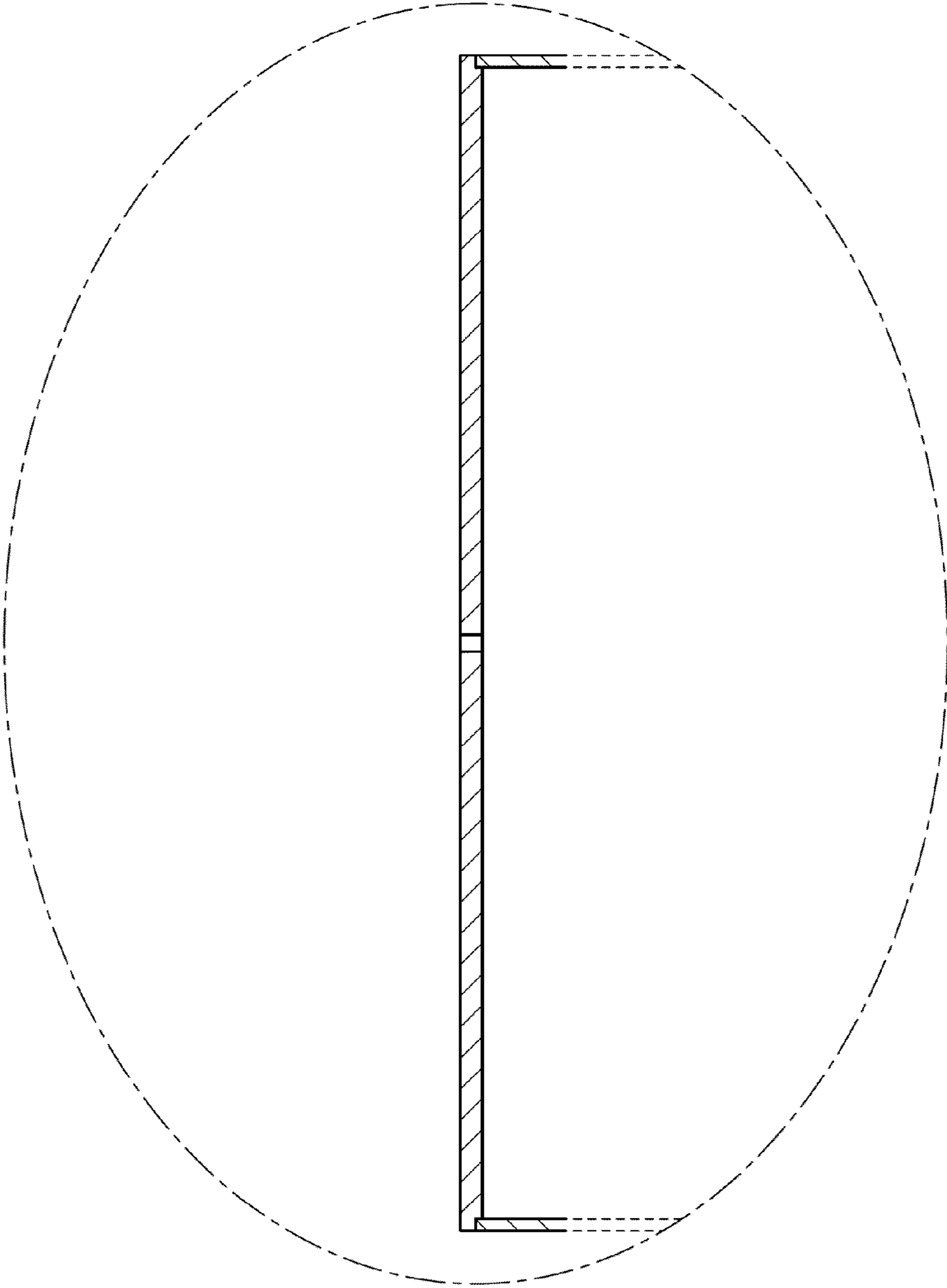


FIG. 9

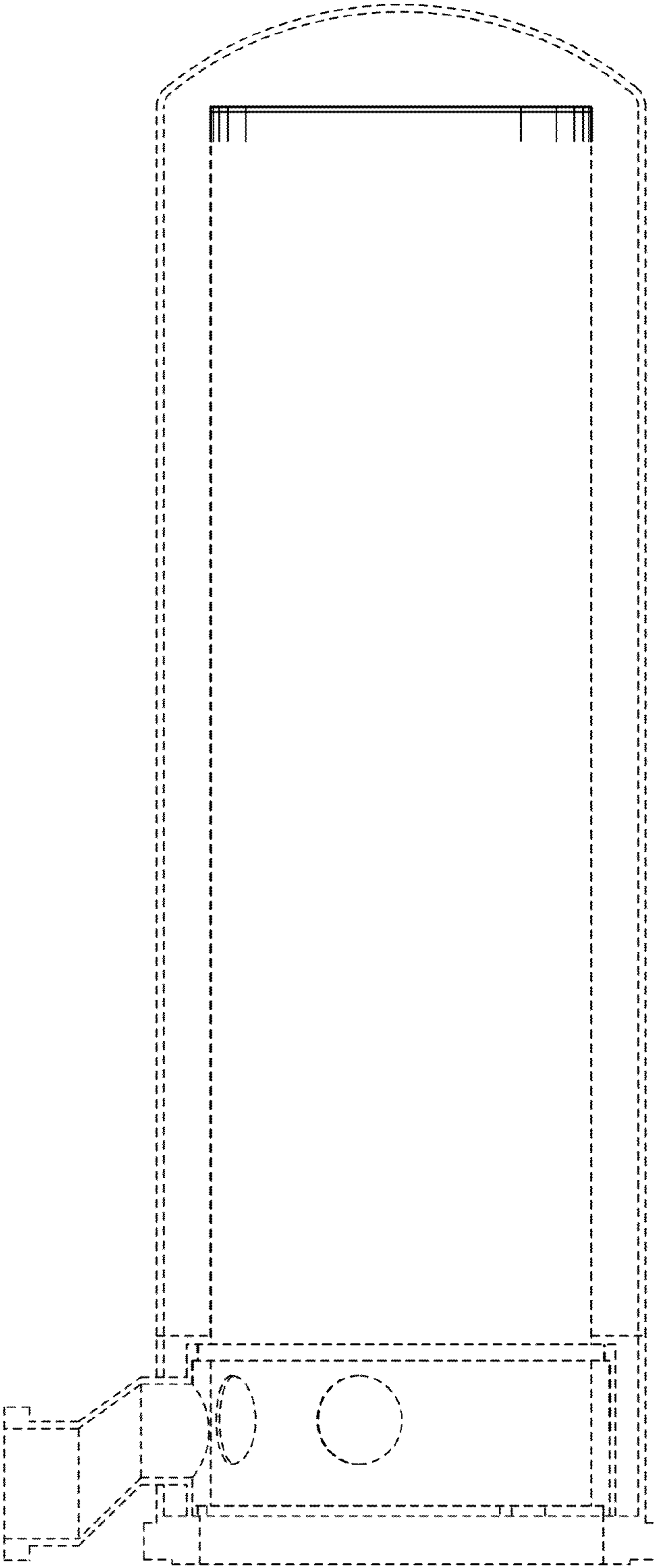


FIG. 10

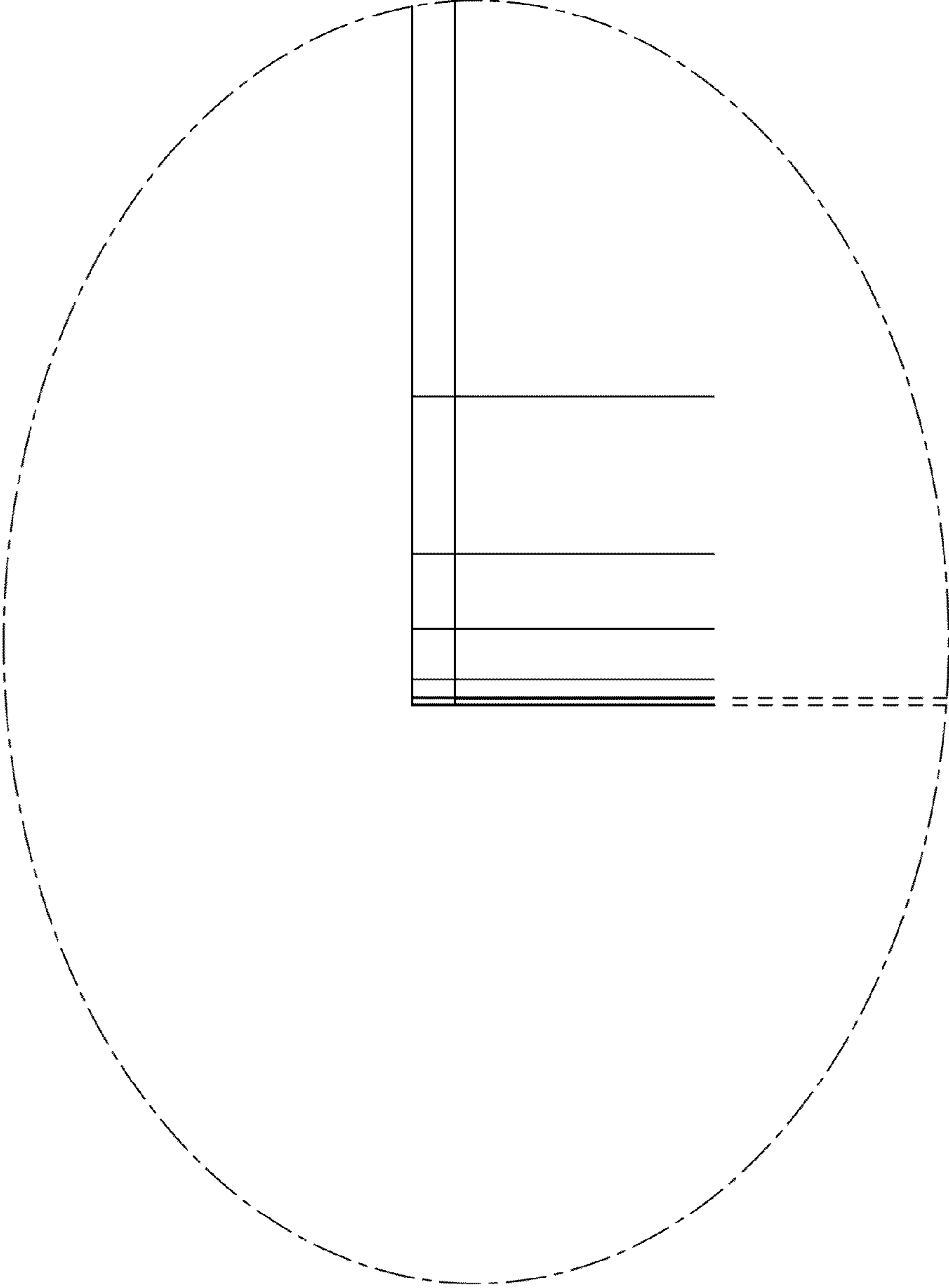


FIG. 11