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Kawase et al.

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(54) **SEMICONDUCTOR DEVICE**

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(**) Term: **14 Years**

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May 8, 2013	(JP)	2013-010101
May 8, 2013	(JP)	2013-010102
May 8, 2013	(JP)	2013-010103
May 8, 2013	(JP)	2013-010104

(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/110, 182, 184; 361/713, 728, 736, 361/760, 761, 775, 679.01, 820; 257/666, 257/668, 678, 690; 324/71.5, 252; 174/250, 174/253; 438/64, 65, 66
See application file for complete search history.

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(74) *Attorney, Agent, or Firm* — Sughrue Mion, PLLC; Richard C. Turner

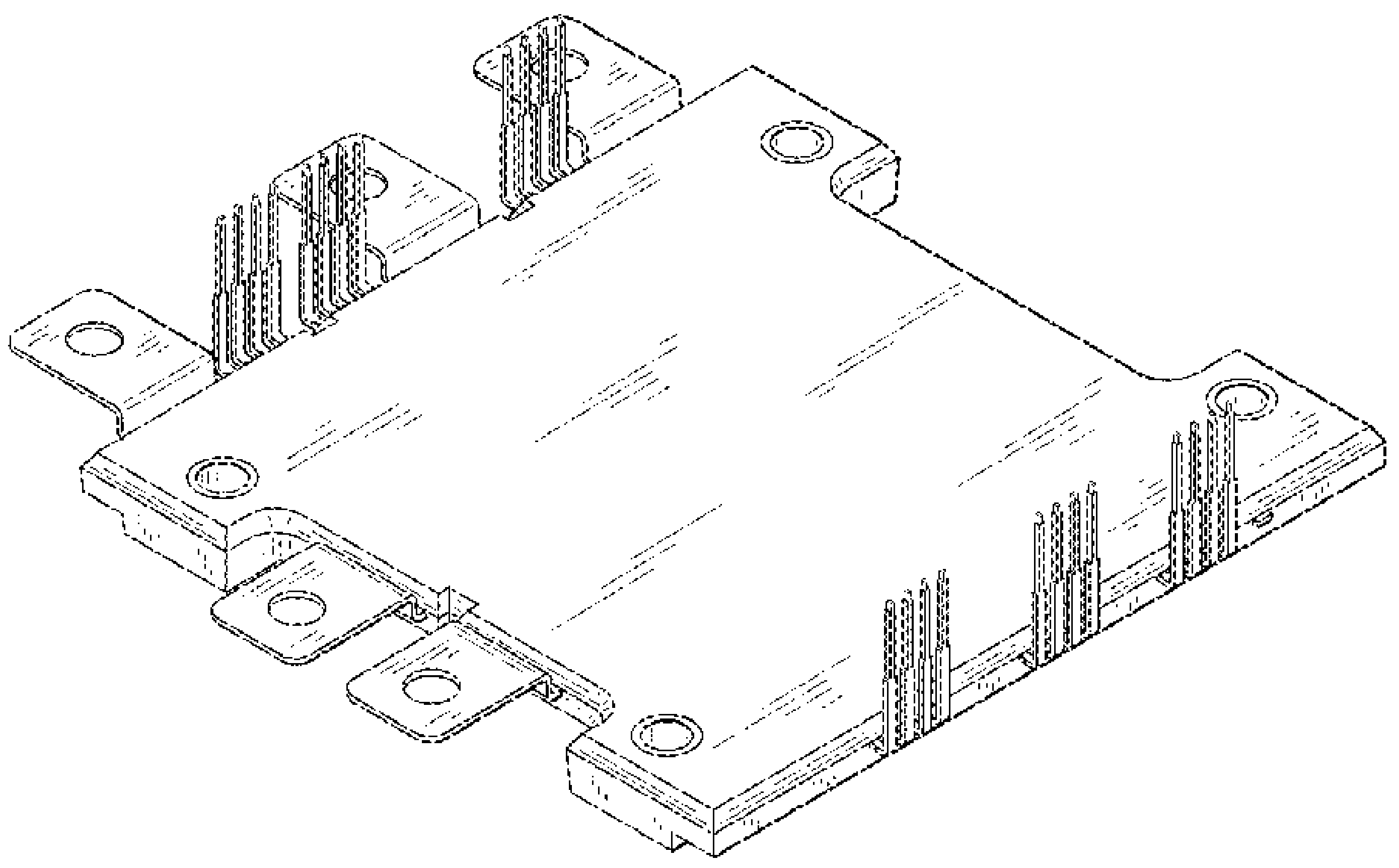
(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. **1** is a front, top and right side perspective view of a semiconductor device, showing our new design;
FIG. **2** is a rear, top and left side perspective view thereof;
FIG. **3** is a front elevational view thereof;
FIG. **4** is a rear elevational view thereof;
FIG. **5** is a left side elevational view thereof;
FIG. **6** is a right side elevational view thereof;
FIG. **7** is a top plan view thereof;
FIG. **8** is a bottom plan view thereof;
FIG. **9** is a perspective view shown in a used condition with a device shown in broken lines; and,
FIG. **10** is a front view shown in a used condition with a device shown in broken lines.
The broken lines shown in the drawings represent portions of the semiconductor device that form no part of the claimed design.

1 Claim, 8 Drawing Sheets



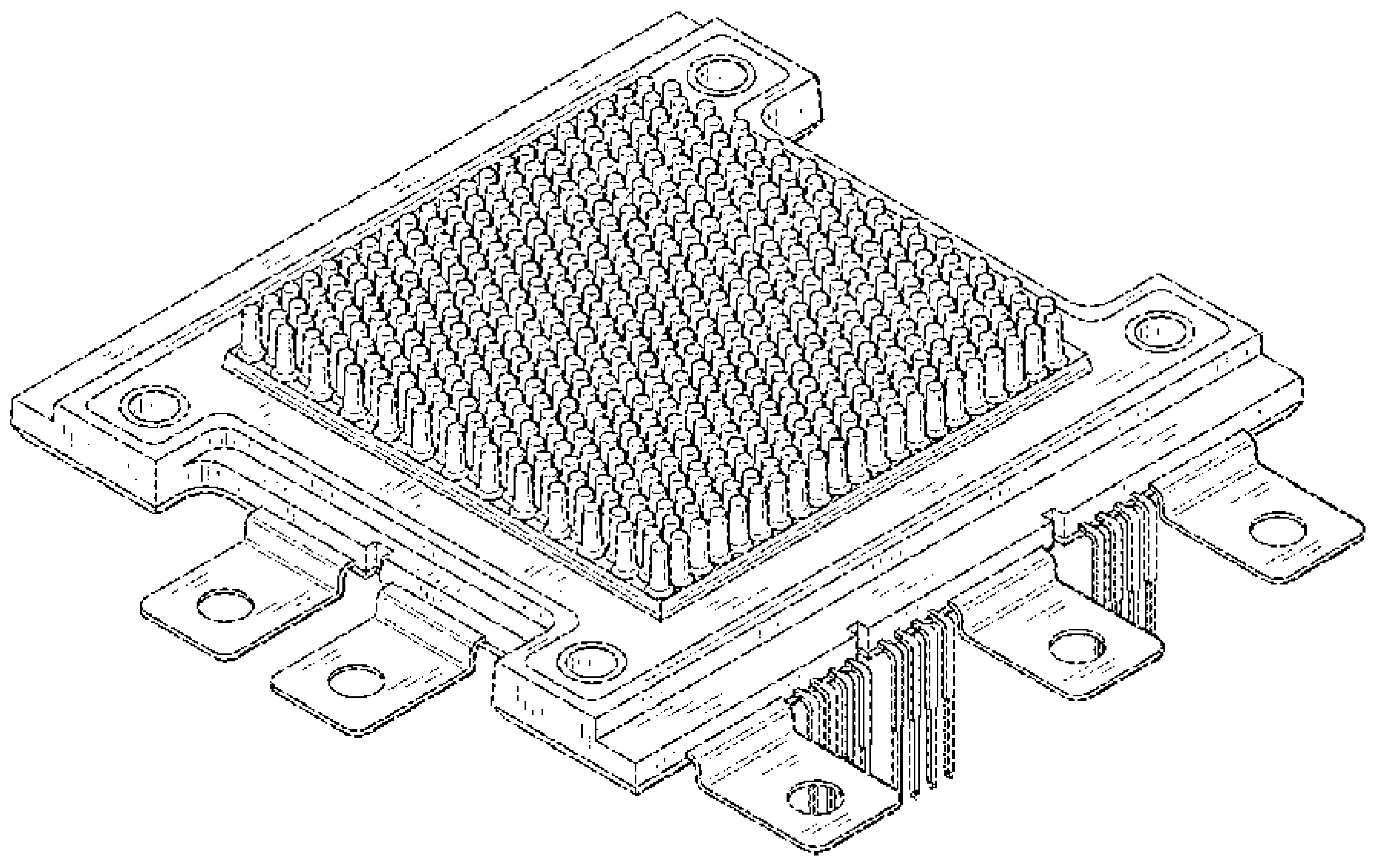


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FIG. 1

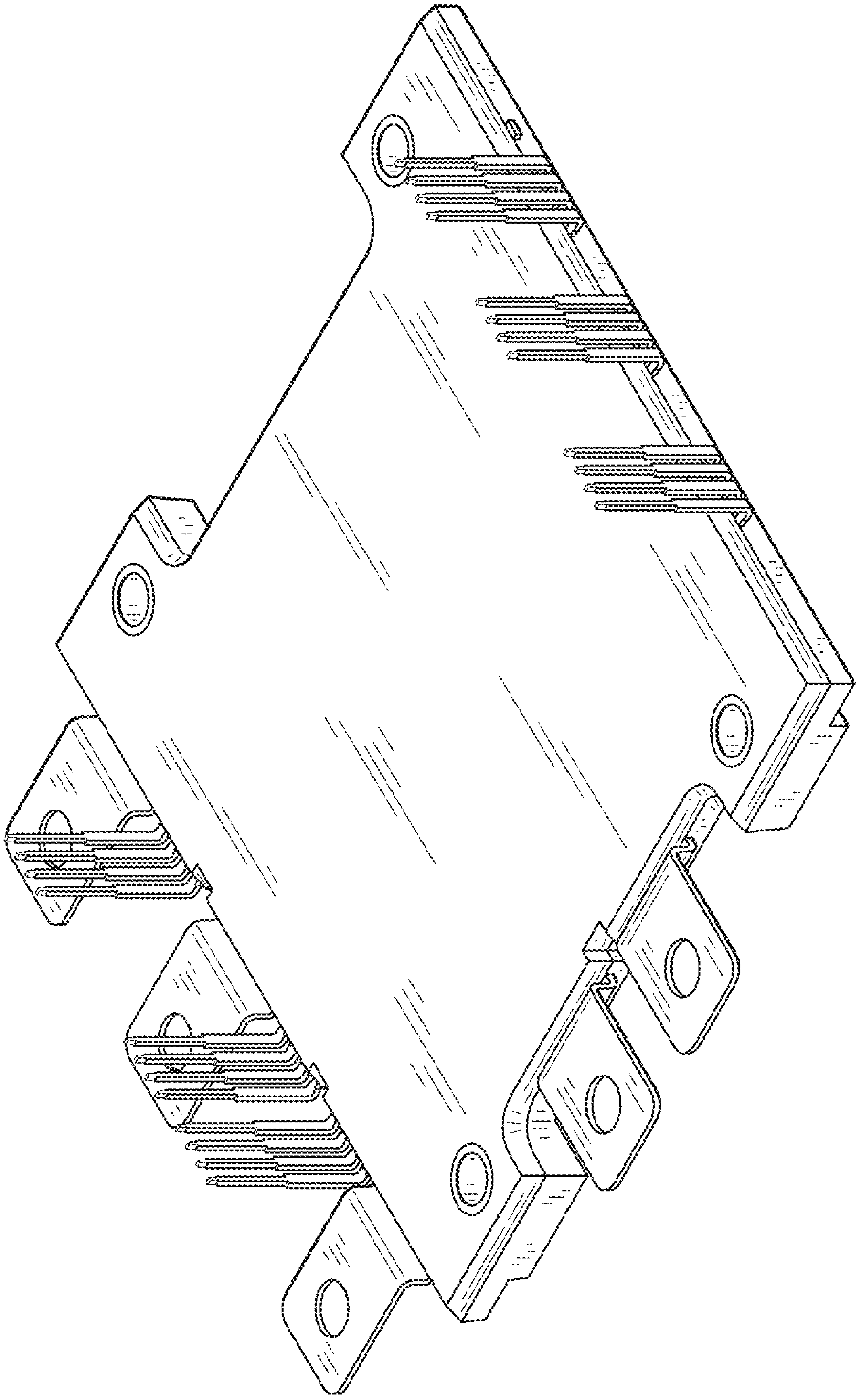

FIG. 2

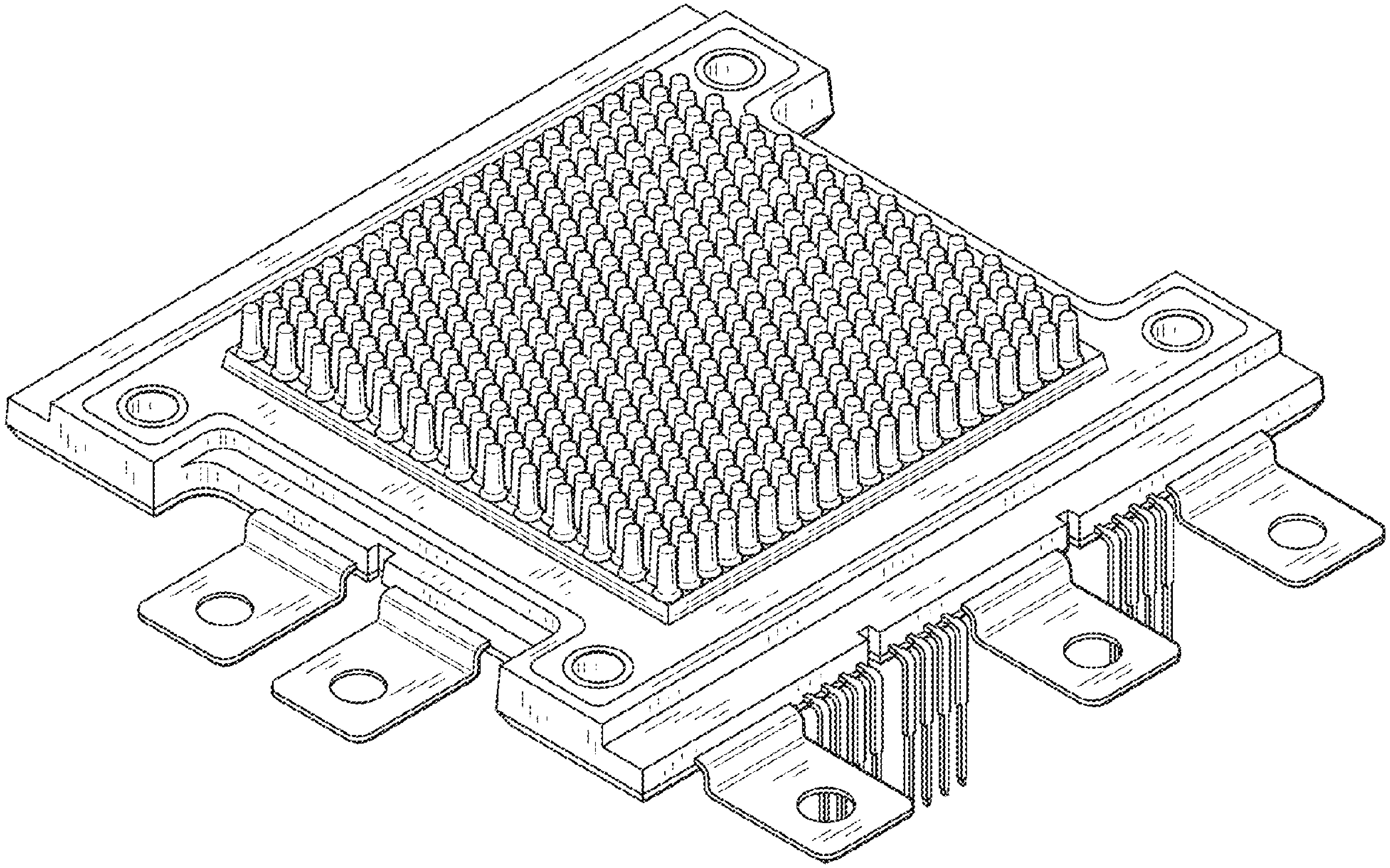

FIG. 3

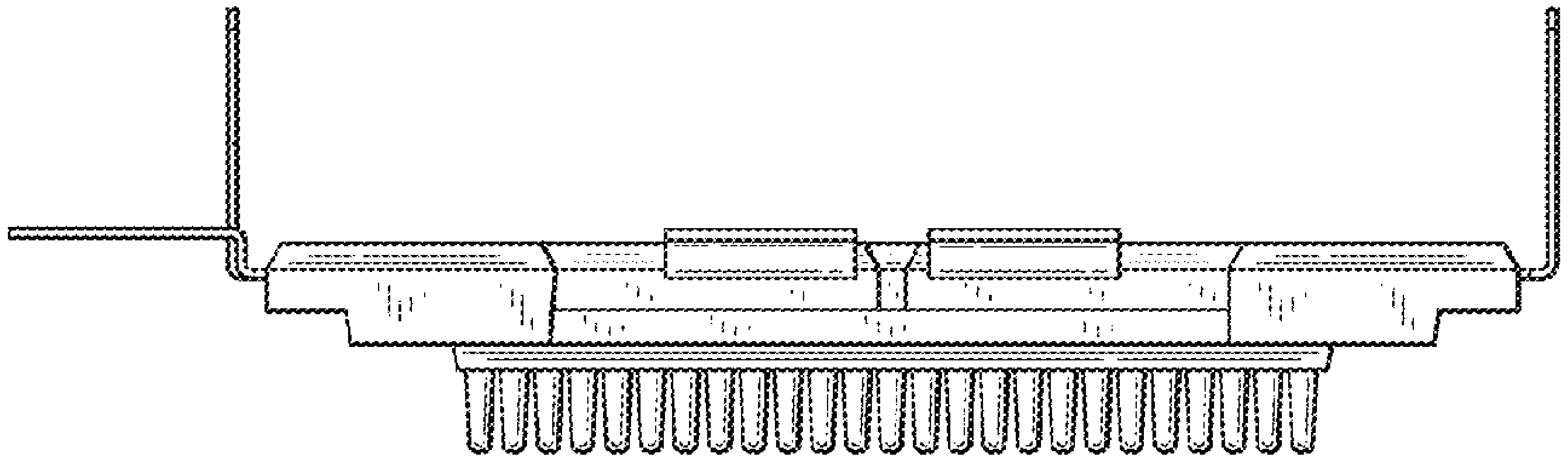

FIG. 4

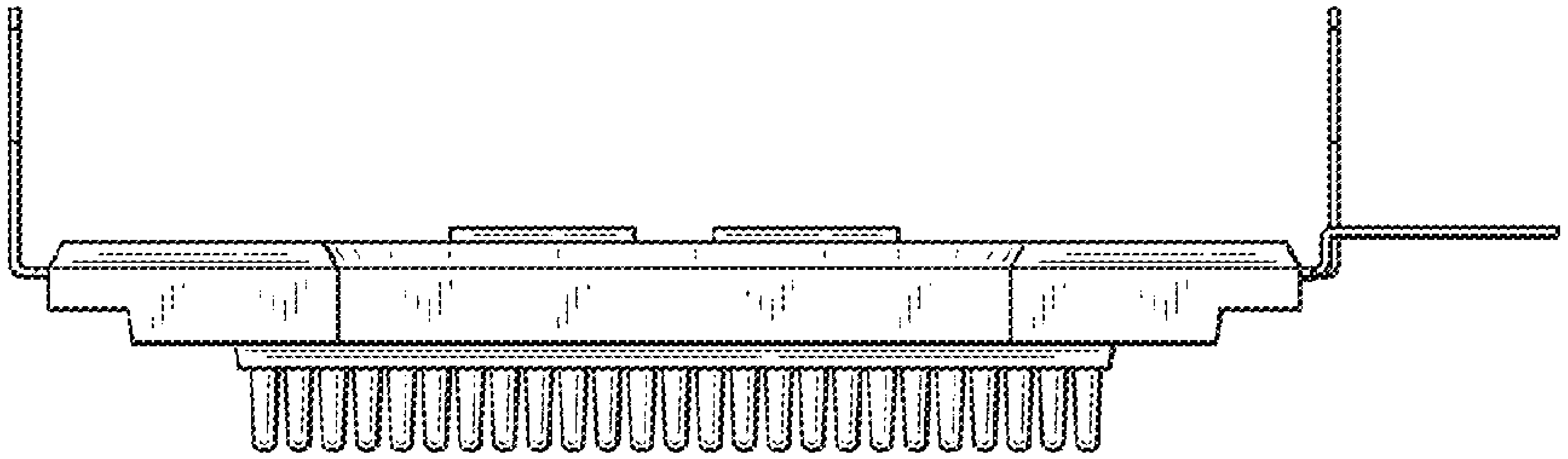

FIG. 5

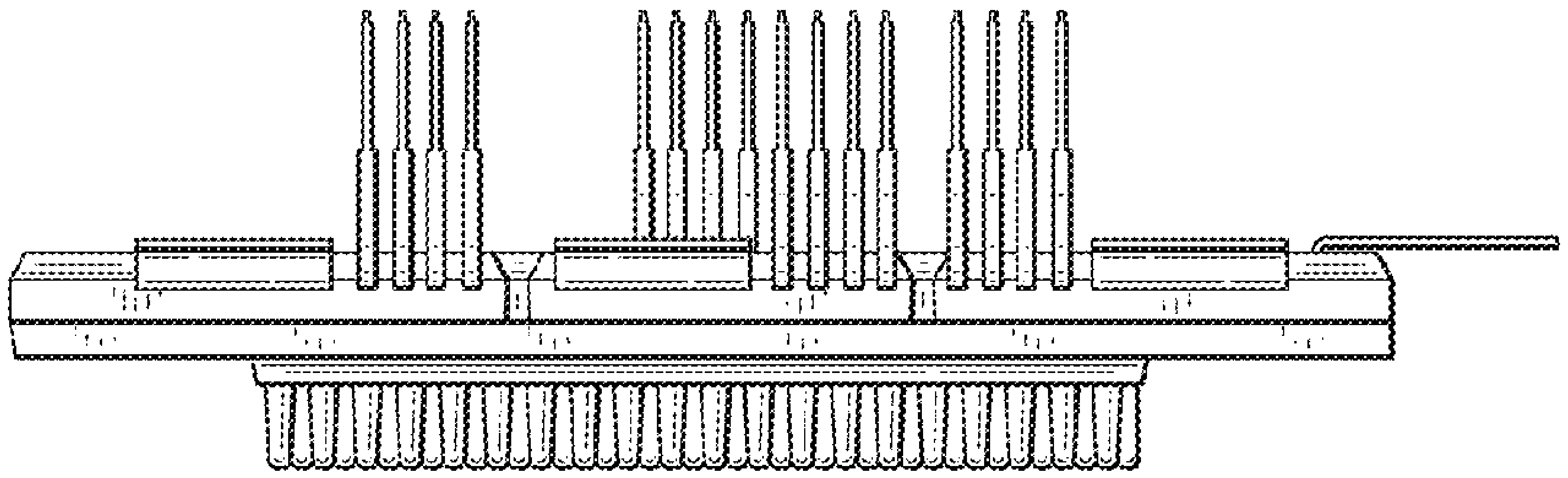

FIG. 6

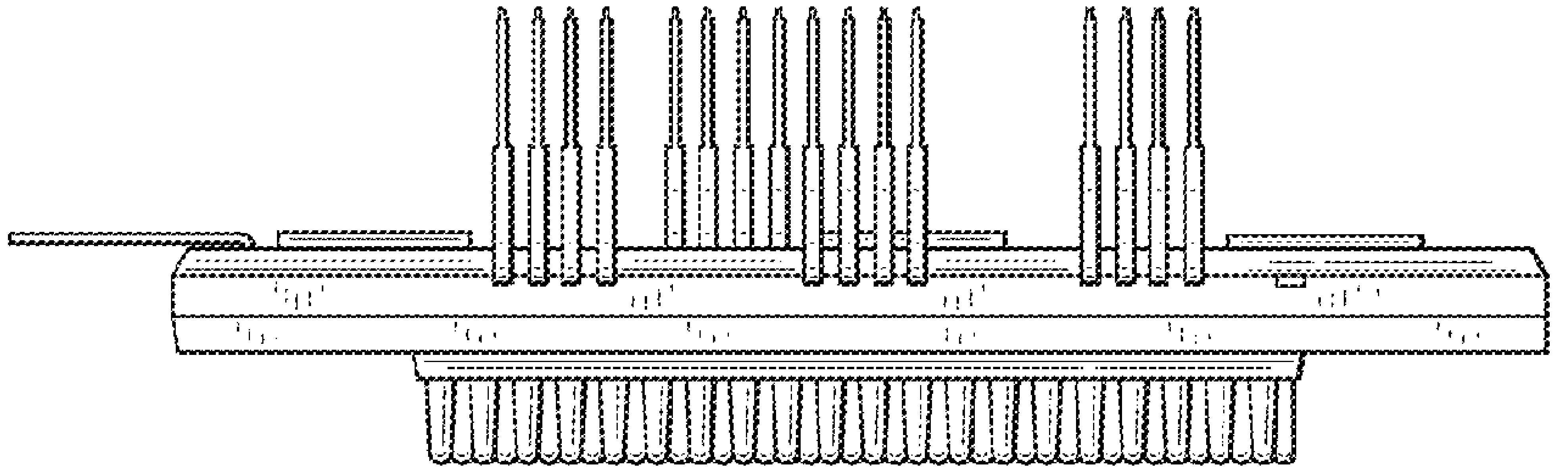

FIG. 7

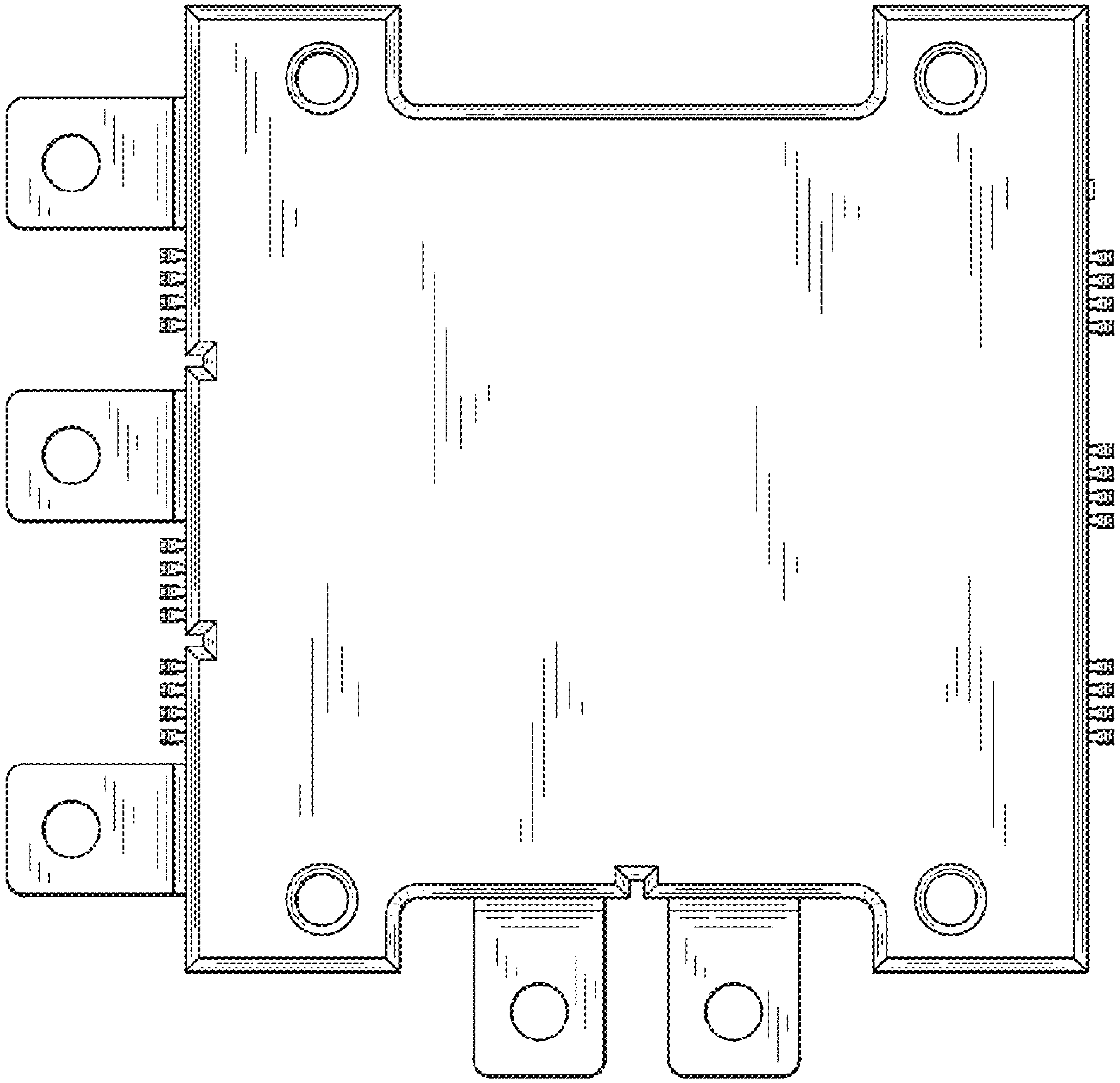

FIG. 8

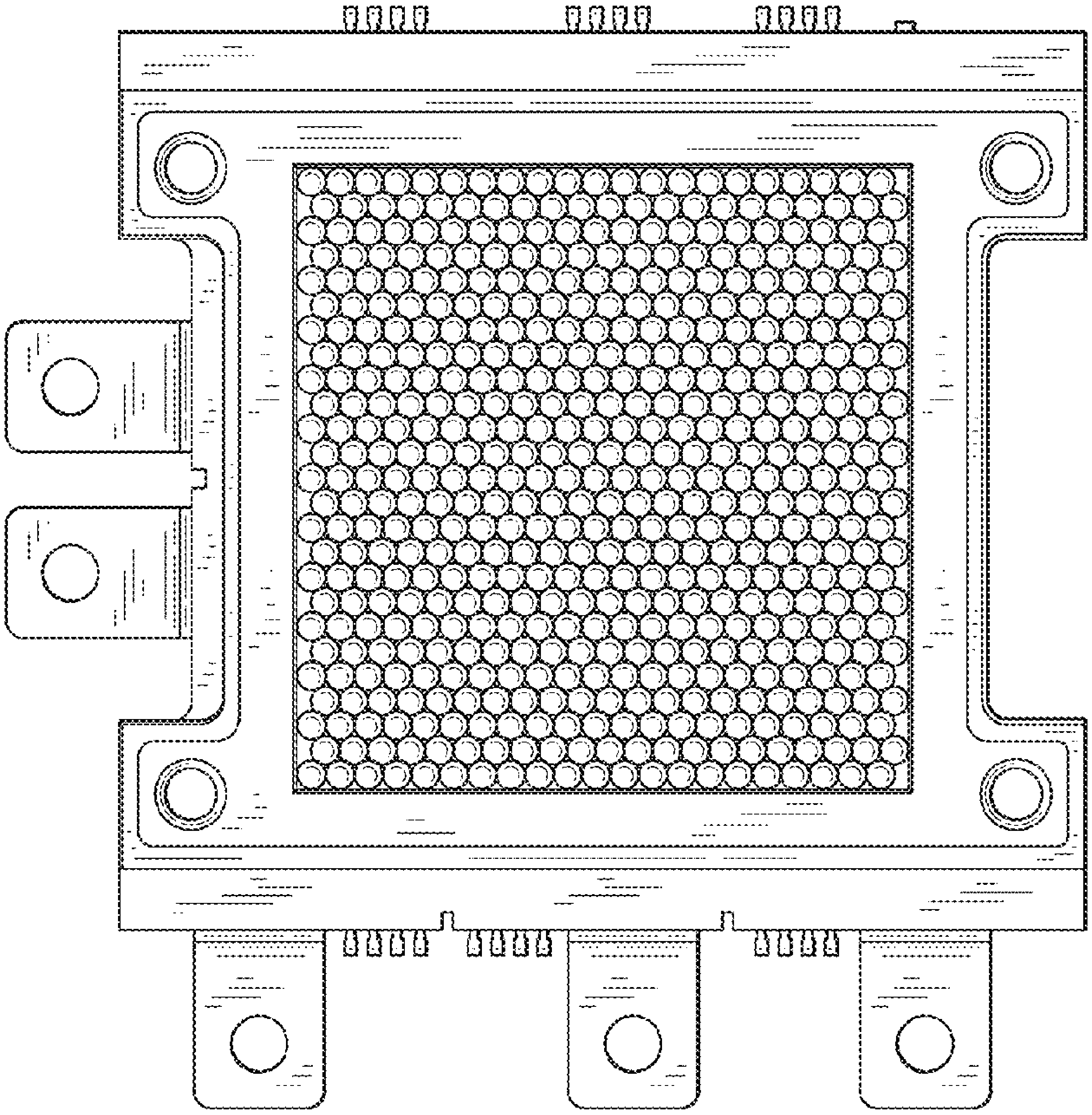

FIG. 9

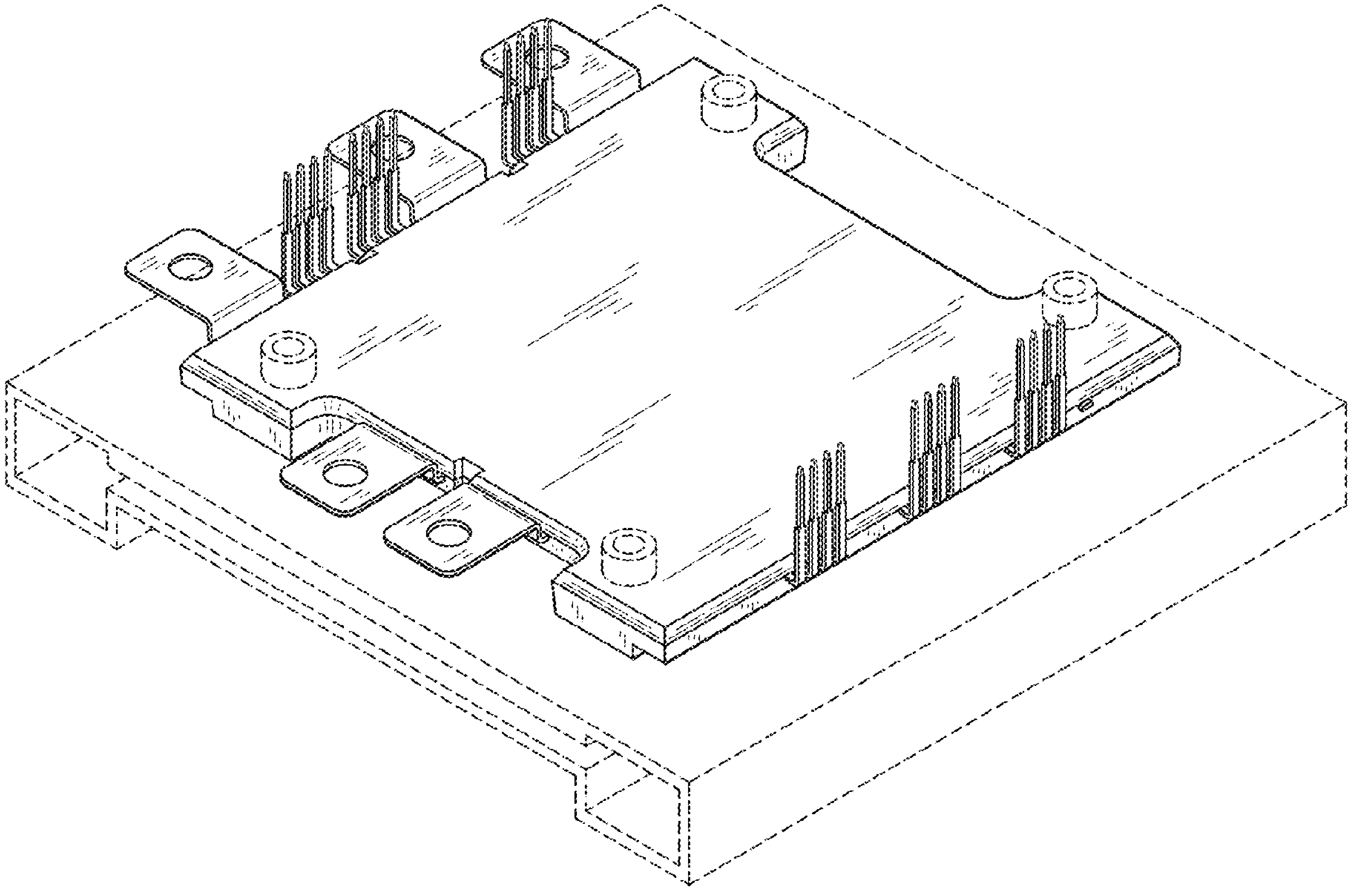

FIG. 10