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(12) **United States Design Patent**
Hu

(10) **Patent No.:** **US D716,743 S**
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(54) **PRINTED CIRCUIT BOARD OF SOLID-STATE MEMORY**

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(**) Term: **14 Years**

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/182; 174/68.1, 250, 256, 257;
318/567, 568.1; 700/22; 361/720, 722,
361/748, 749, 750, 751, 757, 752, 761, 762,
361/763, 764

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D427,159	S *	6/2000	Oba	D13/182
6,381,143	B1 *	4/2002	Nakamura	361/737
6,410,355	B1 *	6/2002	Wallace	438/15
D466,093	S *	11/2002	Ebihara et al.	D13/182
D471,167	S *	3/2003	Ebihara et al.	D13/182
7,094,633	B2 *	8/2006	Takiar	438/113
D529,031	S *	9/2006	Huang et al.	D14/436

D537,081	S *	2/2007	Takiar et al.	D14/436
D538,286	S *	3/2007	Takiar et al.	D14/436
D548,201	S *	8/2007	Jones	D13/182
7,306,161	B2 *	12/2007	Takiar et al.	235/492
7,307,848	B2 *	12/2007	Takiar	361/737
7,336,498	B2 *	2/2008	Takiar et al.	361/737
D603,812	S *	11/2009	Johnson et al.	D13/182
D605,613	S *	12/2009	Carter et al.	D13/182
7,864,540	B2 *	1/2011	Takiar	361/737
D639,756	S *	6/2011	Greene, Jr.	D13/182
D642,546	S *	8/2011	Greene, Jr.	D13/182
D669,478	S *	10/2012	Lepp et al.	D14/436
D669,479	S *	10/2012	Lepp et al.	D14/436
8,581,372	B2 *	11/2013	Asada et al.	257/668
8,649,820	B2 *	2/2014	Schwandt et al.	455/557
2002/0131251	A1 *	9/2002	Corisis et al.	361/760
2007/0163866	A1 *	7/2007	Tsai	200/292
2008/0080151	A1 *	4/2008	Shimizu et al.	361/760

* cited by examiner

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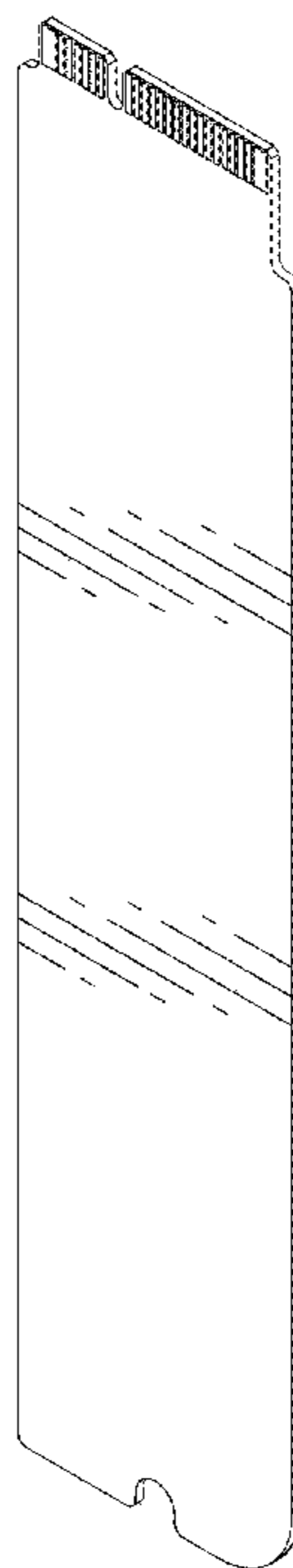
(57) **CLAIM**

The ornamental design for a printed circuit board of solid-state memory, as shown and described.

DESCRIPTION

FIG. 1 is a front, right, top perspective view of a printed circuit board of solid-state memory showing my new design;
FIG. 2 is a front view thereof;
FIG. 3 is a rear view thereof;
FIG. 4 is a left side view thereof;
FIG. 5 is a right side view thereof;
FIG. 6 is a top view thereof; and,
FIG. 7 is a bottom view thereof.

1 Claim, 7 Drawing Sheets



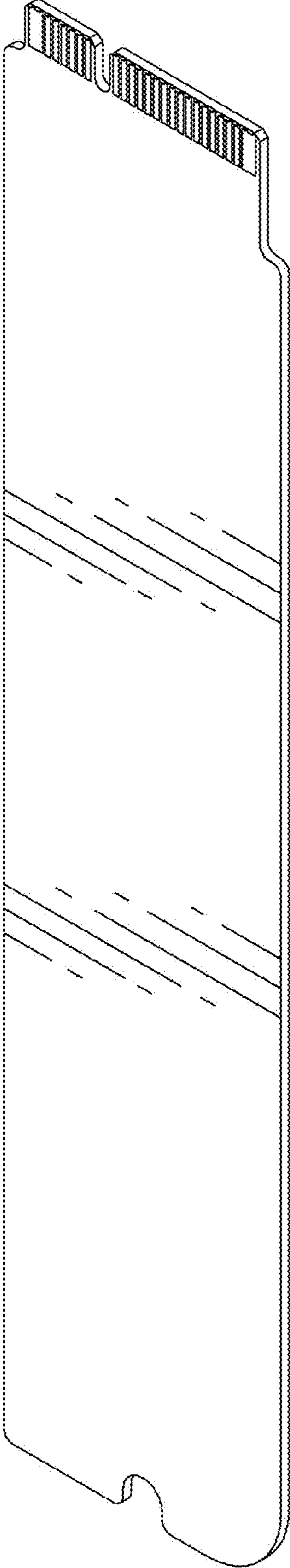


FIG. 1

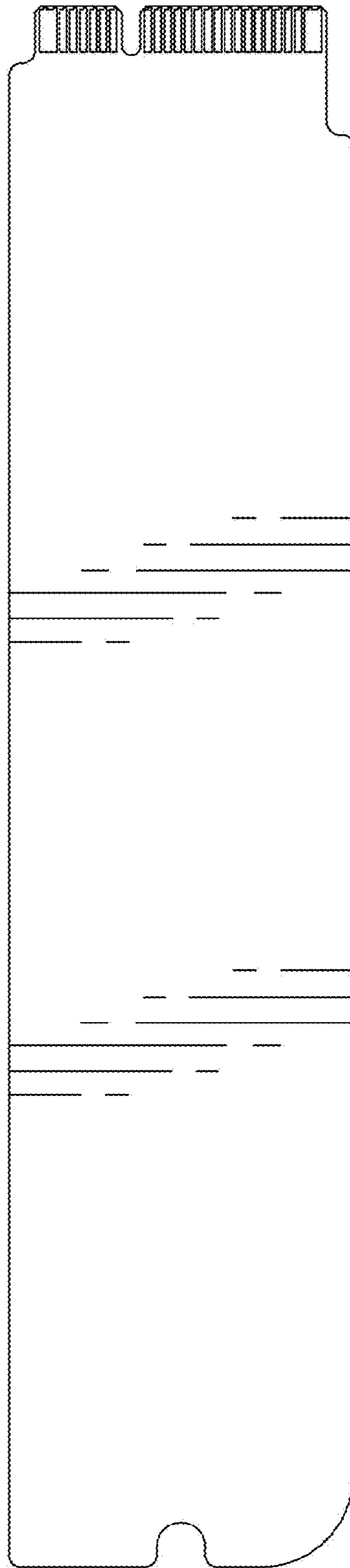


FIG. 2

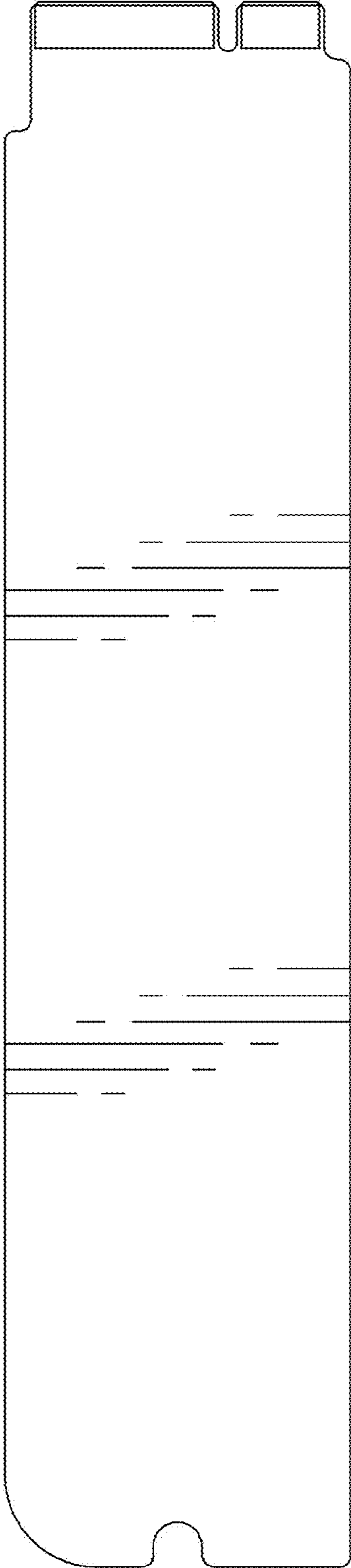


FIG. 3

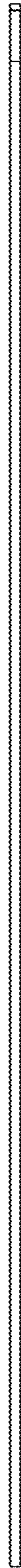


FIG. 4

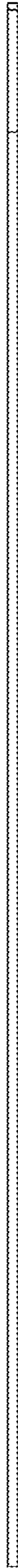


FIG. 5

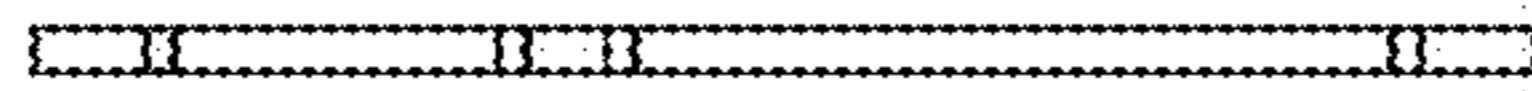


FIG. 6

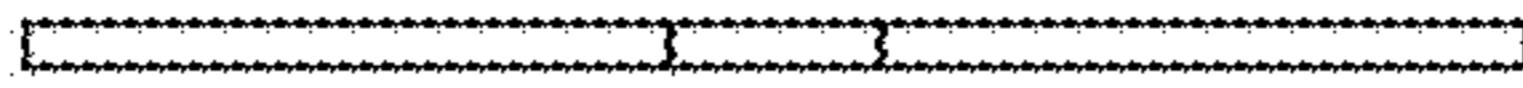


FIG. 7