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Honaga et al.

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(54) **JIG FOR MEASURING WITHSTAND VOLTAGE OF SEMICONDUCTOR ELEMENT**

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(**) Term: **14 Years**

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Oct. 5, 2012	(JP)	2012-024373

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(52) **U.S. Cl.**
USPC **D10/103**
(58) **Field of Classification Search**
USPC D10/78, 103; 206/710, 832; 204/228.7, 204/229.8, 230.8; 257/620, 415, E21.567, 257/228, 79, E29.151, E51.005, 330, 591, 257/E21.384, E29.198, E21.267; 438/680, 438/459, 113, 464, 462, 455, 149, 772, 762, 438/777, 786, 158, 28, 654
See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a jig for measuring withstand voltage of semiconductor element, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a first embodiment of the jig for measuring withstand voltage of semiconductor element, which has tapped holes used to hold a substrate provided with a semiconductor element and has a hollow to contain insulating liquid to submerge the substrate during measurement of a withstanding voltage of the element, showing our new design;
FIG. **2** is a rear view thereof;
FIG. **3** is a top plan view thereof;
FIG. **4** is a bottom plan view thereof;
FIG. **5** is a right side view thereof;
FIG. **6** is a left side view thereof;
FIG. **7** is a front perspective view thereof;
FIG. **8** is a sectional view taken along line **8**-**8** of FIG. **3** thereof;
FIG. **9** is a referential top plan view showing the state in use thereof; and,
FIG. **10** is a referential front perspective view showing the state in use thereof.
The broken line showing is for illustrative purpose only and forms no part of the claimed design.

1 Claim, 5 Drawing Sheets

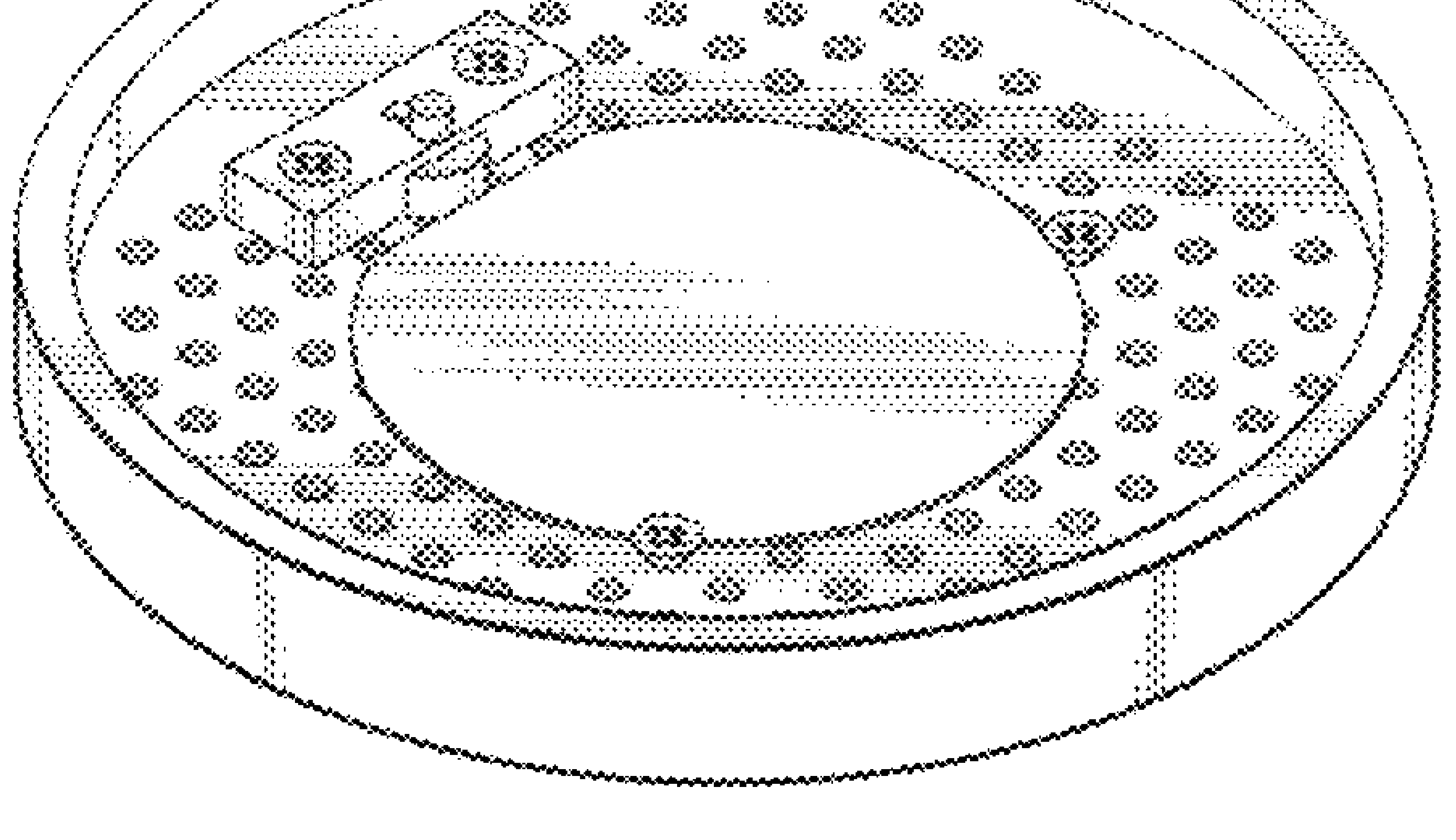

FIG.1

FIG.2

FIG.3

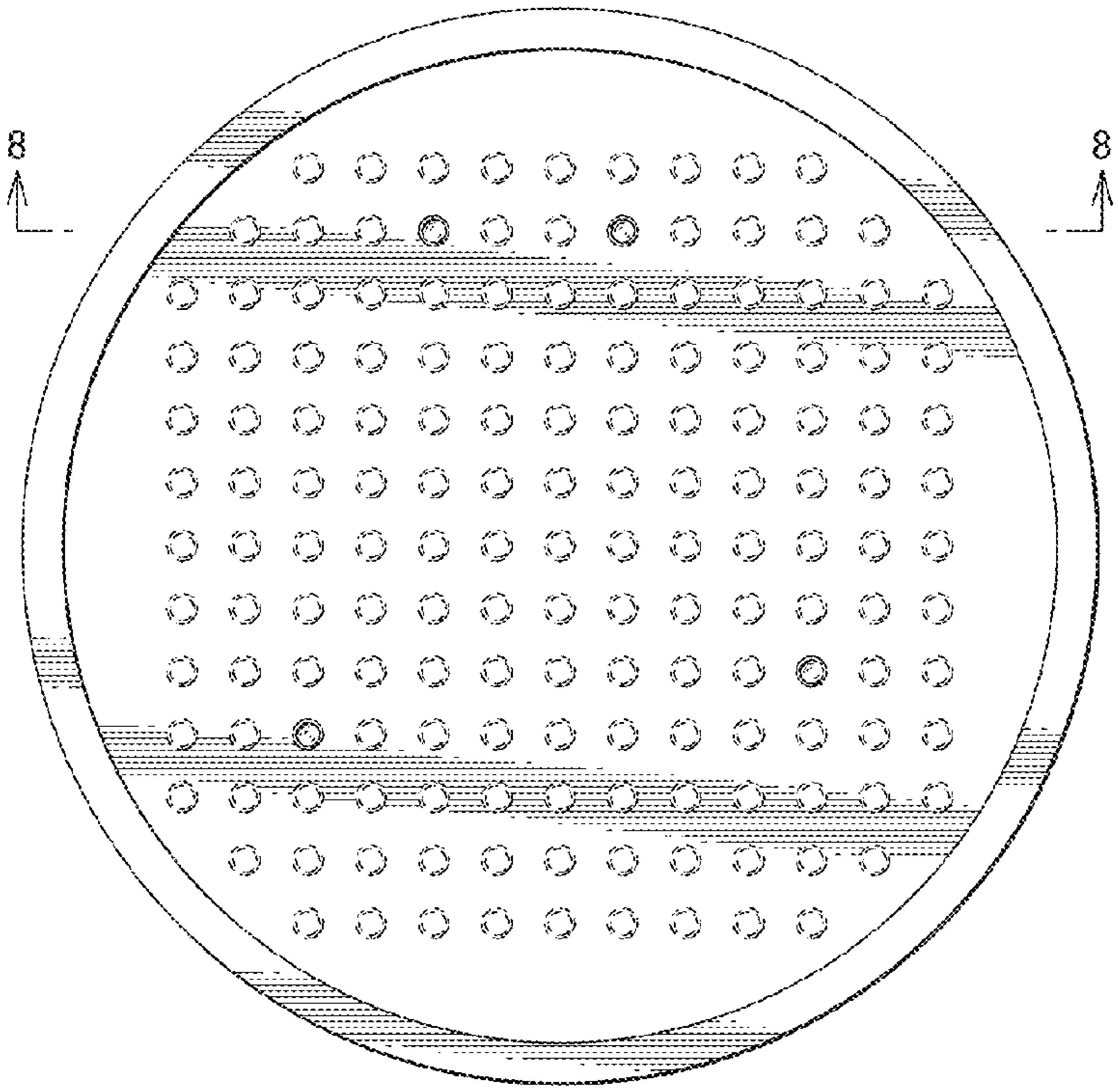

FIG.4

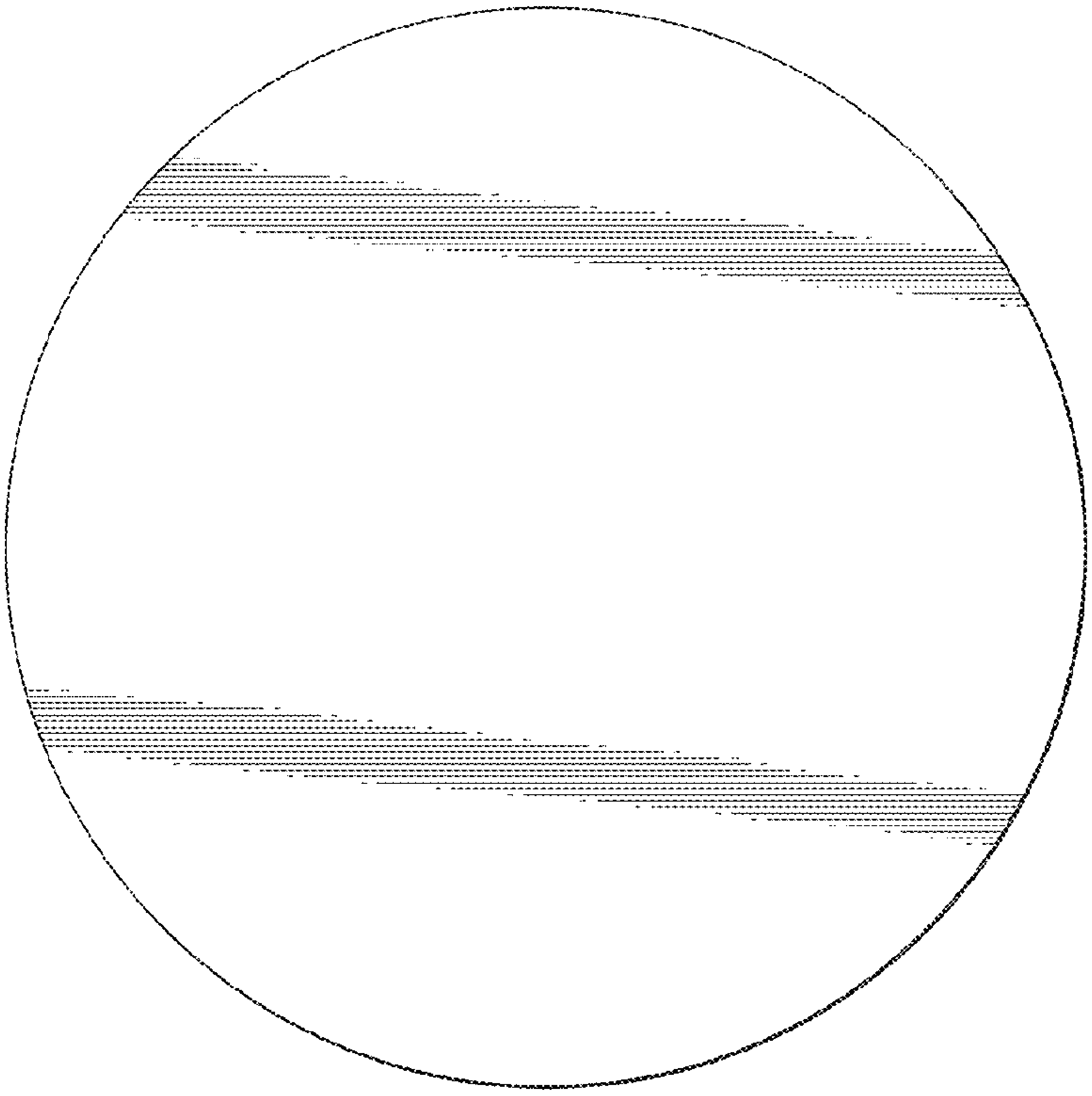

FIG.5

FIG.6

FIG.7

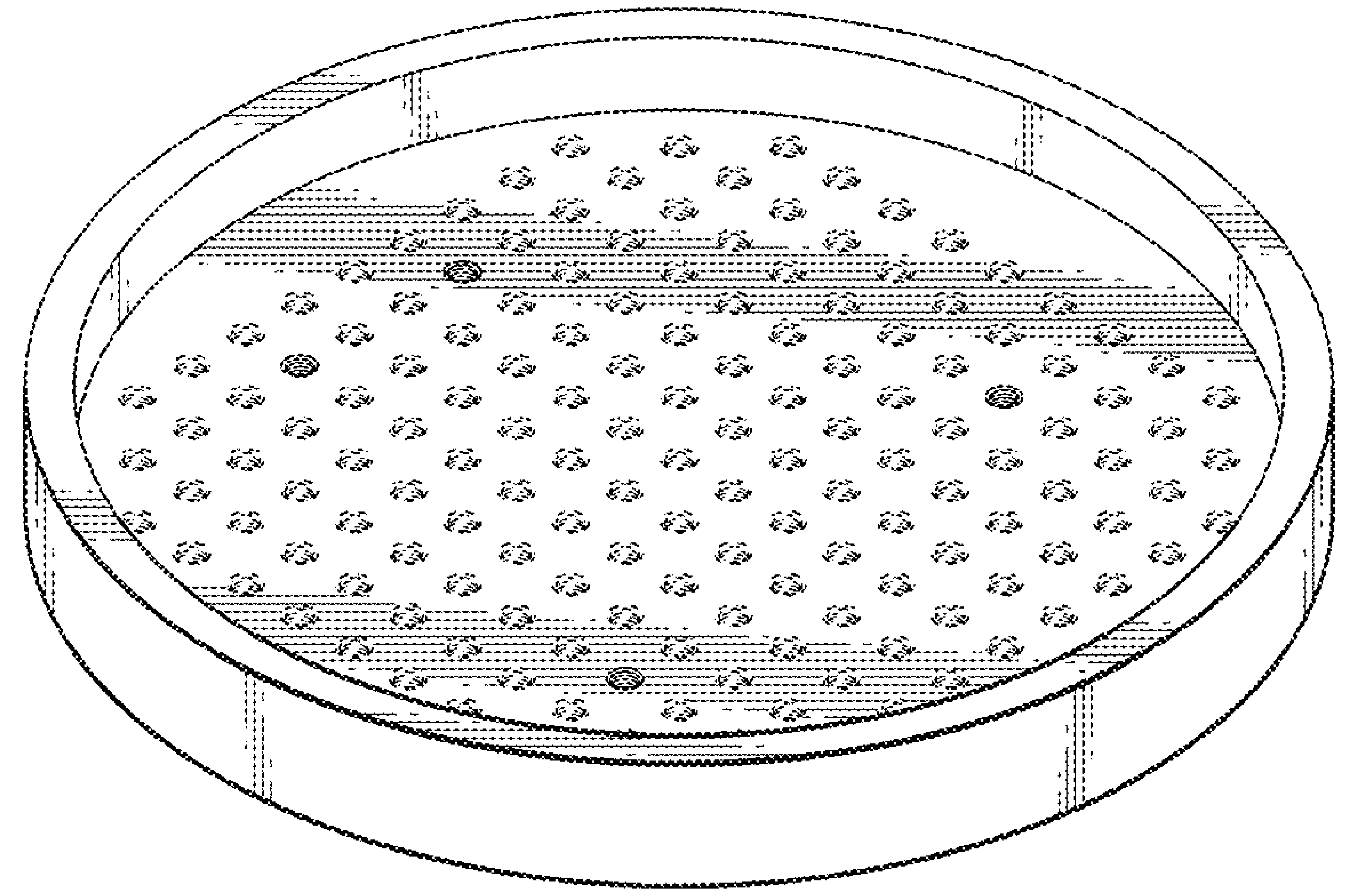

FIG.8

FIG.9

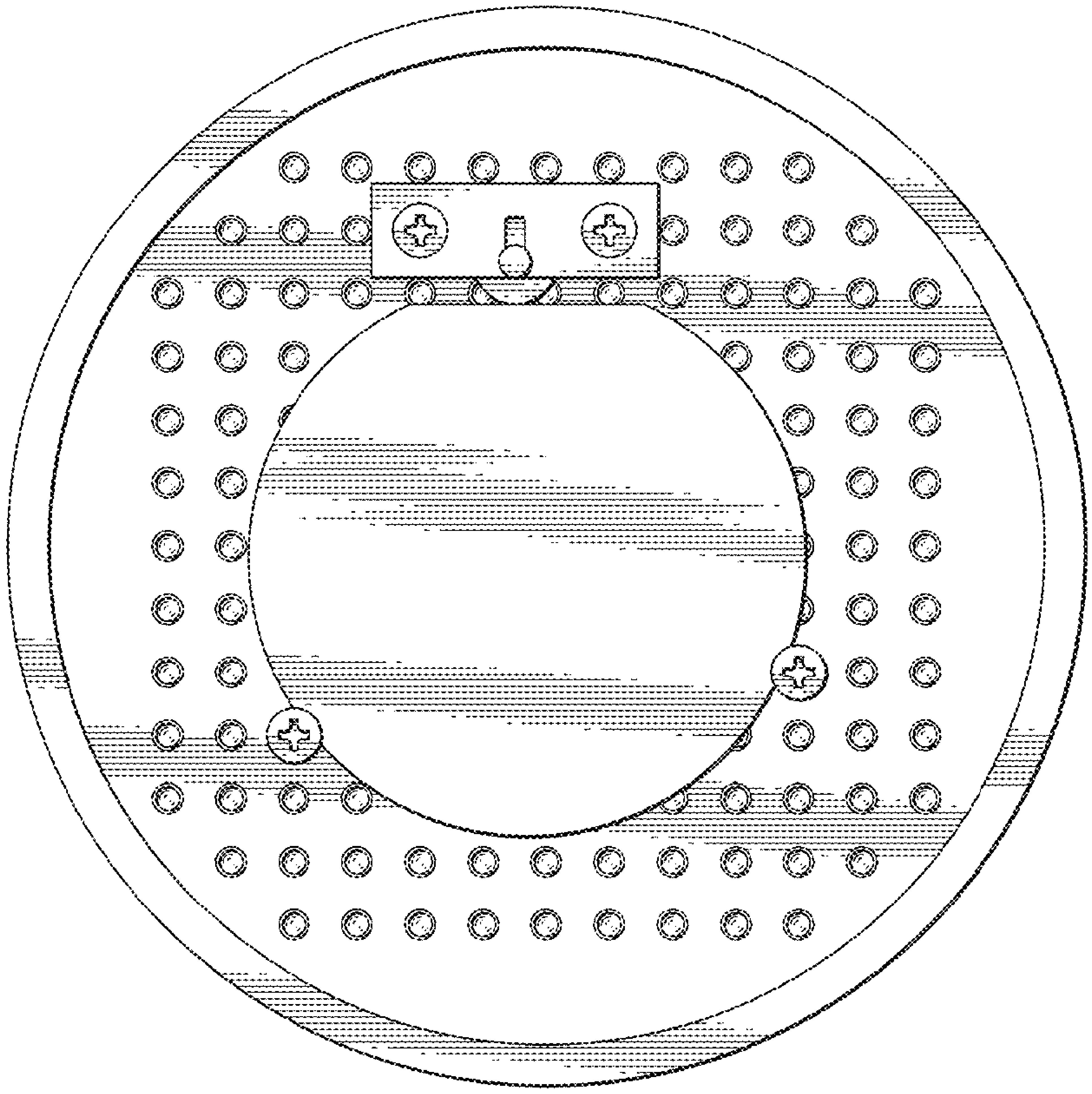

FIG.10