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(12) **United States Design Patent**
Nakano et al.

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- (54) **INTEGRATED CIRCUIT TAG**
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- (30) **Foreign Application Priority Data**
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- (51) **LOC (10) Cl.** **13-03**
- (52) **U.S. Cl.**
USPC **D13/182**
- (58) **Field of Classification Search**
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29/825, 829, 830, 831, 832, 846;
174/68.1, 250-257, 260, 261, 268;
216/13; 361/718, 748, 752, 760, 783,
361/820; 428/901
See application file for complete search history.

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(57) **CLAIM**
The ornamental design for an integrated circuit tag, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of an integrated circuit tag showing our new design;
FIG. 2 is a front elevational view thereof;
FIG. 3 is a right side elevational view thereof;
FIG. 4 is a left side elevational view thereof;
FIG. 5 is a top plan view thereof; and,
FIG. 6 is a bottom plan view thereof.
The broken lines shown in the drawings represent portions of the integrated circuit tag that form no part of the claimed design.

1 Claim, 4 Drawing Sheets

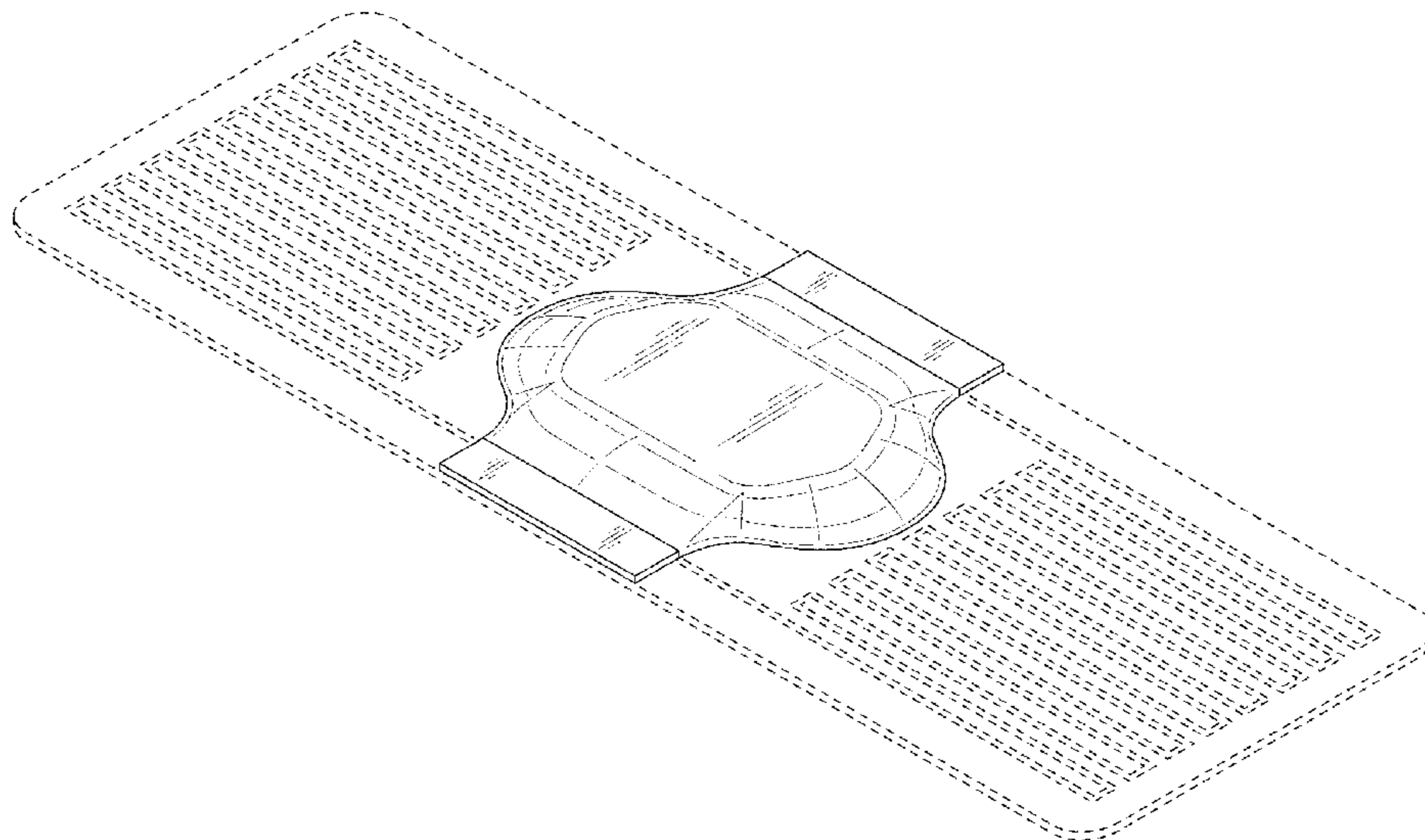


FIG.1

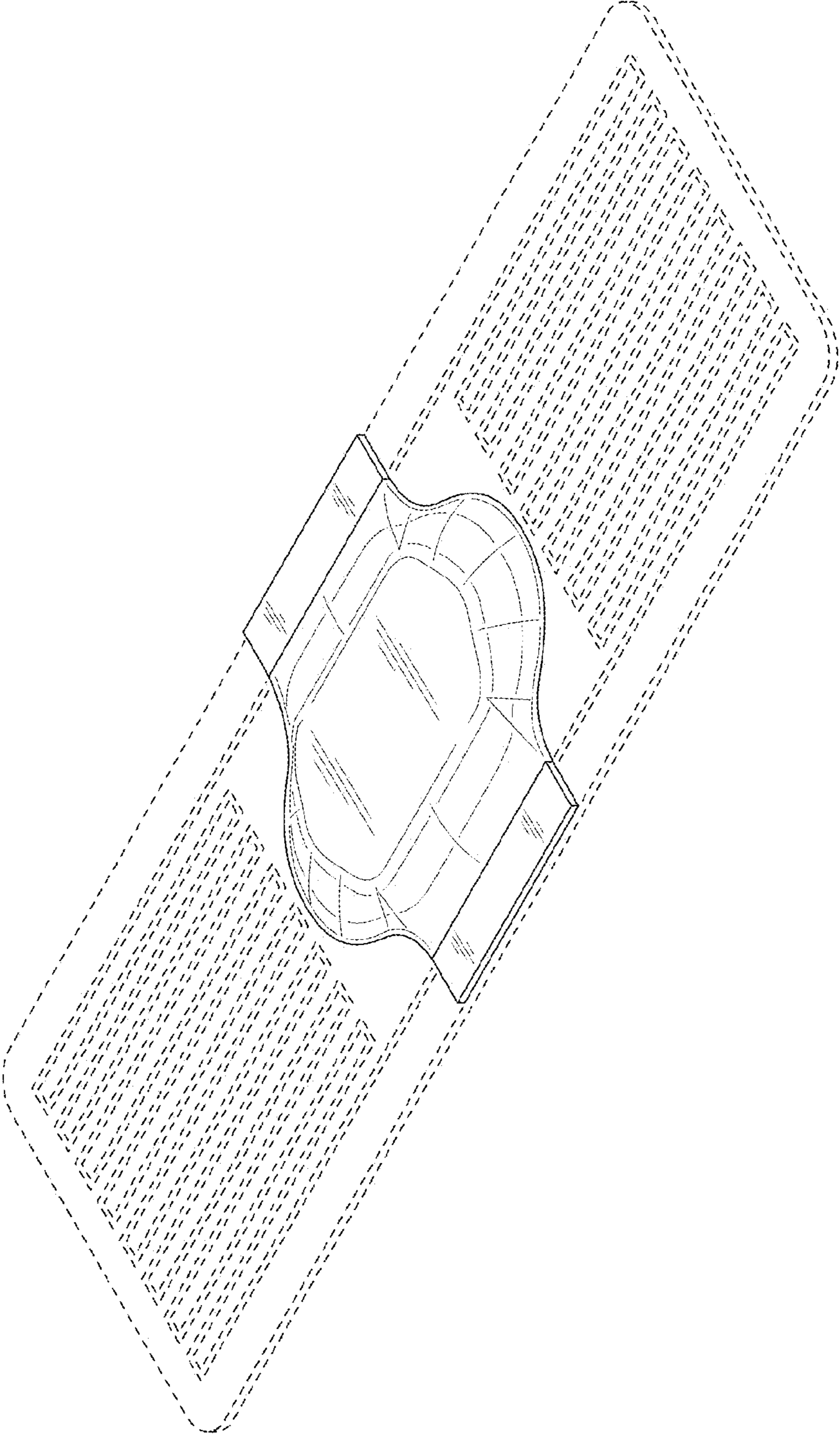


FIG.2

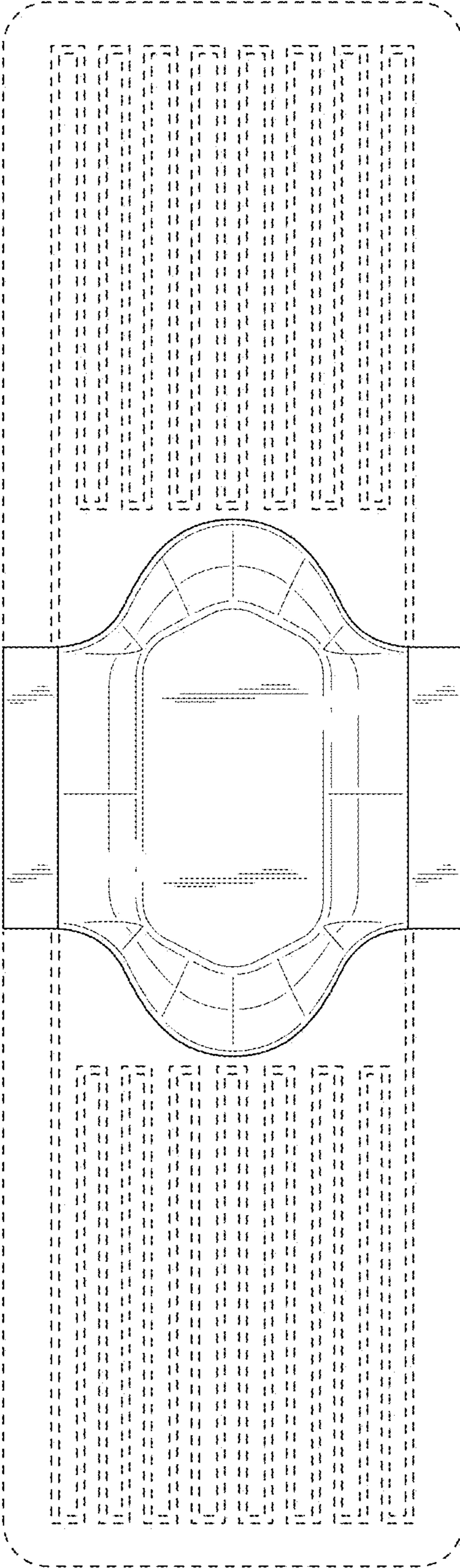


FIG.3

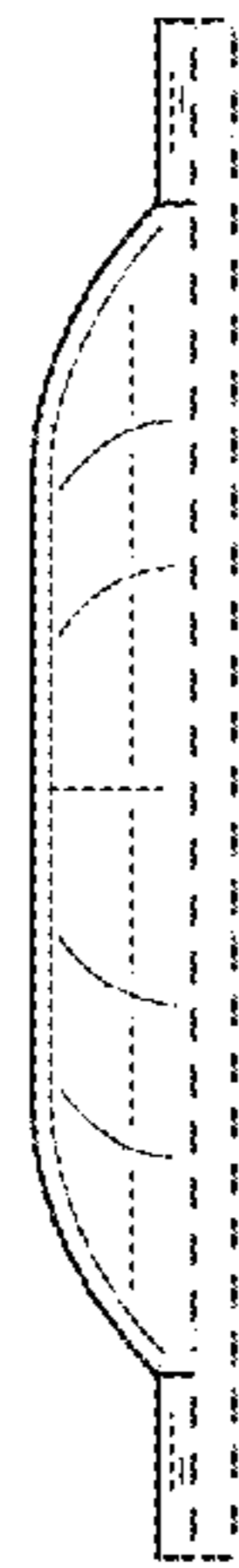


FIG.4

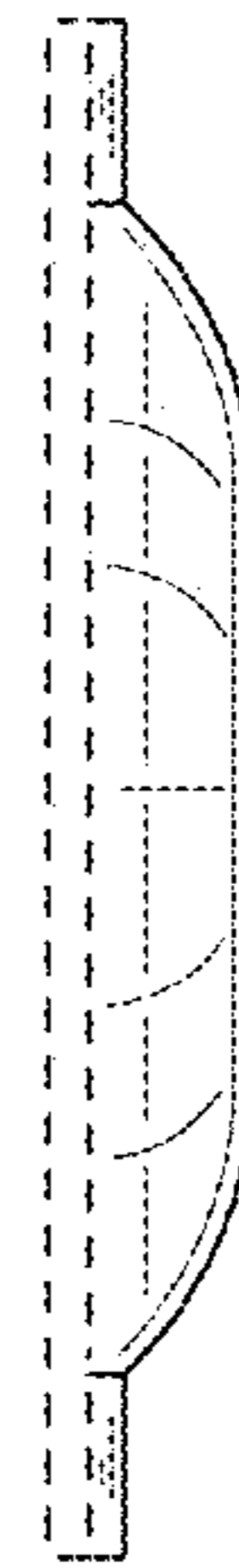


FIG.5

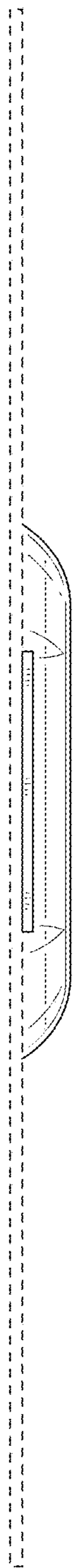


FIG.6

