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(12) **United States Design Patent**
Chen et al.

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(54) **SEMICONDUCTOR DEVICE**

(71) Applicant: **Fuji Electric Co., Ltd.**, Kawasaki (JP)

(72) Inventors: **Shuangching Chen**, Matsumoto (JP);
Akira Iso, Matsumoto (JP); **Takashi Hyakutake**, Matsumoto (JP); **Syongo Ogawa**, Matsumoto (JP); **Syuuji Miyashita**, Matsumoto (JP)

(73) Assignee: **Fuji Electric Co., Ltd.**, Kawasaki-shi, Kanagawa (JP)

(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/110, 182; 257/668, 678, 690;
361/679.01, 713, 728, 736, 760, 761,
361/775, 820; 324/71.5, 252; 174/250, 253;
438/64, 65, 66

See application file for complete search history.

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Primary Examiner — Elizabeth J Oswecki

(74) *Attorney, Agent, or Firm* — Young Basile Hanlon & MacFarlane P.C.

(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. 1 is a front view of a semiconductor device showing our new design;

FIG. 2 is a rear view of the semiconductor device of FIG. 1; FIG. 3 is a left side view of the semiconductor device of FIG. 1;

FIG. 4 is a right side view of the semiconductor device of FIG. 1;

FIG. 5 is a top view of the semiconductor device of FIG. 1; FIG. 6 is a bottom view of the semiconductor device of FIG. 1;

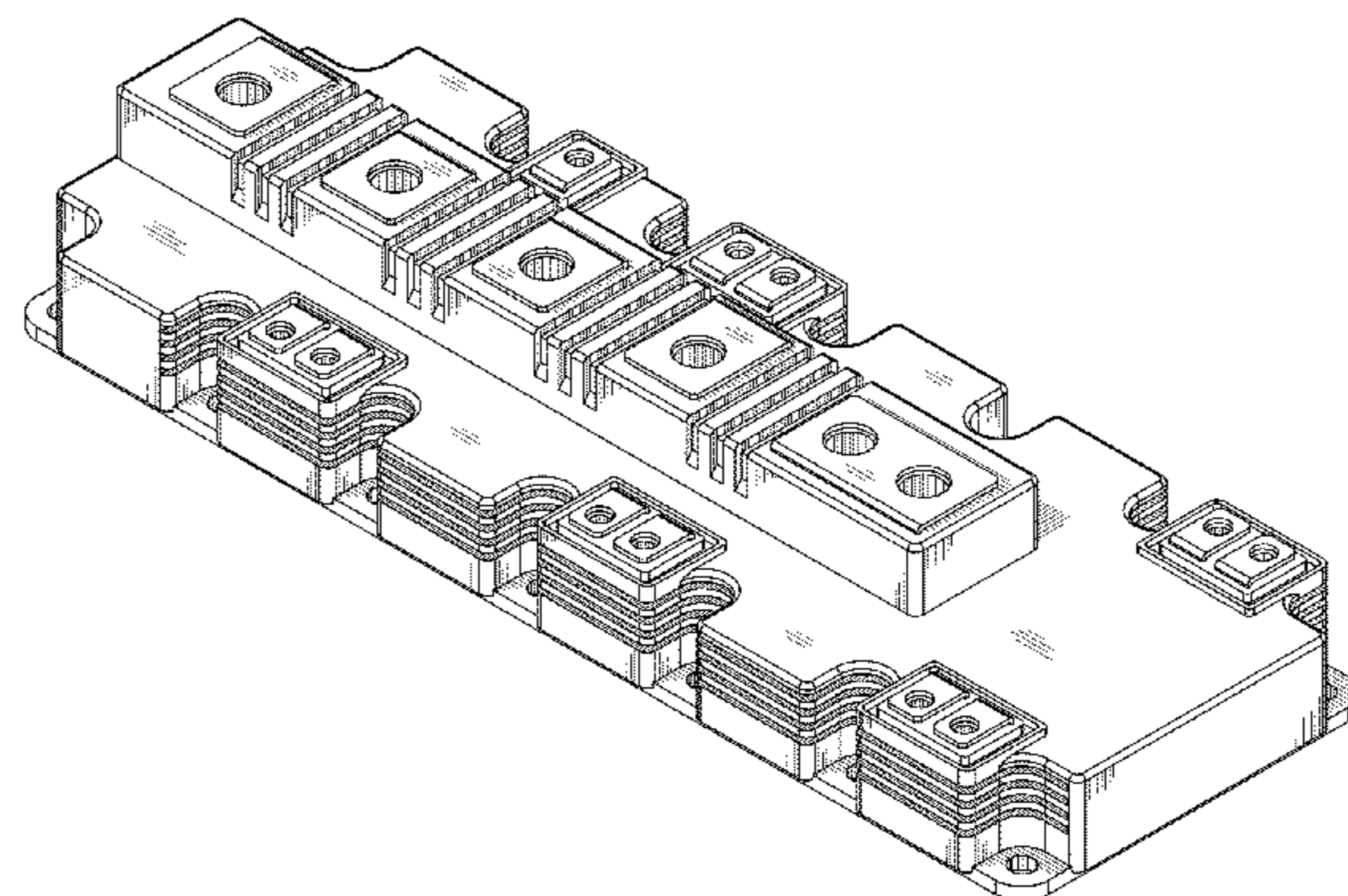
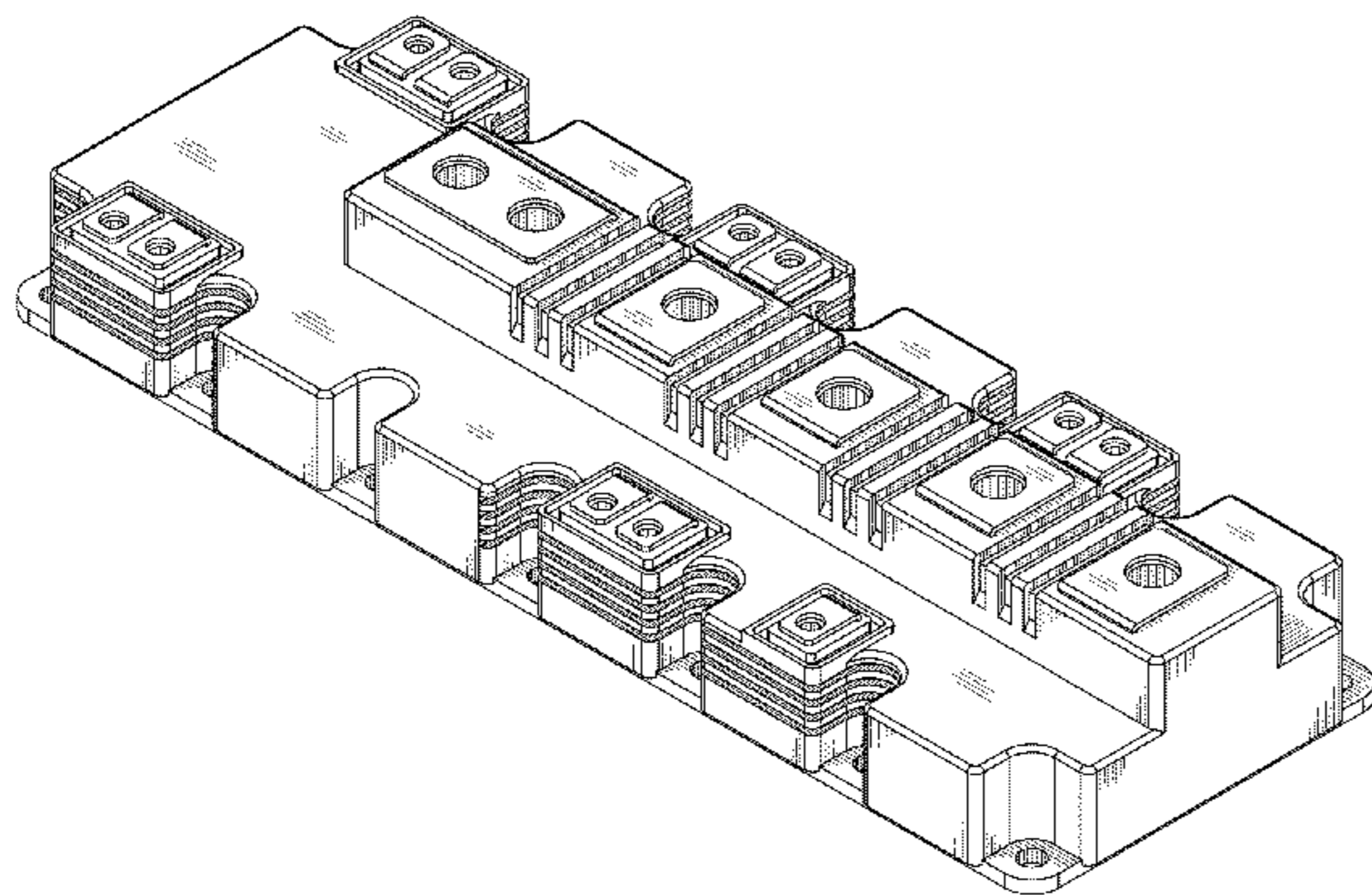
FIG. 7 is a top, front and right side perspective view of the semiconductor device of FIG. 1; and,

FIG. 8 is a top, rear and left side perspective view of the semiconductor device of FIG. 1.

The broken lines shown in the drawings represent portions of the semiconductor device that form no part of the claimed design.

The ornamental design of the present disclosure is for a semiconductor device that may accommodate a circuit board on which circuit components such as power semiconductor elements are mounted.

1 Claim, 8 Drawing Sheets



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Fig. 1

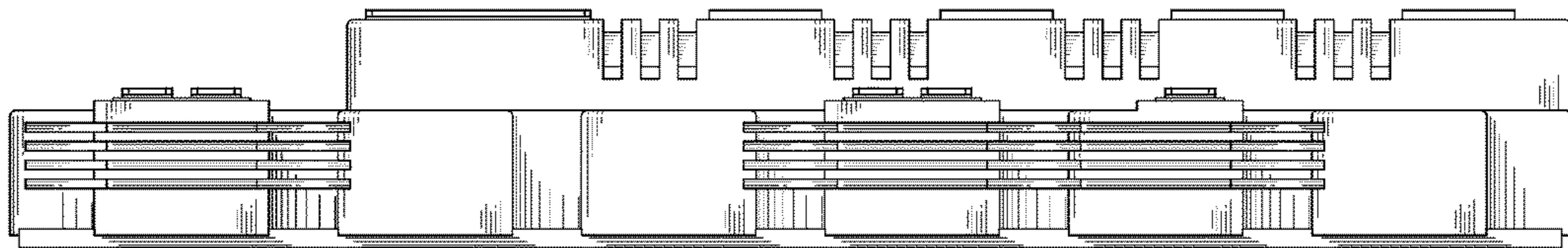


Fig.2

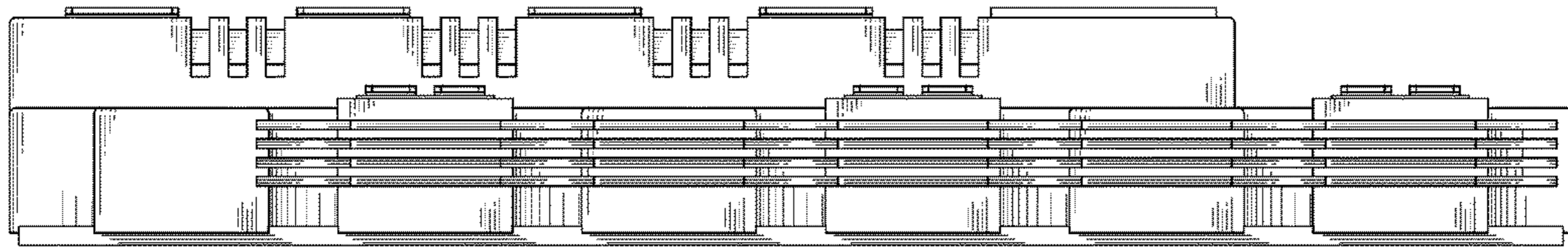


Fig. 3

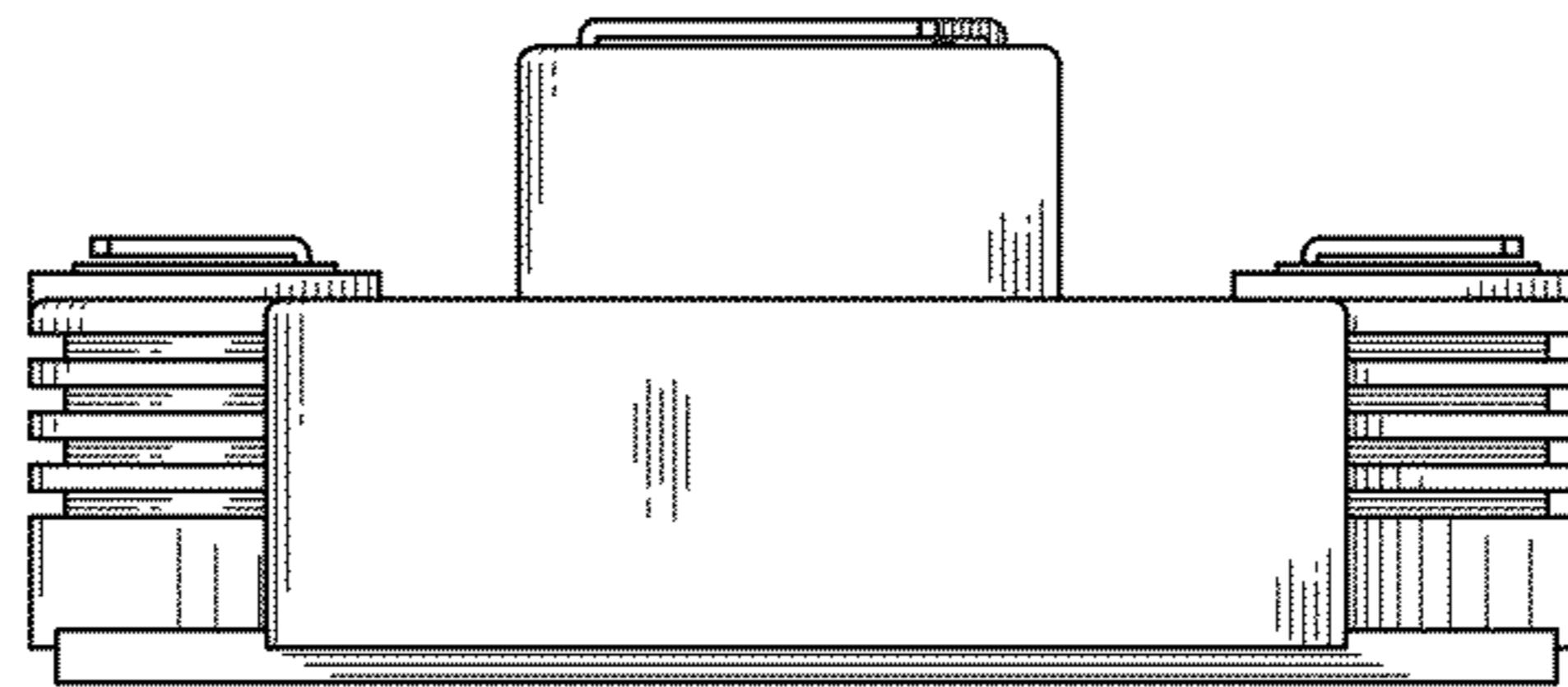


Fig. 4

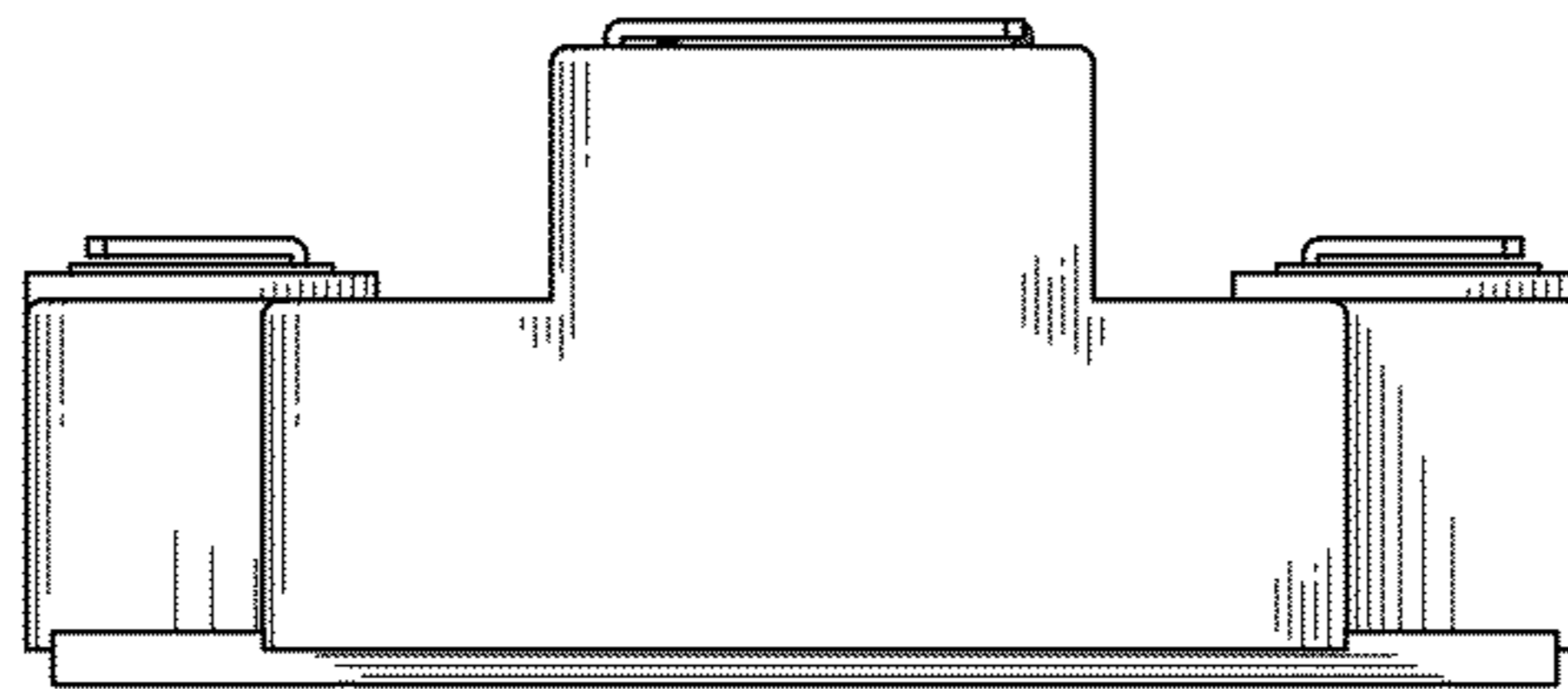


Fig. 5

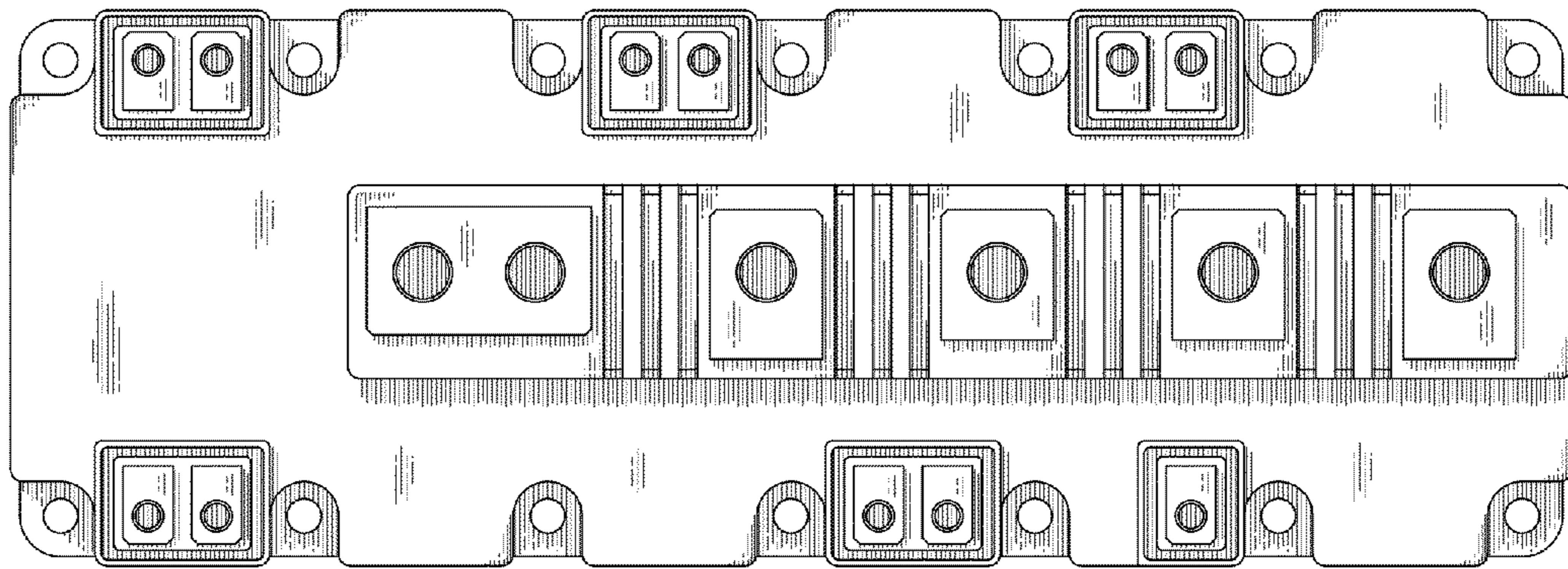


Fig.6

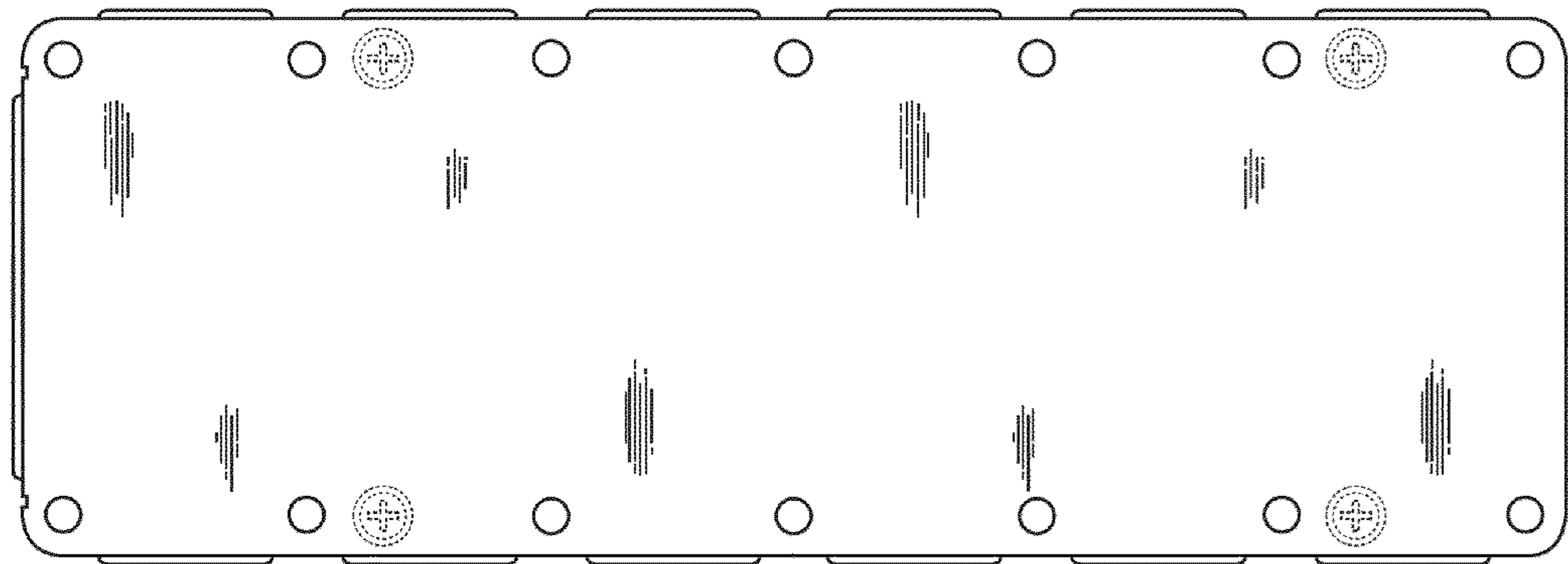


Fig. 7

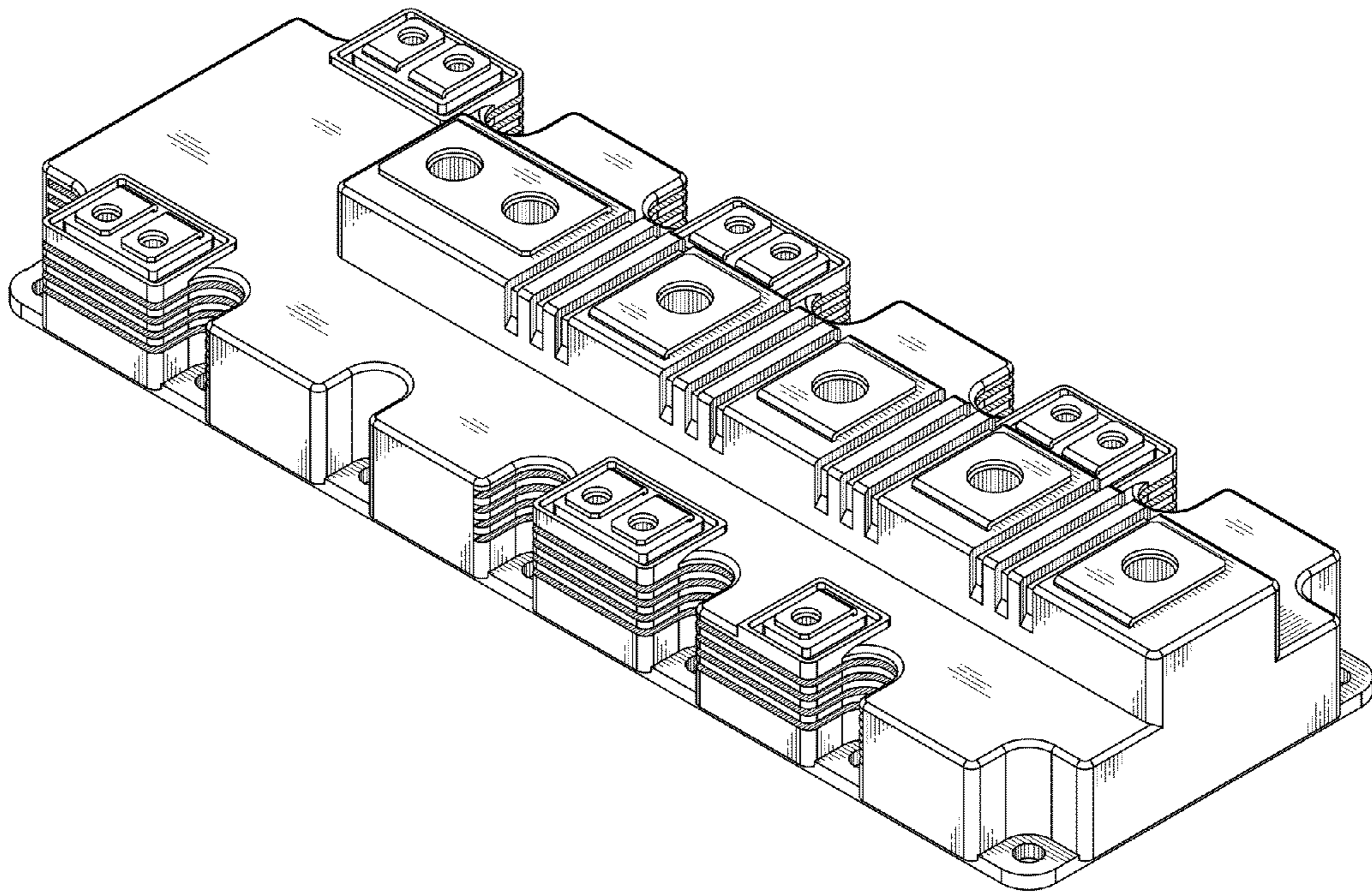


Fig. 8

