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(12) United States Design Patent

Nakamura

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(54) **SEMICONDUCTOR DEVICE**

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(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/110, 182, 184; 361/713, 728, 736, 361/760, 761, 775, 679.01, 820; 257/666, 257/668, 678, 690; 324/71.5, 252; 174/250, 174/253; 438/64, 65, 66
See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a semiconductor device showing my new design;
FIG. **2** is a rear view of the semiconductor device of FIG. **1**;
FIG. **3** is a left side view of the semiconductor device of FIG. **1**;
FIG. **4** is a right side view of the semiconductor device of FIG. **1**;
FIG. **5** is a top view of the semiconductor device of FIG. **1**;
FIG. **6** is a bottom view of the semiconductor device of FIG. **1**; and,
FIG. **7** is a perspective view of the semiconductor device of FIG. **1**.

The ornamental design of the present disclosure is a semiconductor device forming a case that may accommodate a plurality of semiconductor modules arranged in a line.

1 Claim, 7 Drawing Sheets

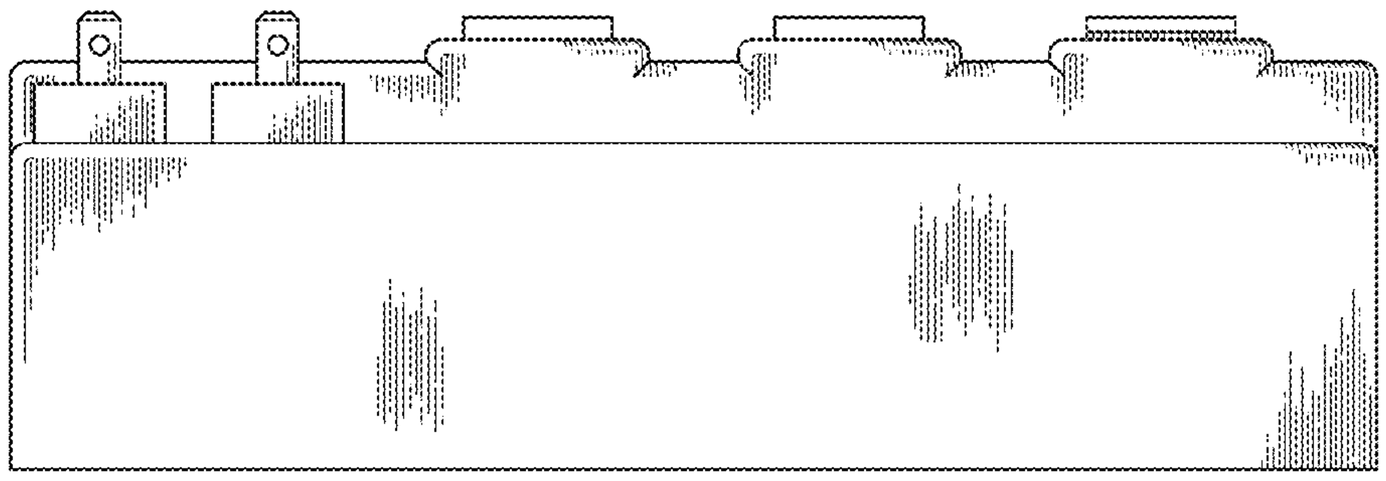

Fig.1

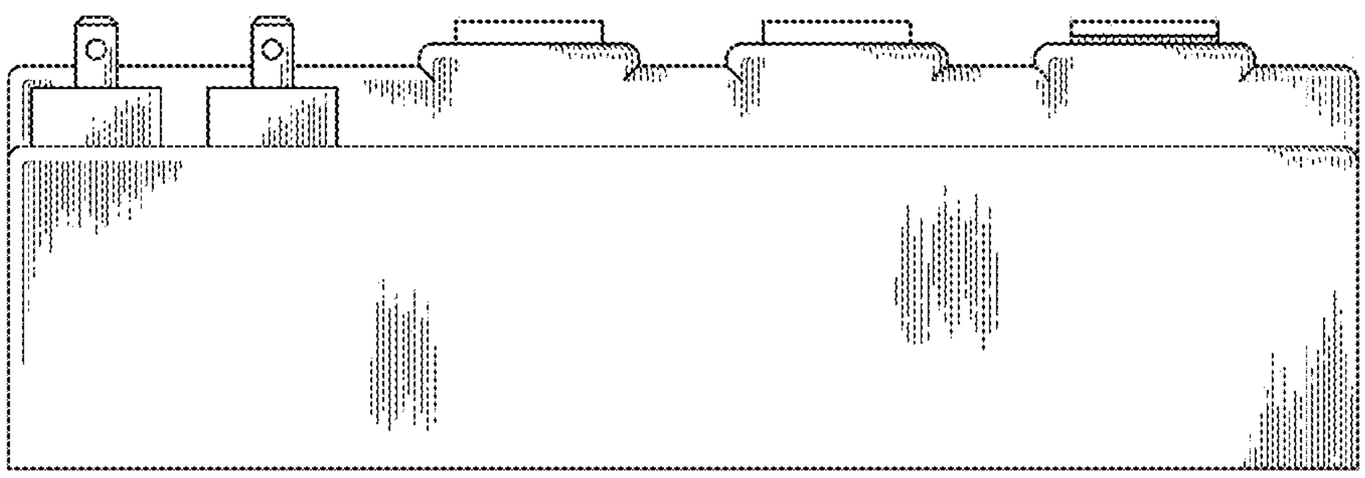

Fig.2

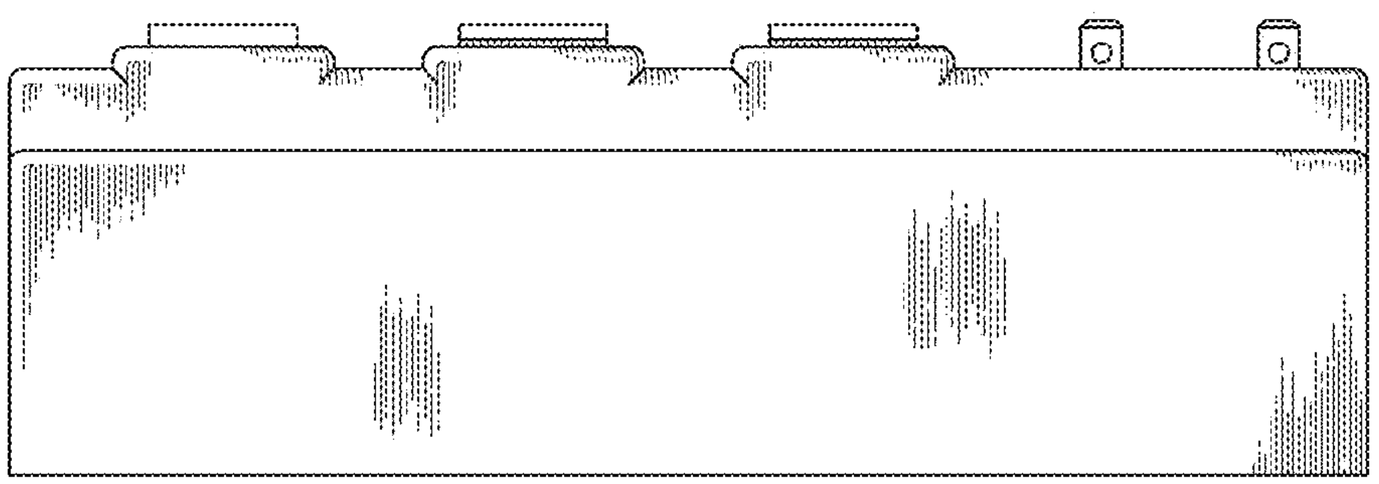

Fig.3

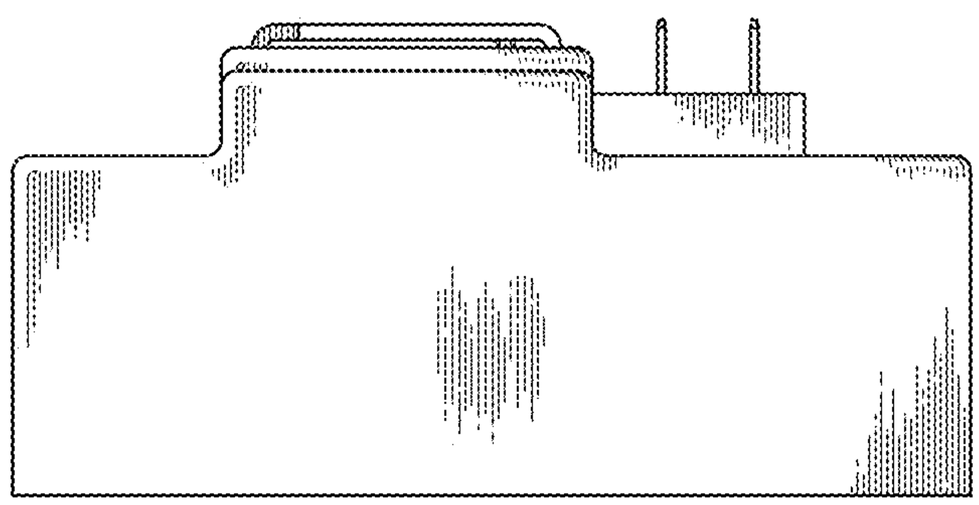

Fig.4

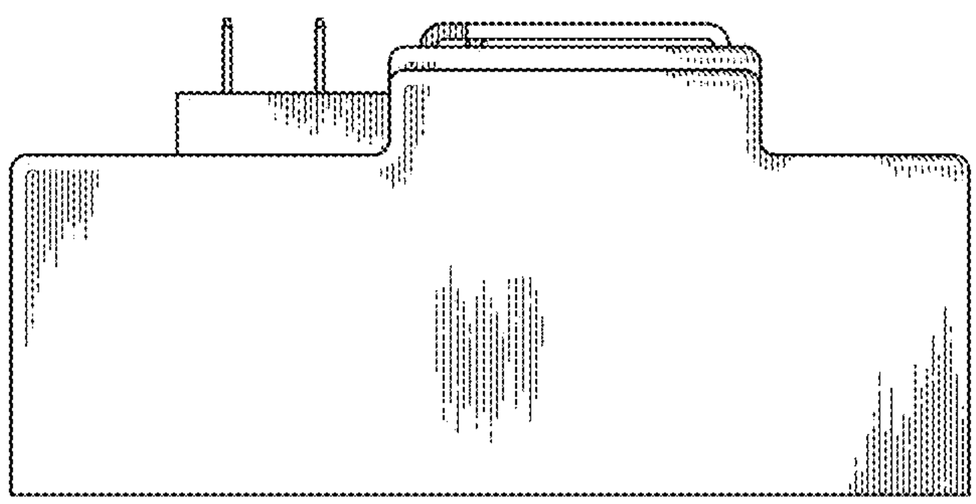

Fig.5

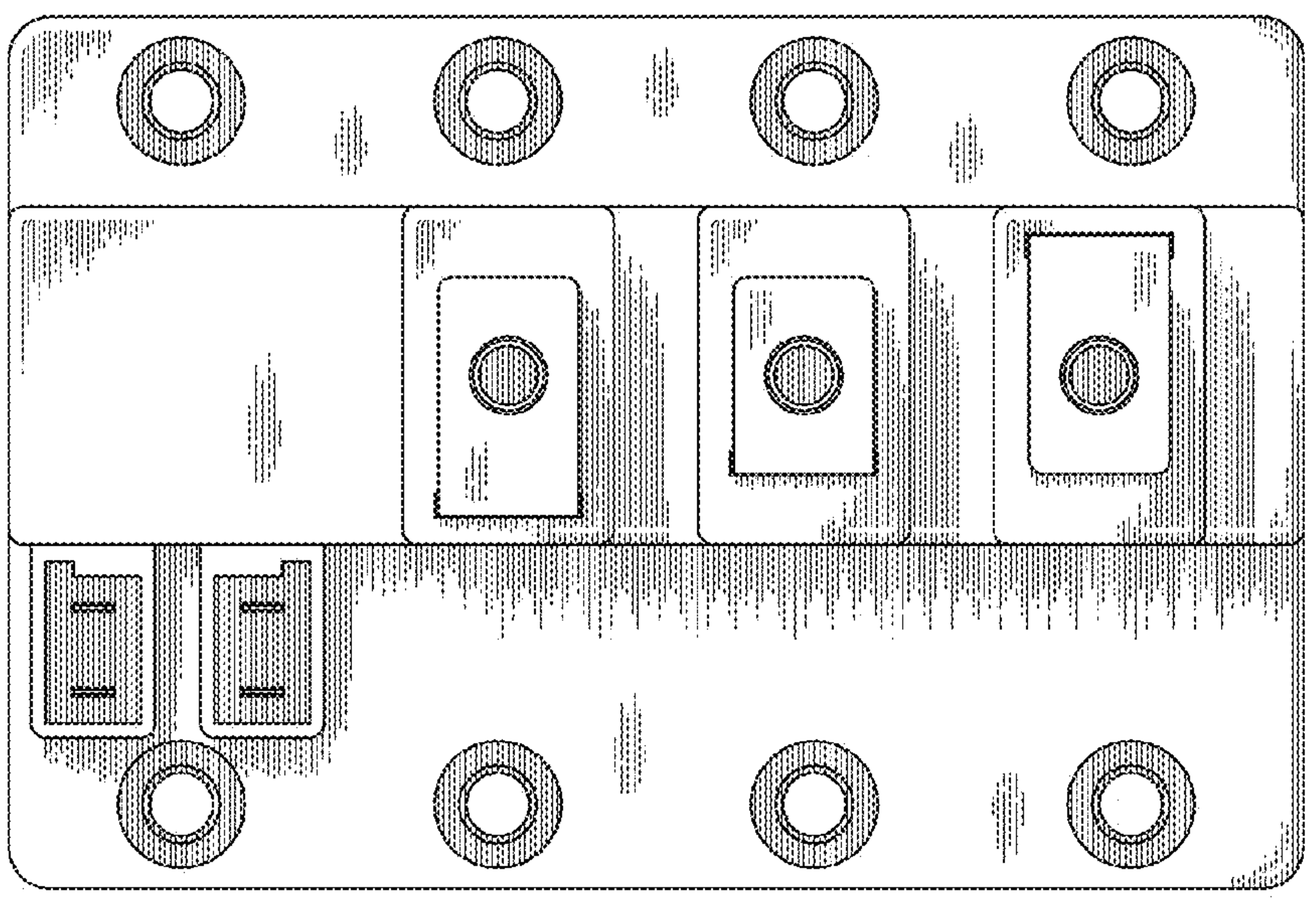

Fig.6

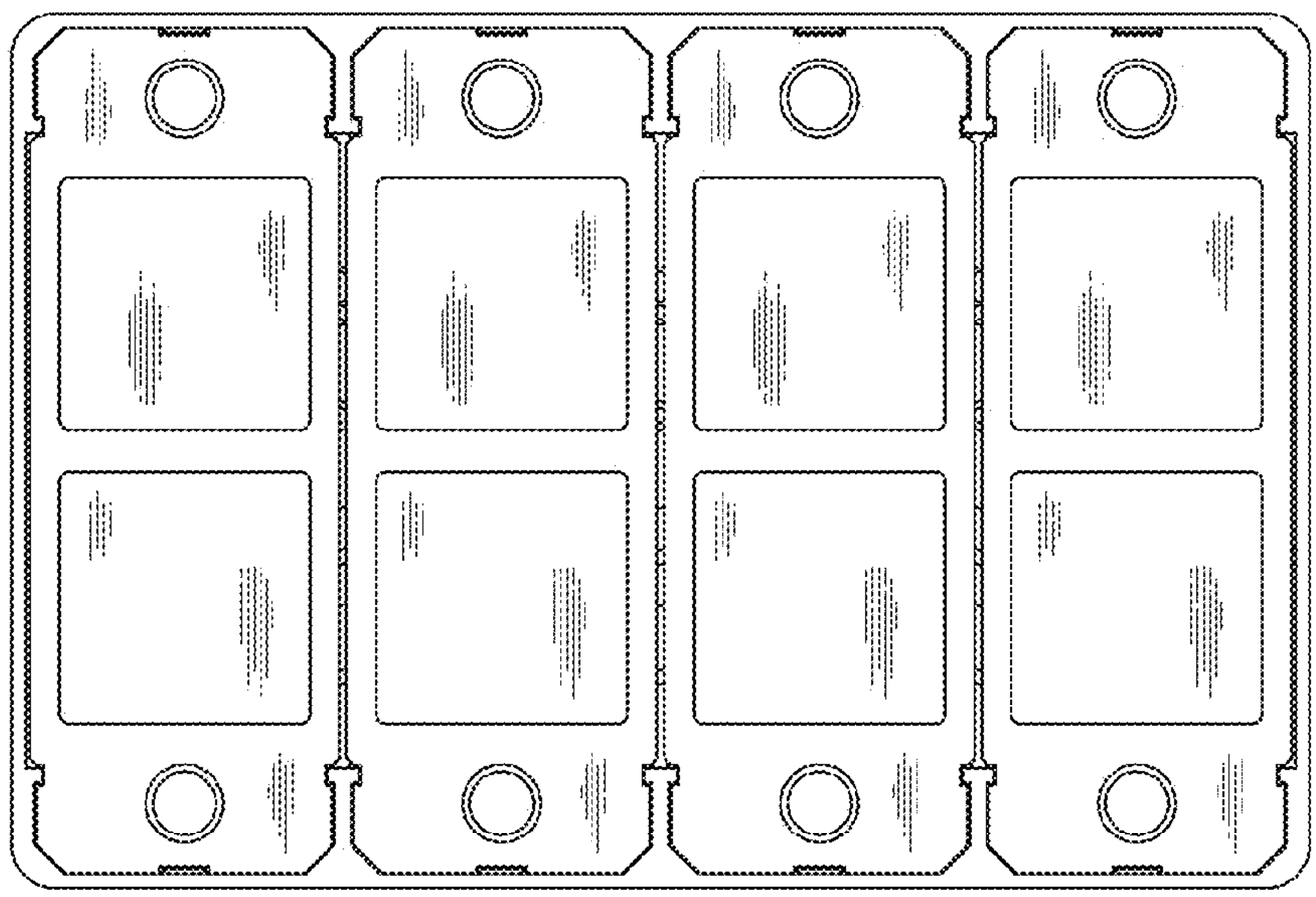

Fig.7