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(12) **United States Design Patent**
Chen et al.

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(54) **SEMICONDUCTOR DEVICE**

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(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (10) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/182**

(58) **Field of Classification Search**
USPC D13/110, 182; 257/668, 678, 690;
361/713, 679.01, 728, 736, 760, 761,
361/775, 820; 324/71.5, 252; 174/250, 253;
438/64, 65, 66
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D357,672 S *	4/1995	Terasawa et al.	D13/182
D364,383 S *	11/1995	Yamada et al.	D13/182
D364,384 S *	11/1995	Shimizu et al.	D13/182
D432,096 S *	10/2000	Jeon et al.	D13/182
D441,726 S *	5/2001	Sofue et al.	D13/182
D470,825 S *	2/2003	Iwasaki et al.	D13/182
6,521,983 B1 *	2/2003	Yoshimatsu et al.	257/678
D476,959 S *	7/2003	Yamada et al.	D13/182
D539,761 S *	4/2007	Takahashi et al.	D13/182

D548,202 S *	8/2007	Takahashi	D13/182
D548,203 S *	8/2007	Takahashi	D13/182
D587,662 S *	3/2009	Soutome et al.	D13/182
D589,012 S *	3/2009	Soyano et al.	D13/182
D648,290 S *	11/2011	Mori	D13/182
D653,633 S *	2/2012	Soyano	D13/182
D653,634 S *	2/2012	Soyano	D13/182

(Continued)

OTHER PUBLICATIONS

U.S. Appl. No. 29/458,663, filed Jun. 21, 2013.

(Continued)

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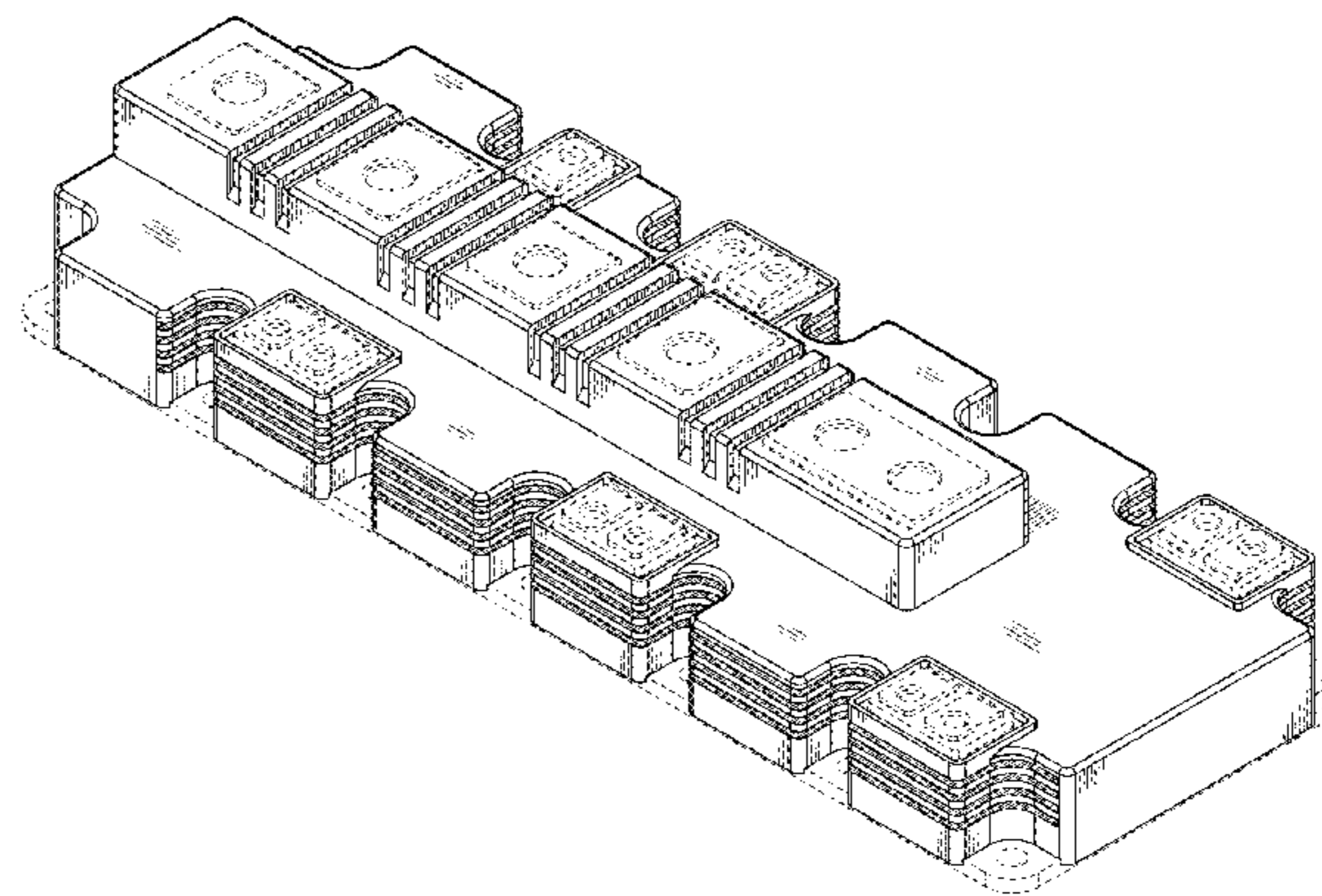
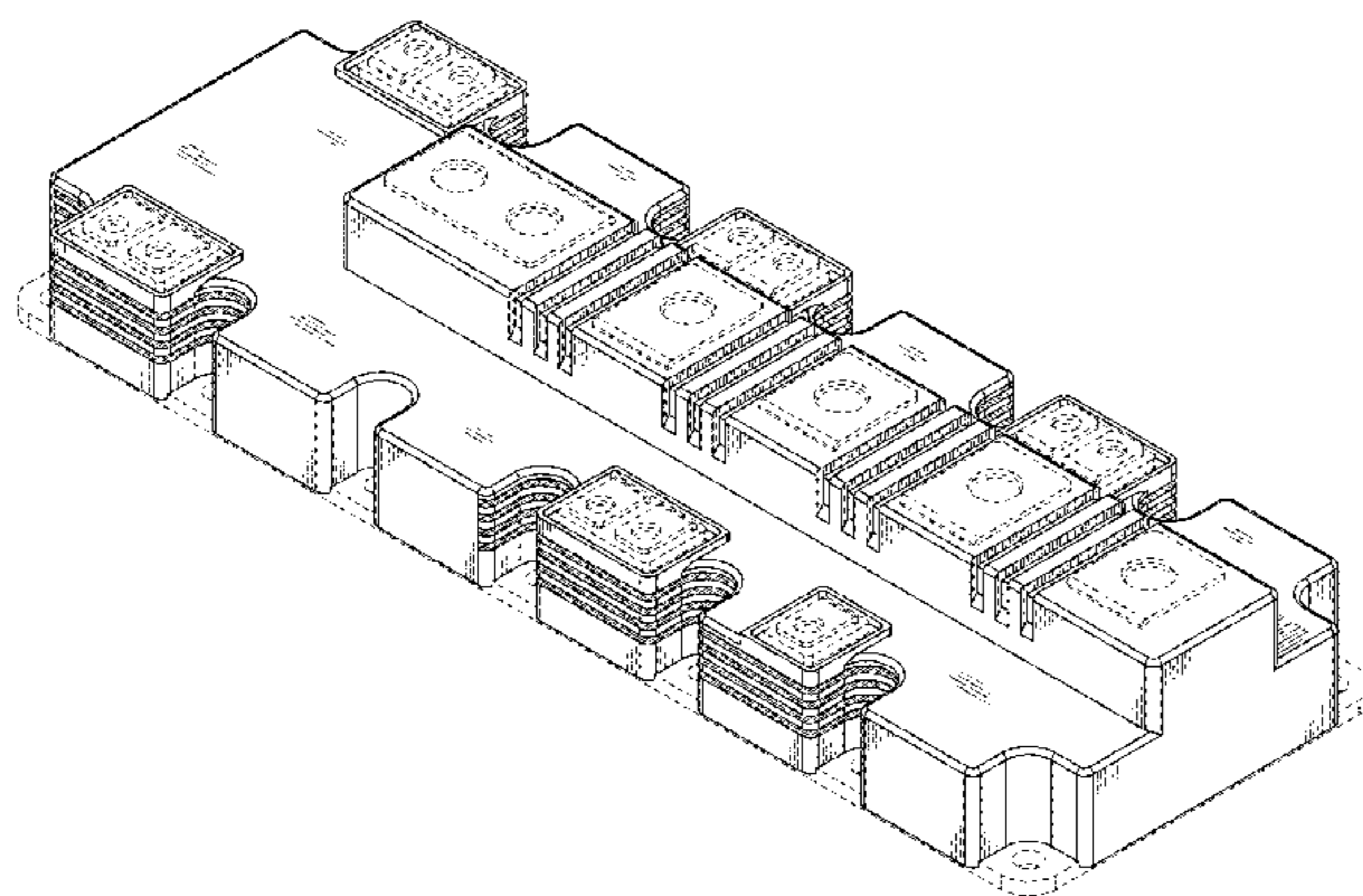
(57) **CLAIM**

The ornamental design for a semiconductor device, as shown and described.

DESCRIPTION

FIG. 1 is a front view of a semiconductor device showing our new design;
FIG. 2 is a rear view of the semiconductor device of FIG. 1;
FIG. 3 is a left side view of the semiconductor device of FIG. 1;
FIG. 4 is a right side view of the semiconductor device of FIG. 1;
FIG. 5 is a top view of the semiconductor device of FIG. 1;
FIG. 6 is a bottom view of the semiconductor device of FIG. 1;
FIG. 7 is a top, front and right side perspective view of the semiconductor device of FIG. 1; and,
FIG. 8 is a top, rear and left side perspective view of the semiconductor device of FIG. 1.
The broken lines shown in the drawings represent portions of the semiconductor device that form no part of the claimed design.

1 Claim, 8 Drawing Sheets



(56)

References Cited

OTHER PUBLICATIONS

U.S. PATENT DOCUMENTS

D673,922	S *	1/2013	Moriai et al.	D13/182
D686,174	S *	7/2013	Soyano	D13/182
D689,446	S *	9/2013	Soyano	D13/180
2001/0038143	A1 *	11/2001	Sonobe et al.	257/690
2011/0044012	A1 *	2/2011	Matsumoto	361/728

U.S. Appl. No. 29/458,665, filed Jun. 21, 2013.

U.S. Appl. No. 29/458,667, filed Jun. 21, 2013.

U.S. Appl. No. 29/458,669, filed Jun. 21, 2013.

* cited by examiner

Fig. 1

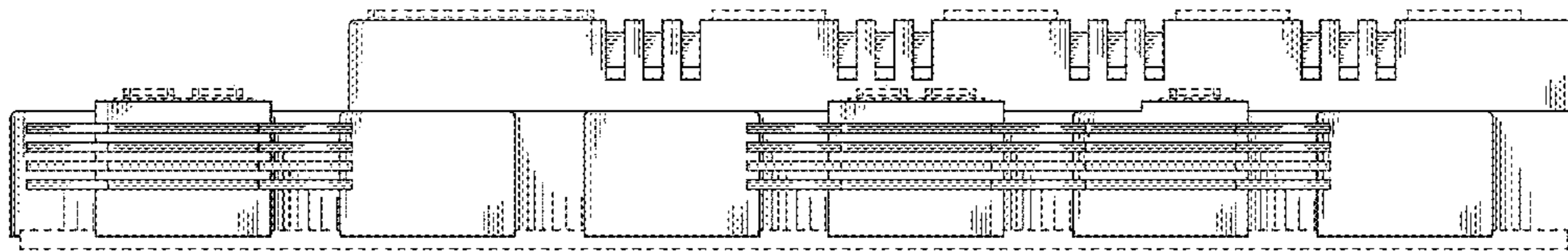


Fig. 2

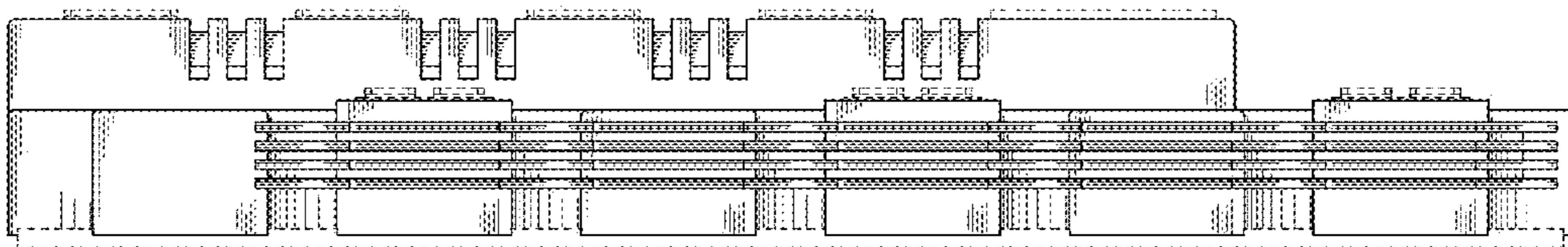


Fig. 3

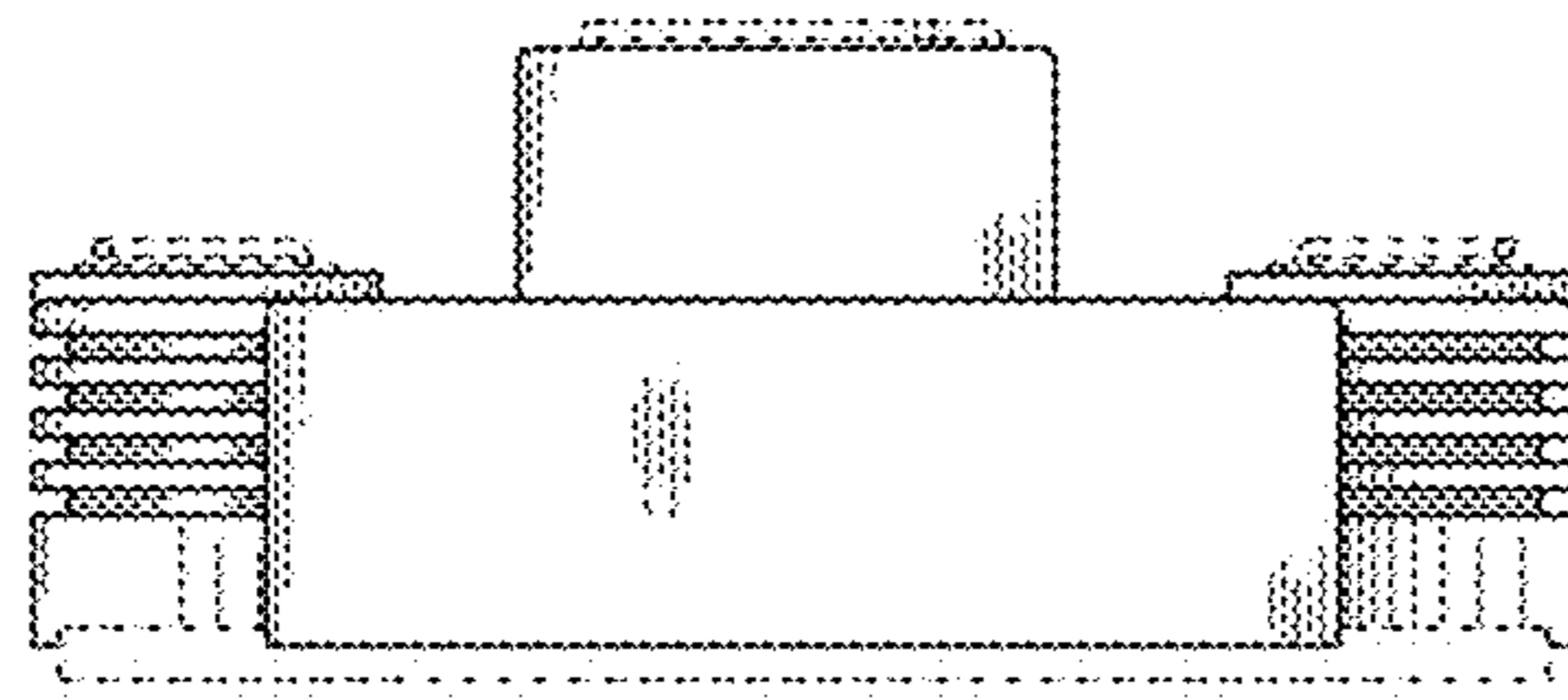


Fig. 4

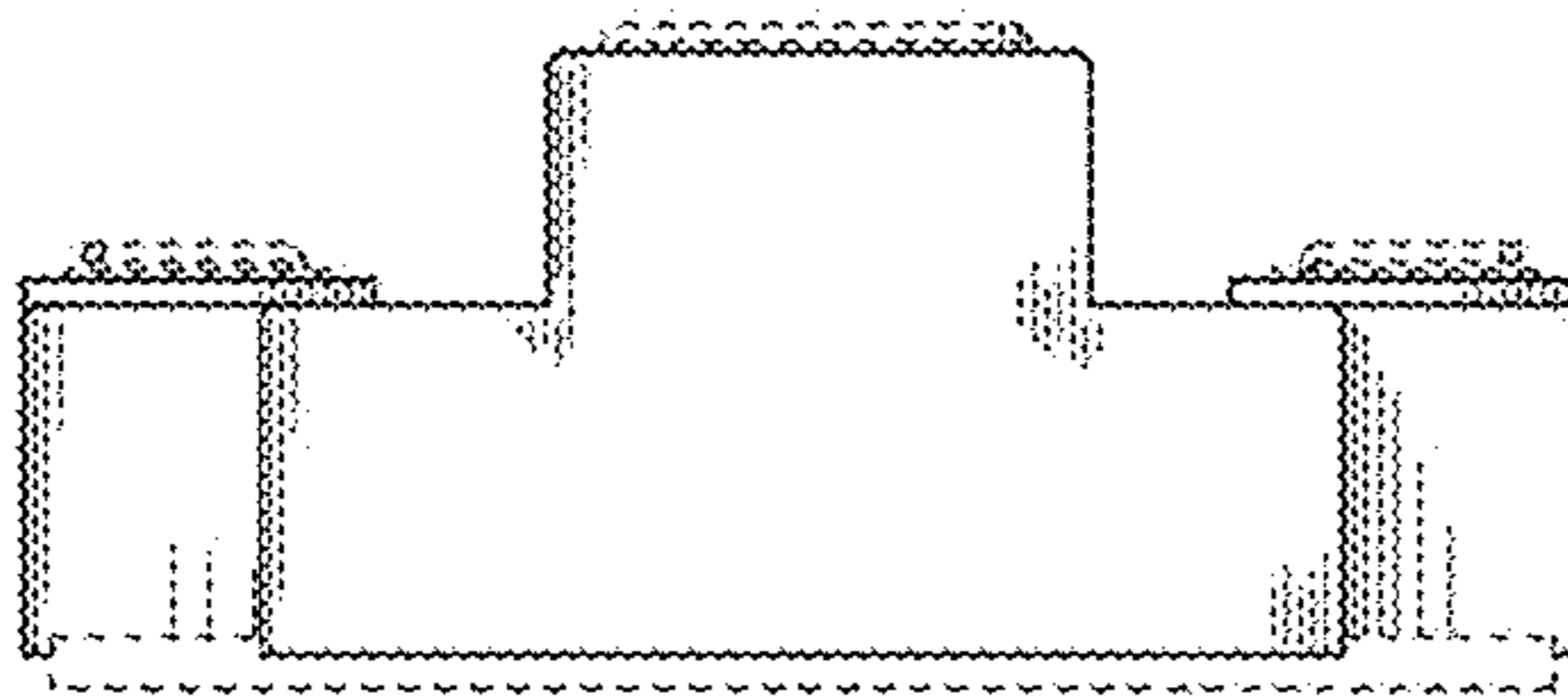


Fig. 5

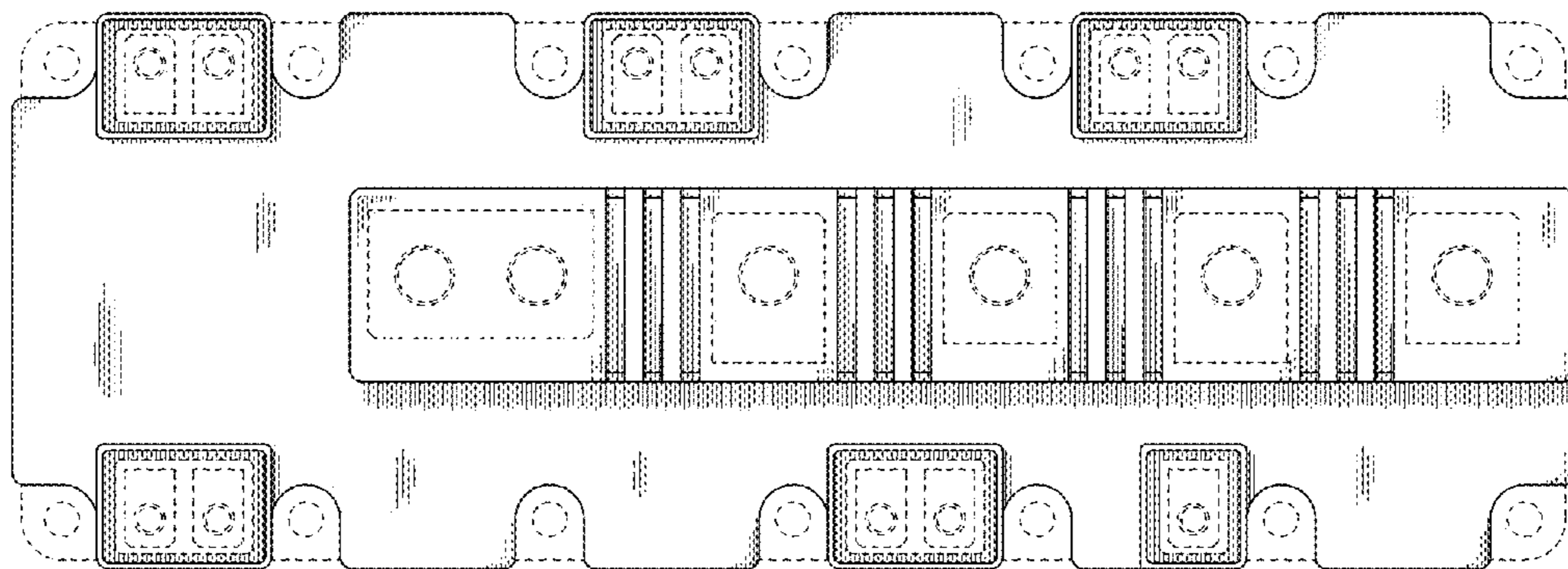


Fig. 6

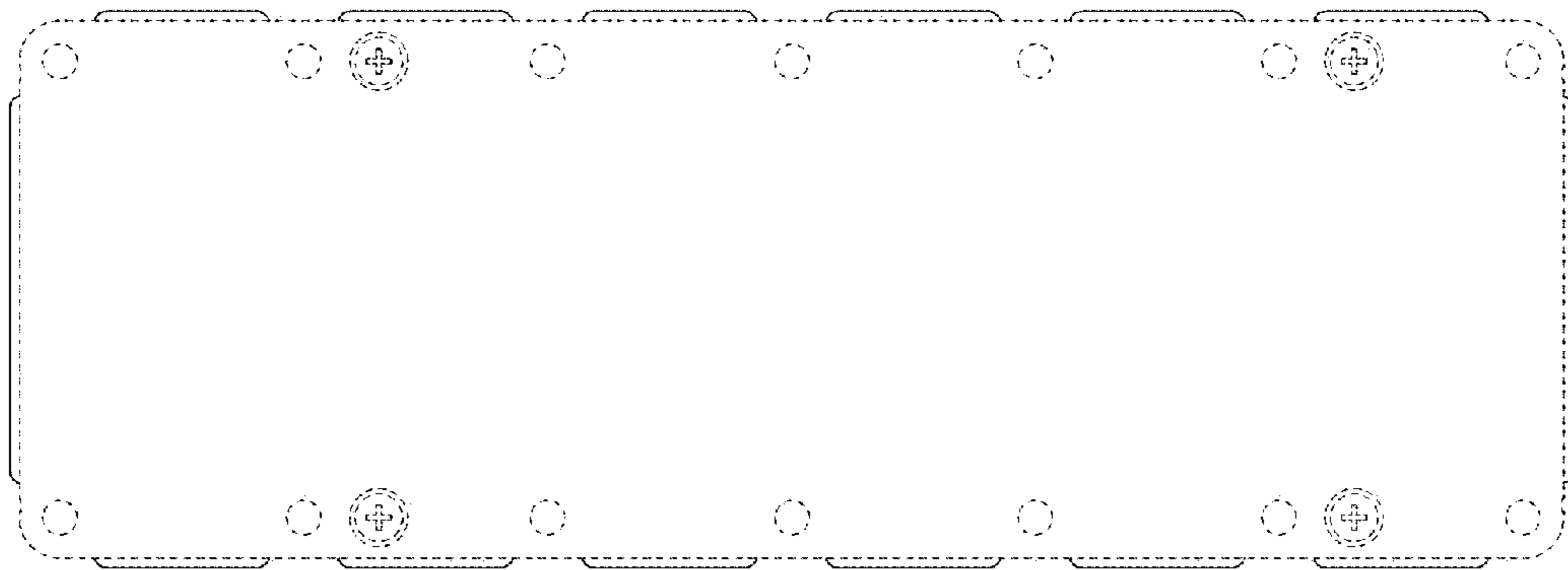


Fig. 7

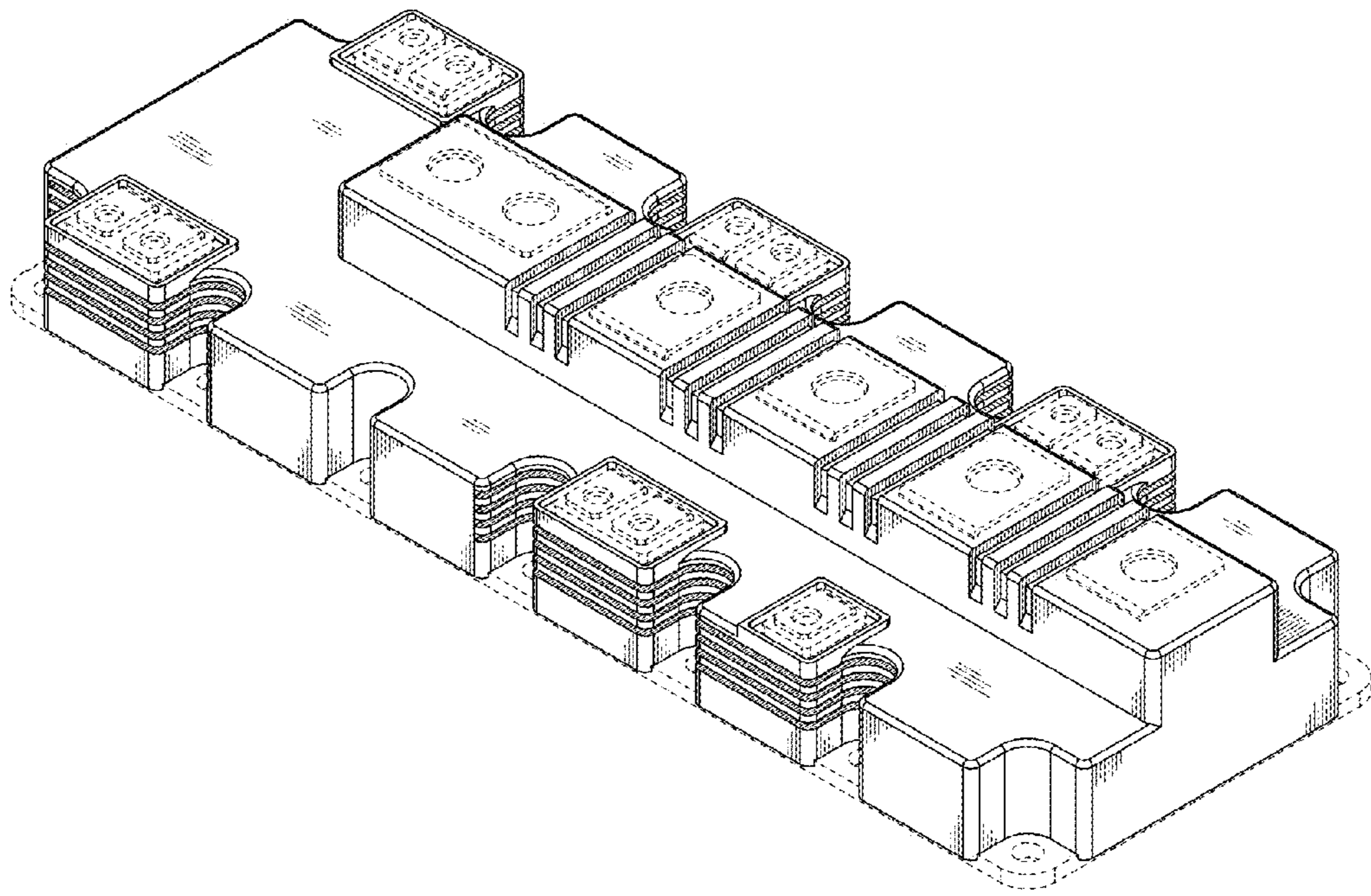


Fig.8

