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(12) United States Design Patent

Matsumoto et al.

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(54) **BAFFLE PLATE FOR MANUFACTURING SEMICONDUCTOR**

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(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/416,088**

(22) Filed: **Mar. 19, 2012**

(30) **Foreign Application Priority Data**

Sep. 20, 2011 (JP) D2011-021504

(51) **LOC (9) Cl.** **15-99**

(52) **U.S. Cl.**
USPC **D15/144**; D15/138

(58) **Field of Classification Search**
USPC D13/182; D15/138, 144, 199; 118/723; 156/345, 345.36, 345.41, 345.48; 204/298.06, 298.08, 298.11, 298.34; 336/232
See application file for complete search history.

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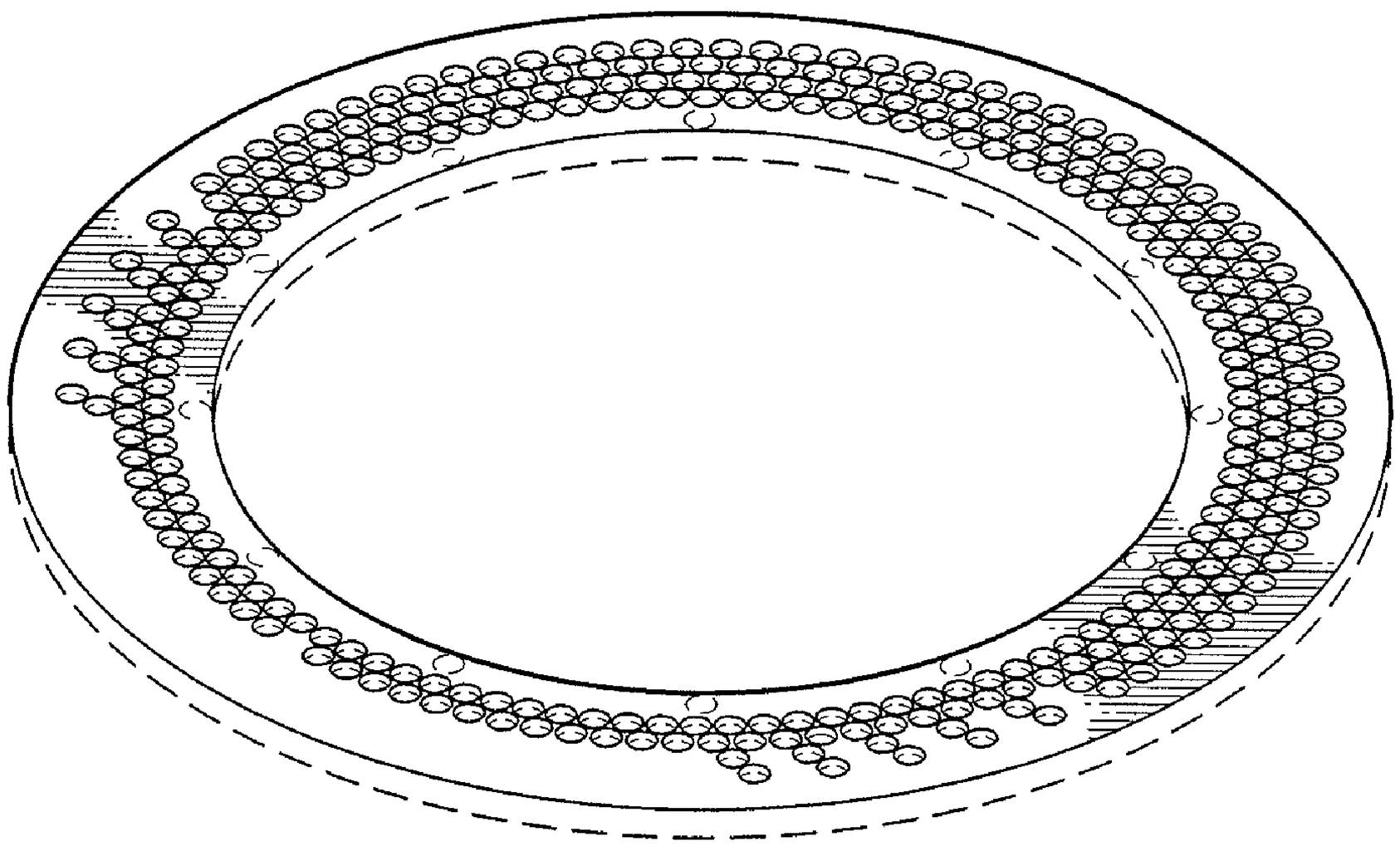
(57) **CLAIM**

The ornamental design for a baffle plate for manufacturing semiconductor, as shown and described.

DESCRIPTION

FIG. **1** is a front view of a baffle plate of the present invention.
FIG. **2** is a rear view of the baffle plate of FIG. **1**.
FIG. **3** is a top plan view of the baffle plate of FIG. **1**.
FIG. **4** is a bottom view of the baffle plate of FIG. **1**.
FIG. **5** is a right side view of the baffle plate of FIG. **1**.
FIG. **6** is a left view of the baffle plate of FIG. **1**.
FIG. **7** is a perspective view of the baffle plate of FIG. **1**; and,
FIG. **8** is a view of the baffle plate of FIG. **1** in use, wherein, for example, in a plasma processing device, gas entering a chamber is ionized, and a wafer is treated by an etching process with ions, and gas is exhausted from the chamber.
The features shown in broken lines depict environmental subject matter only and form no part of the claimed design.

1 Claim, 4 Drawing Sheets



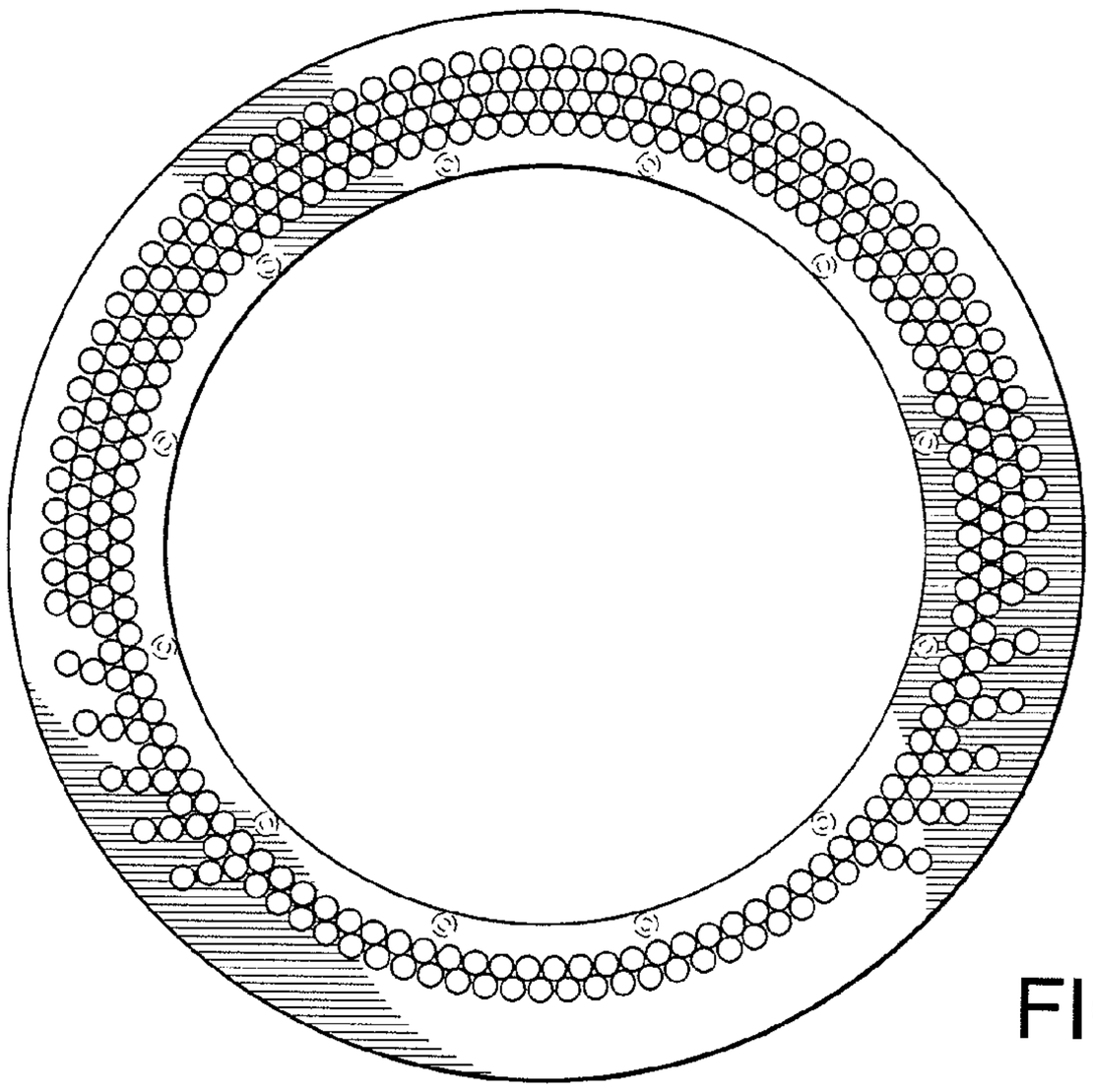


FIG. 1

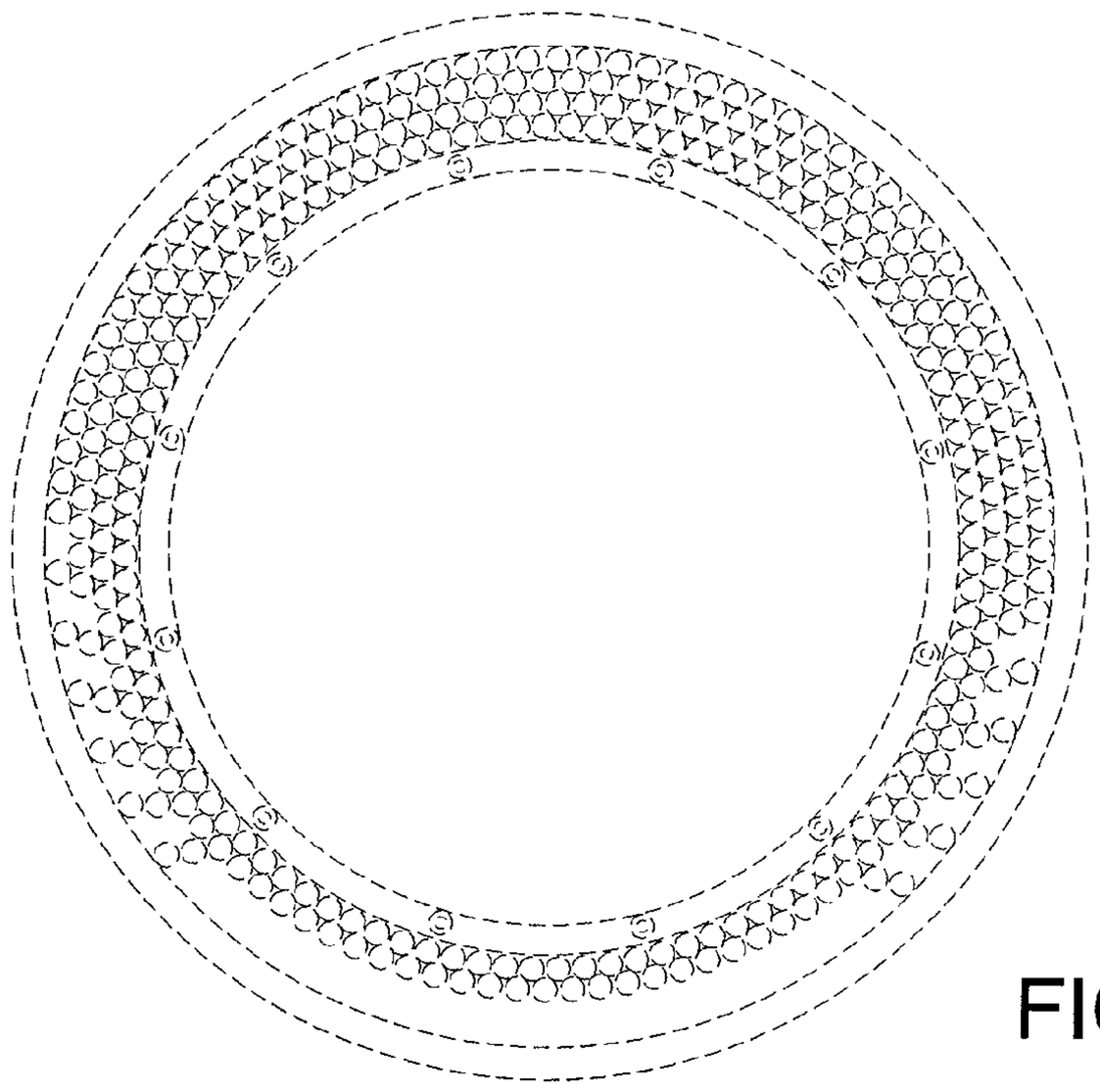


FIG. 2

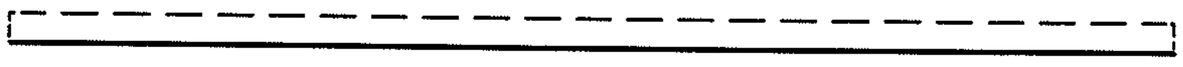


FIG. 3

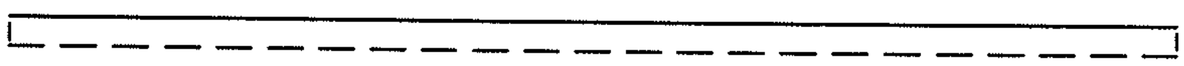


FIG. 4

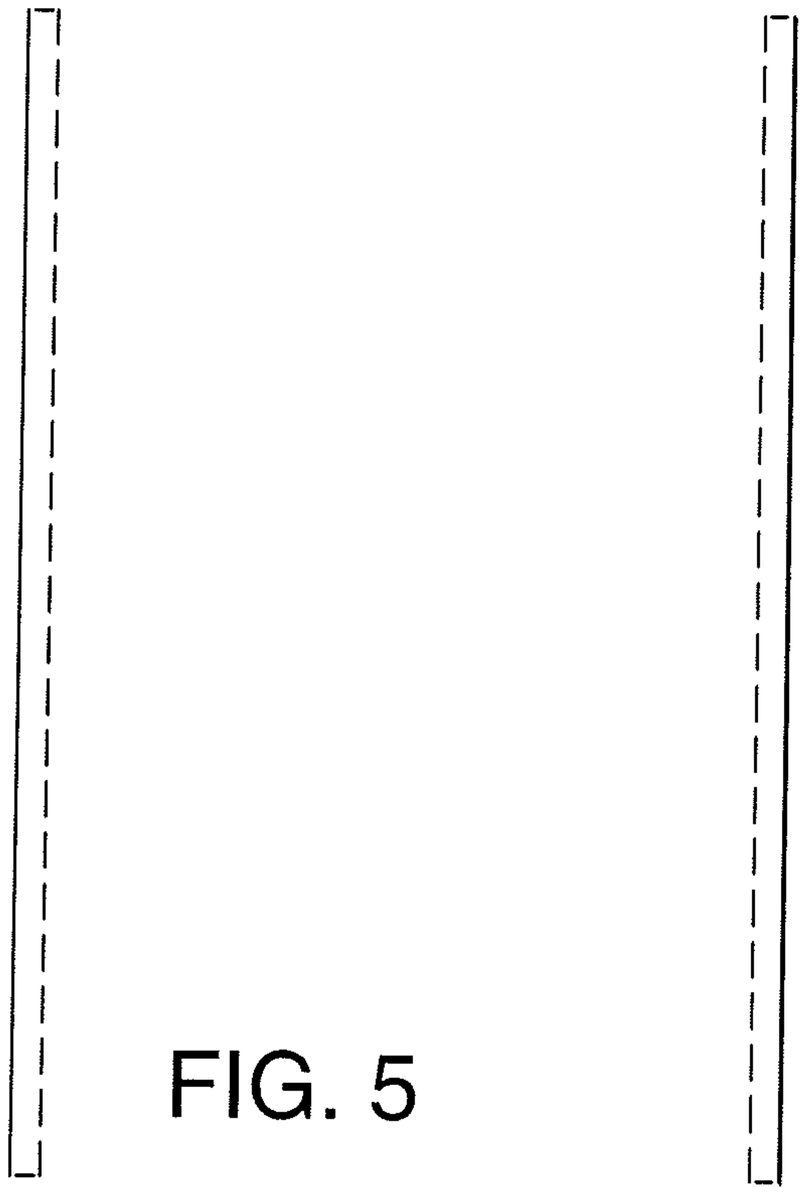


FIG. 5

FIG. 6

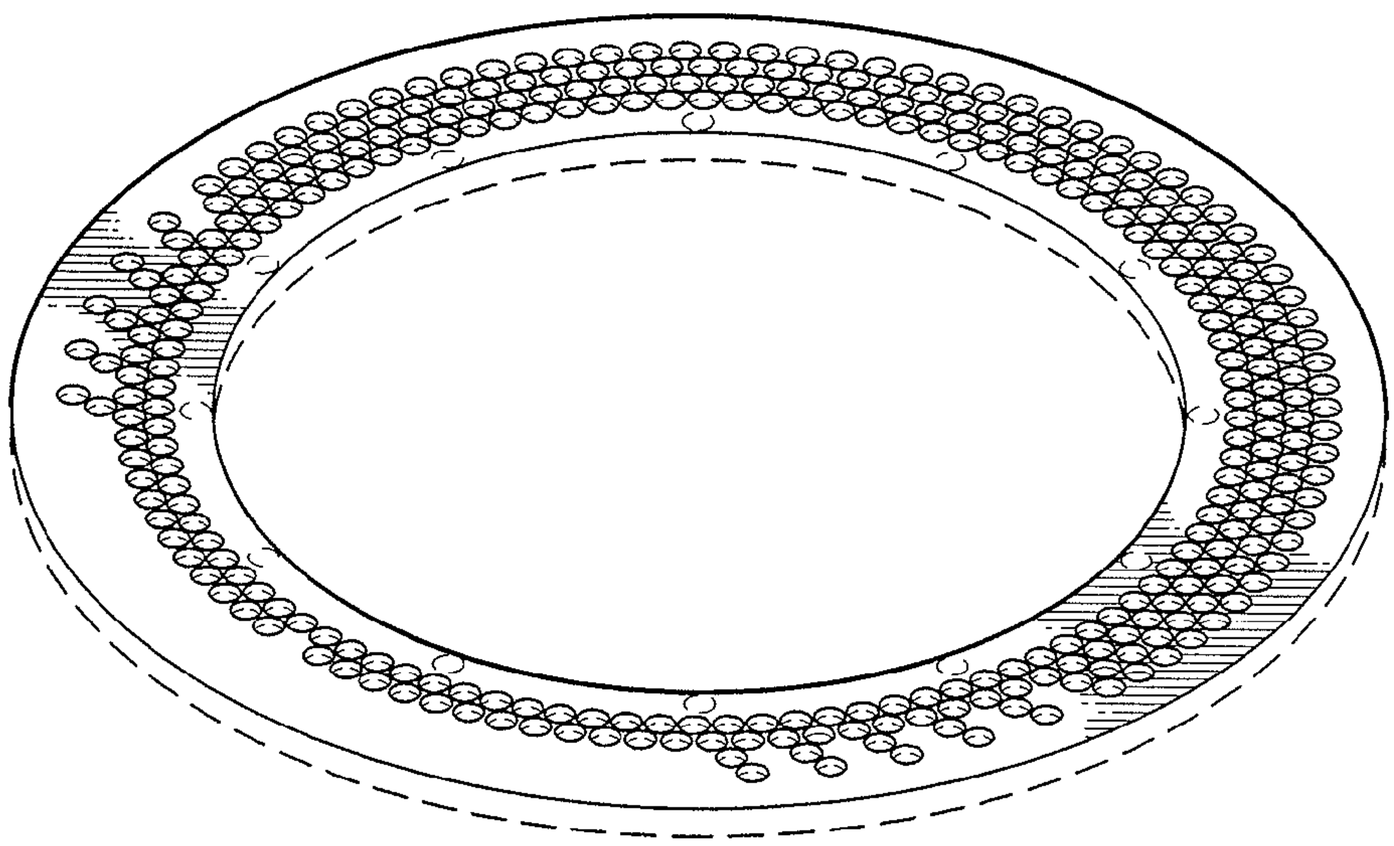


FIG. 7

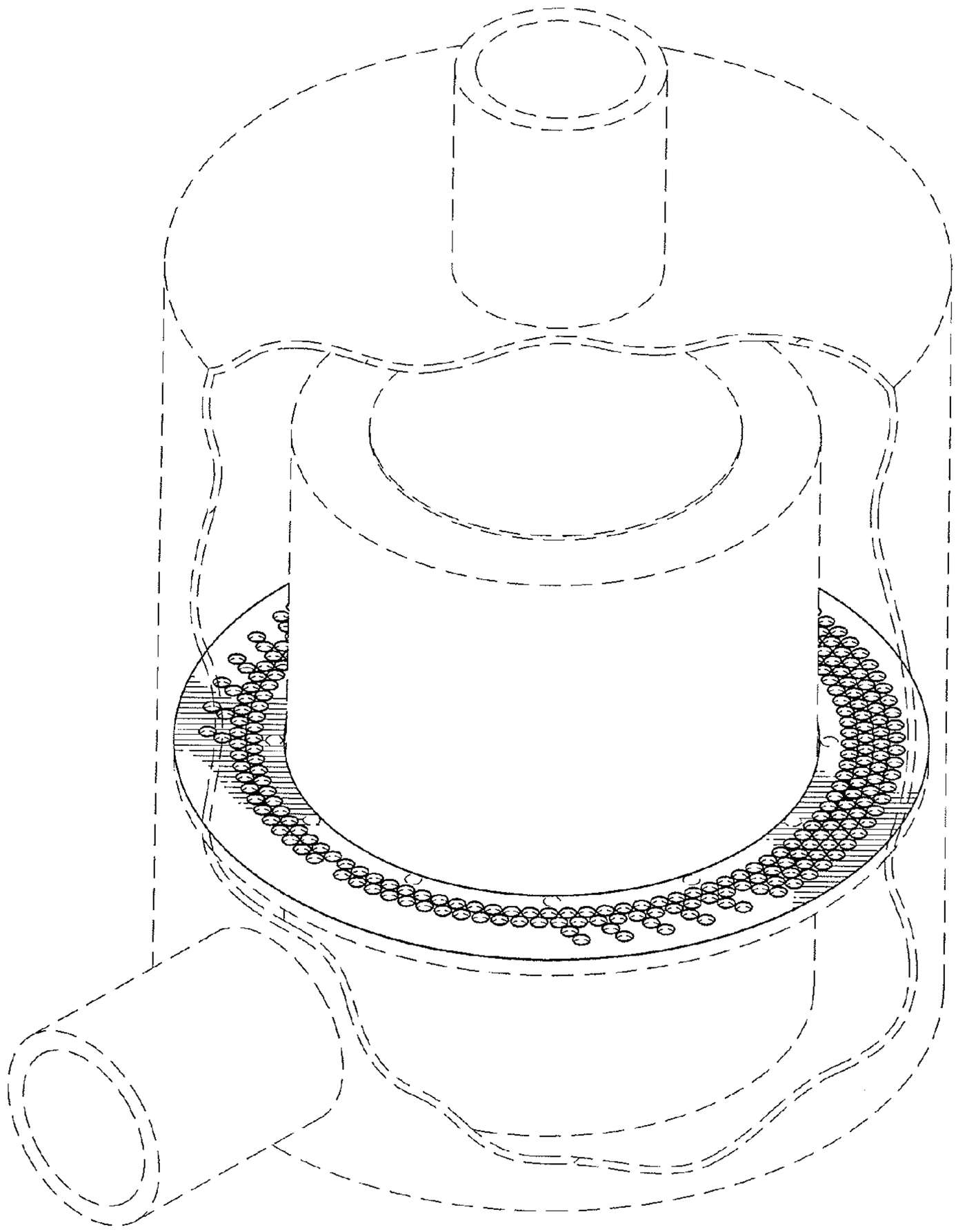


FIG. 8