US00D684130S

(12) United States Design Patent

Vincent et al.

(10) Patent No.: US D684,130 S
(45) Date of Patent: ** Jun. 11, 2013

(54) **ELECTRONICS ENCLOSURE**

(75) Inventors: **Laith Anthony Vincent**, Charlottesville, VA (US); **Kenneth Wayne Crawford**, Charlottesville, VA (US); **Vinson R Epperson**, Ruckersville, VA (US)

(73) Assignee: **GE Intelligent Platforms, Inc.**, Charlottesville, VA (US)

(**) Term: **14 Years**

(21) Appl. No.: **29/422,058**

(22) Filed: **May 16, 2012**

(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.**
USPC **D13/184**

(58) **Field of Classification Search**
USPC D14/300, 301, 308, 314, 348, 349–356, D14/358; D13/162, 184, 199; 312/223.1–223.2; 360/99.01–99.12; 369/34.01, 36.01; 361/679.01, 679.6, 679.22; 345/173
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,933,928	B1 *	8/2005	Lilienthal	345/173
D512,059	S *	11/2005	Zhang et al.	D14/348
D520,519	S *	5/2006	Chin et al.	D14/203.3
D563,994	S *	3/2008	Liu et al.	D14/496
D580,933	S *	11/2008	Ju et al.	D14/358
D594,876	S *	6/2009	Hwang	D14/496
D618,232	S *	6/2010	O'Neil et al.	D14/314
D620,953	S *	8/2010	Andre et al.	D14/496
D624,912	S *	10/2010	Chen et al.	D14/356
2008/0062636	A1 *	3/2008	Liu	361/685

* cited by examiner

Primary Examiner — Freda S Nunn
(74) *Attorney, Agent, or Firm* — Global Patent Operation; Mark A. Conklin

(57) **CLAIM**

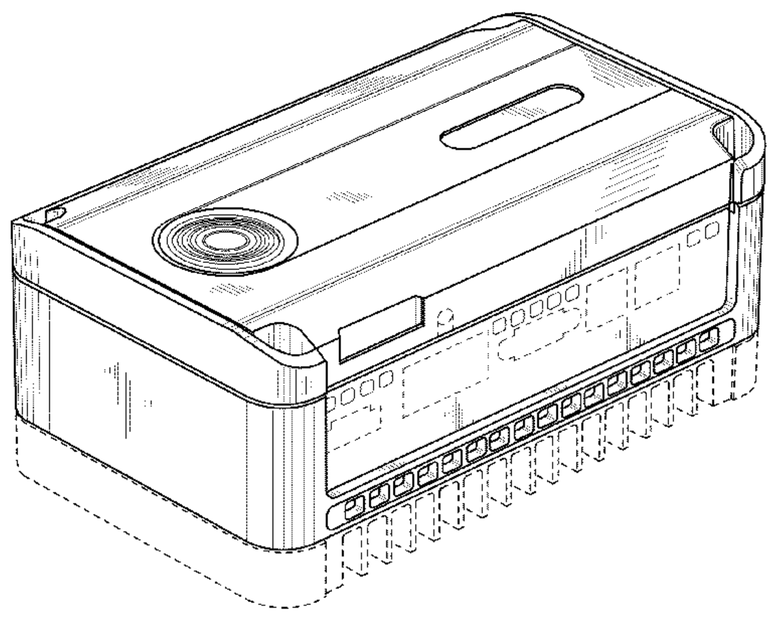
The ornamental design for an electronics enclosure, as shown and described.

DESCRIPTION

FIG. **1** is a perspective view of our design;
FIG. **2** is a top plan view of the embodiment of FIG. **1**;
FIG. **3** is a side elevational view of the embodiment of FIG. **1**, the opposite side being a mirror image thereof;
FIG. **4** is a front elevational view of the embodiment of FIG. **1**;
FIG. **5** is a back view of the embodiment of FIG. **1**;
FIG. **6** is a perspective view of a second embodiment of our design;
FIG. **7** is a top plan view of the embodiment of FIG. **6**;
FIG. **8** is a side elevational view of the embodiment of FIG. **6**, the opposite side being a mirror image thereof;
FIG. **9** is a front view of the embodiment of FIG. **6**;
FIG. **10** is a back view of the embodiment of FIG. **6**;
FIG. **11** is a perspective view of a third embodiment of our design;
FIG. **12** is a top plan view of the embodiment of FIG. **11**;
FIG. **13** is a side elevational view of the embodiment of FIG. **11**, the opposite side being a mirror image thereof;
FIG. **14** is a front view of the embodiment of FIG. **11**; and,
FIG. **15** is a back view of the embodiment of FIG. **11**.

Broken lines shown in the drawings illustrate portions of the electronics enclosure, and form no part of the claimed design.

1 Claim, 9 Drawing Sheets



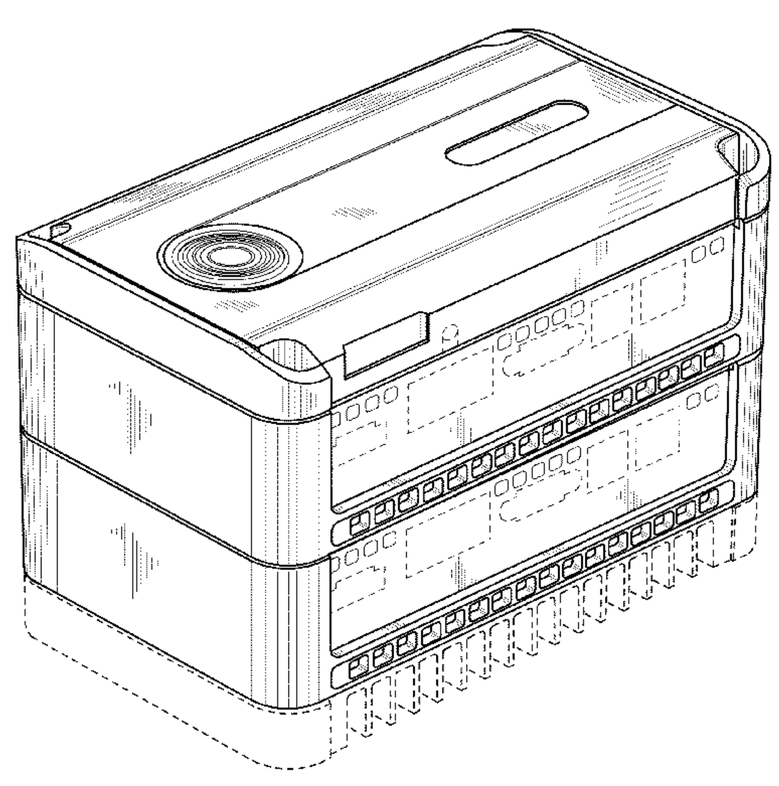


Figure 1

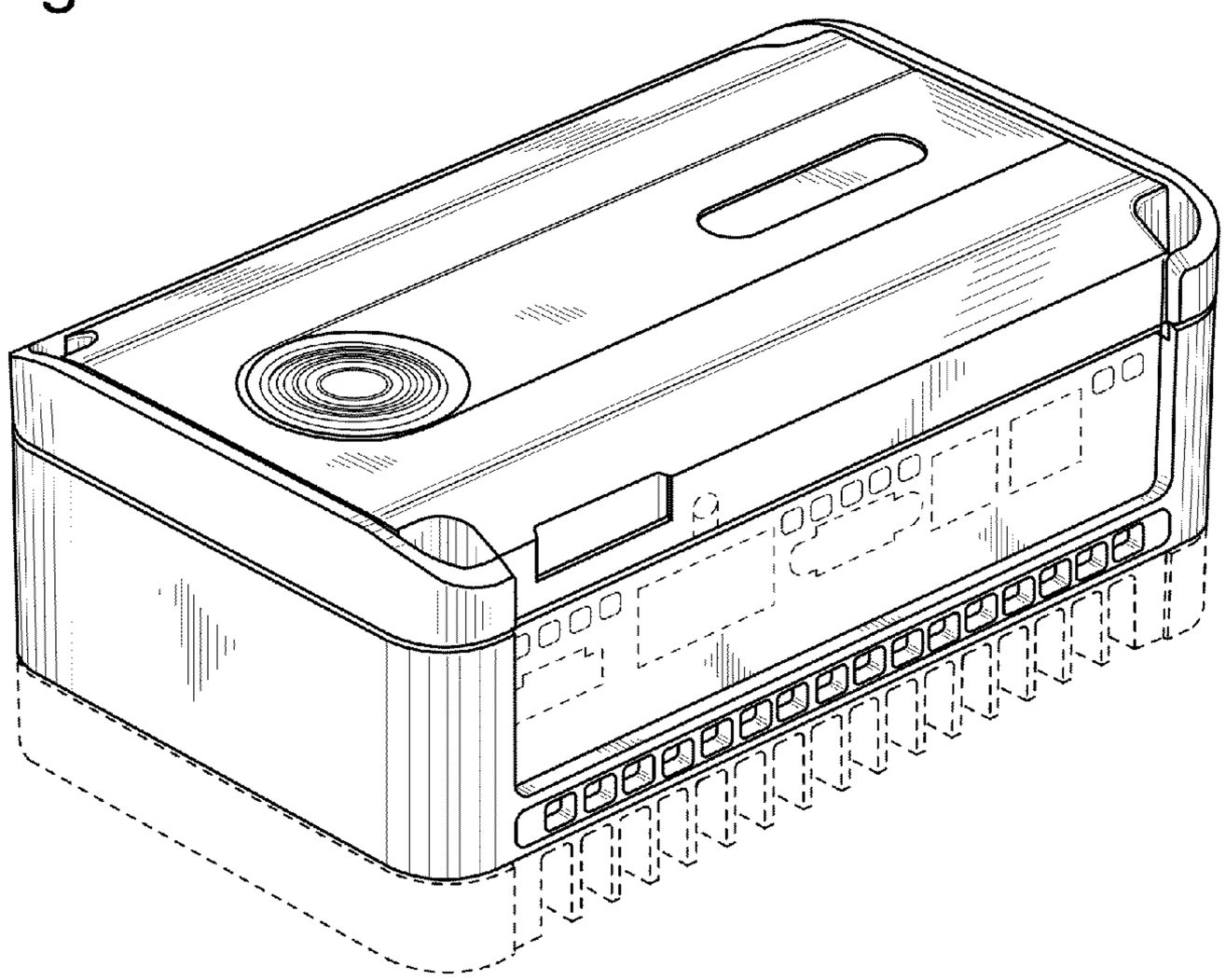


Figure 2

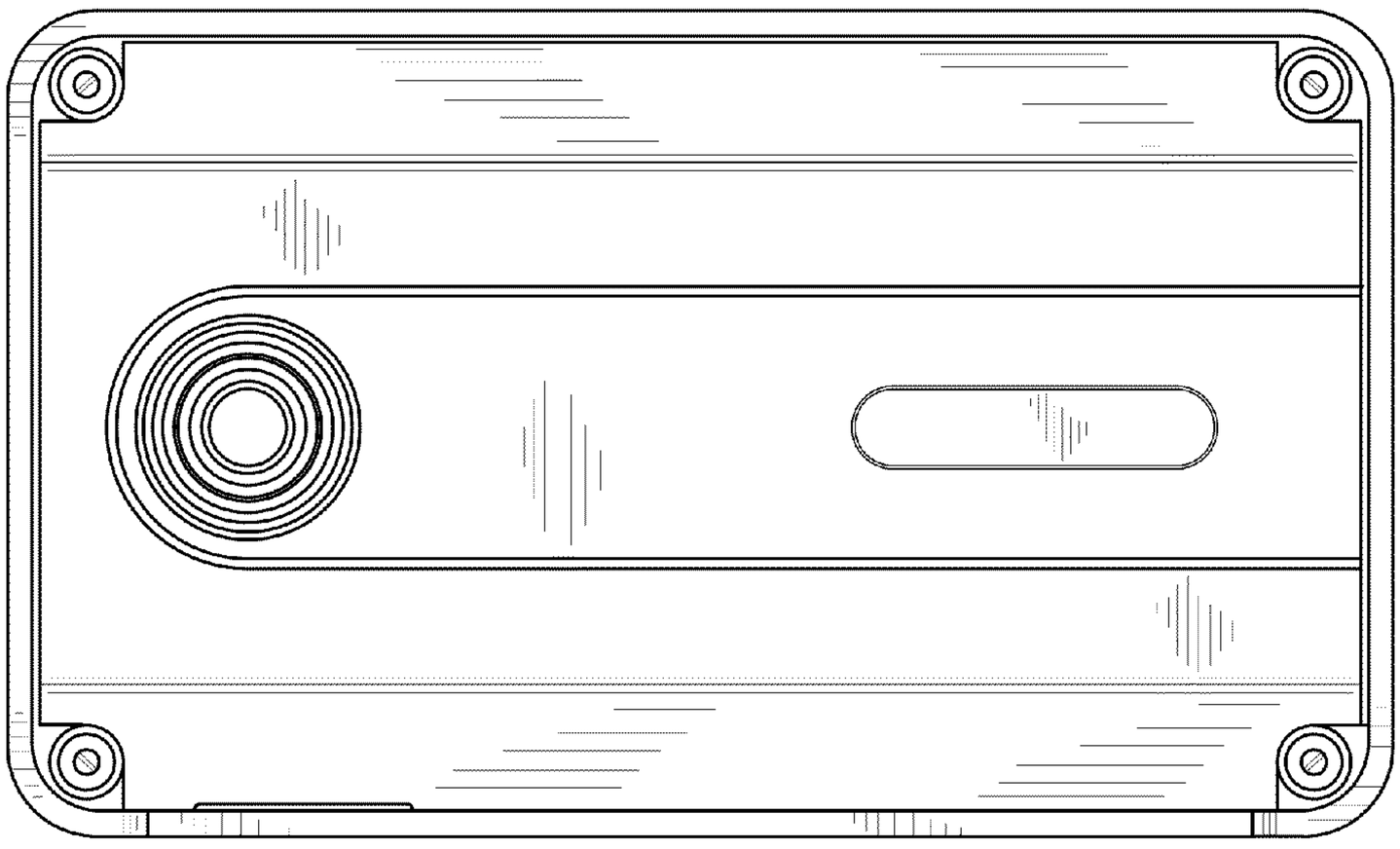
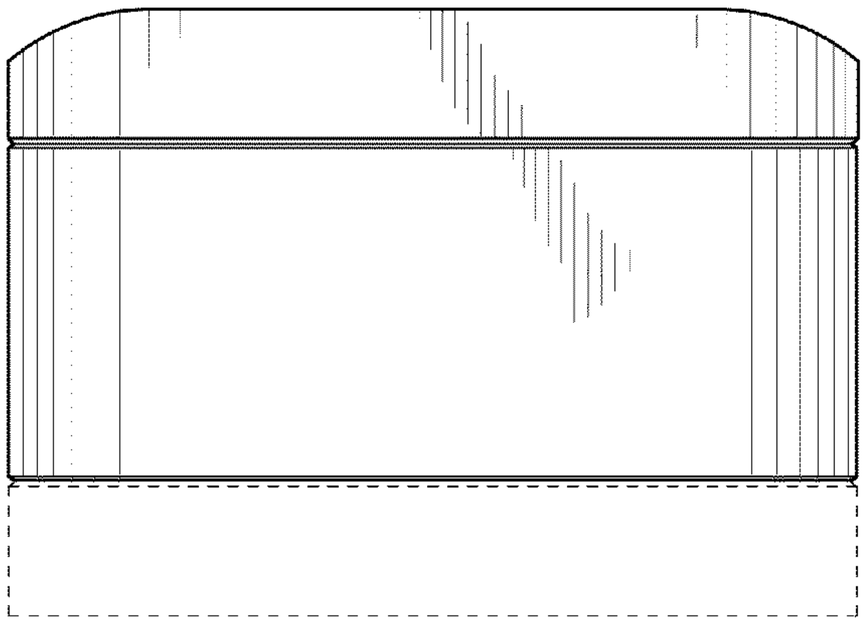


Figure 3



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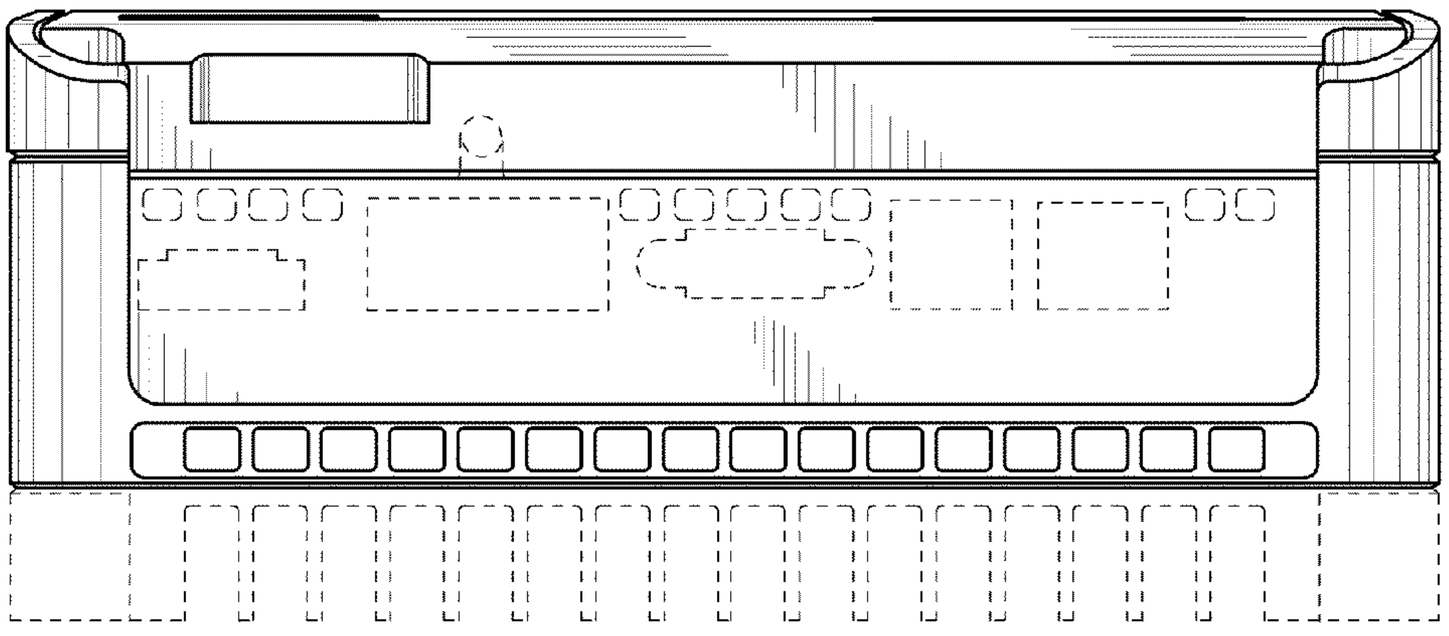

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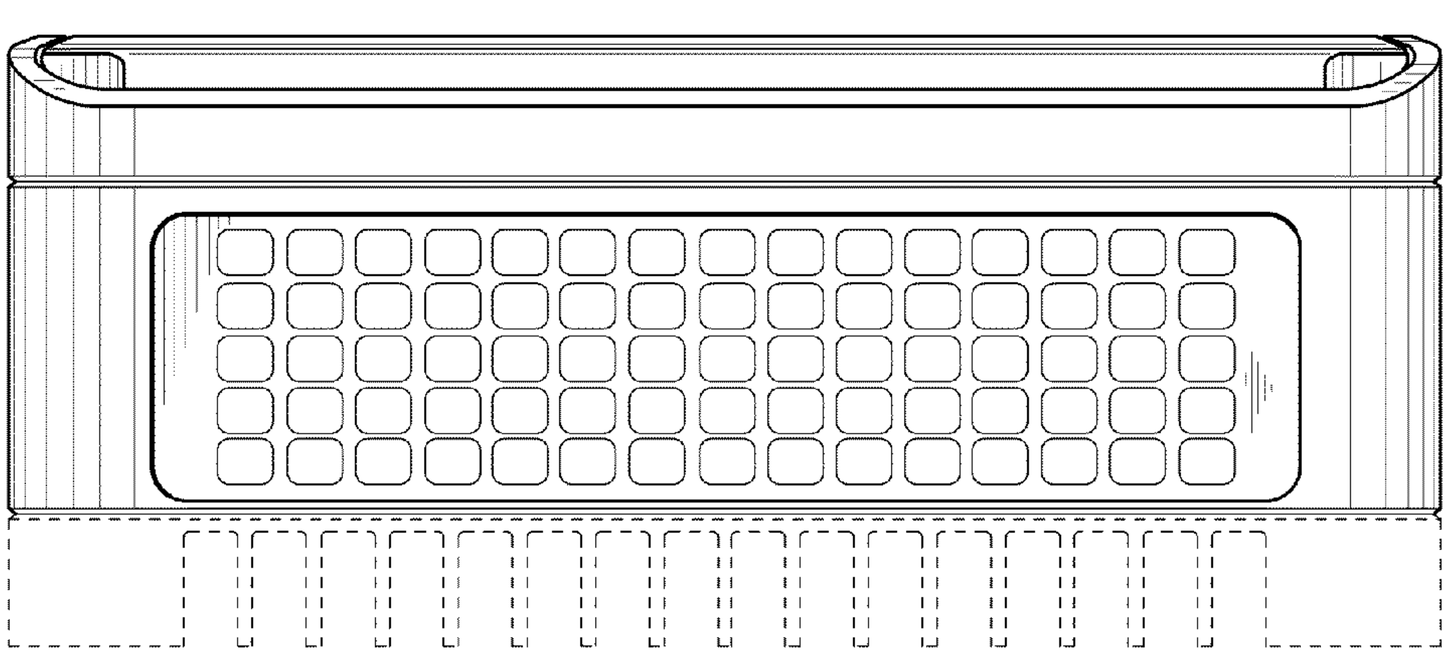

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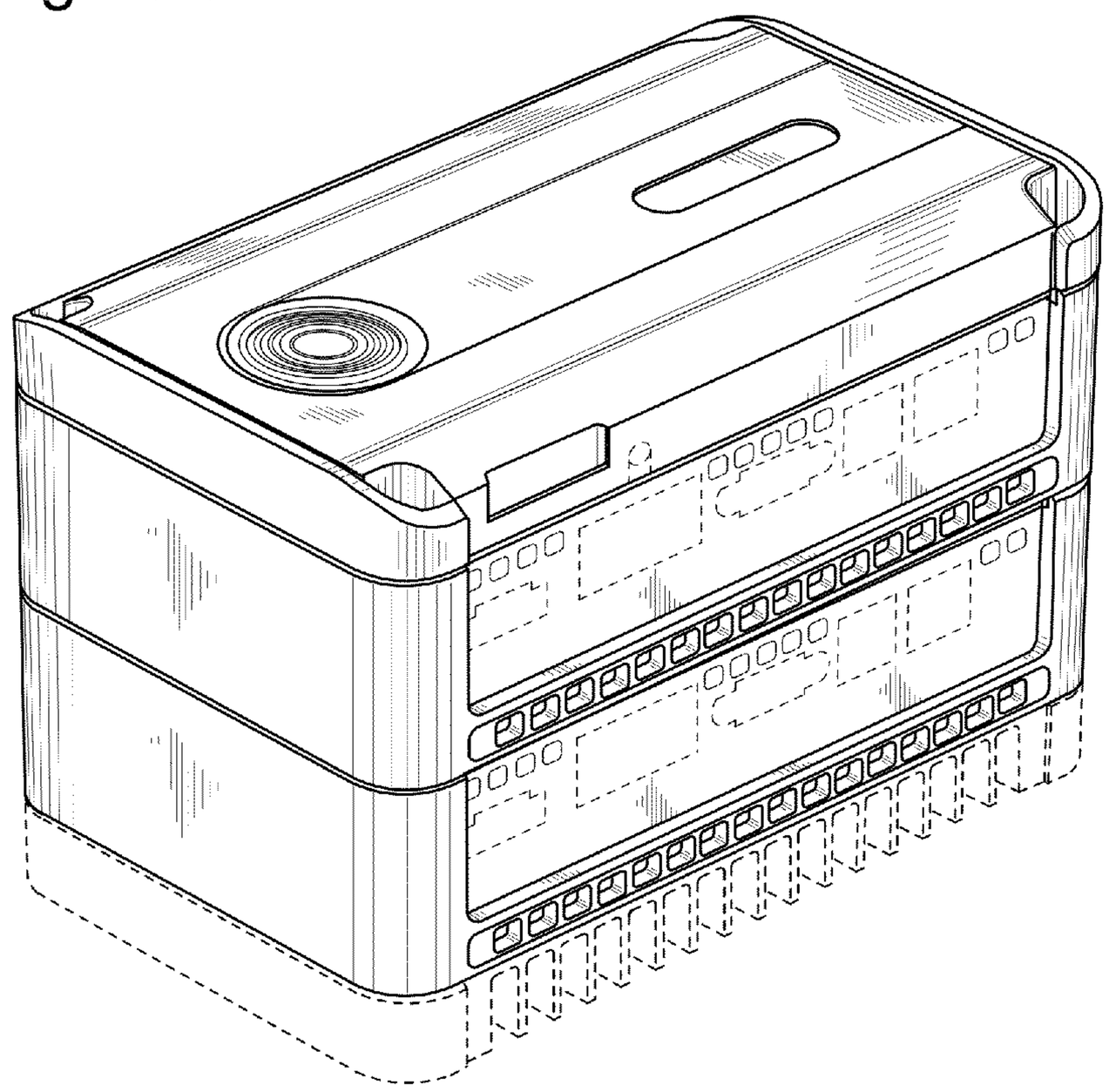
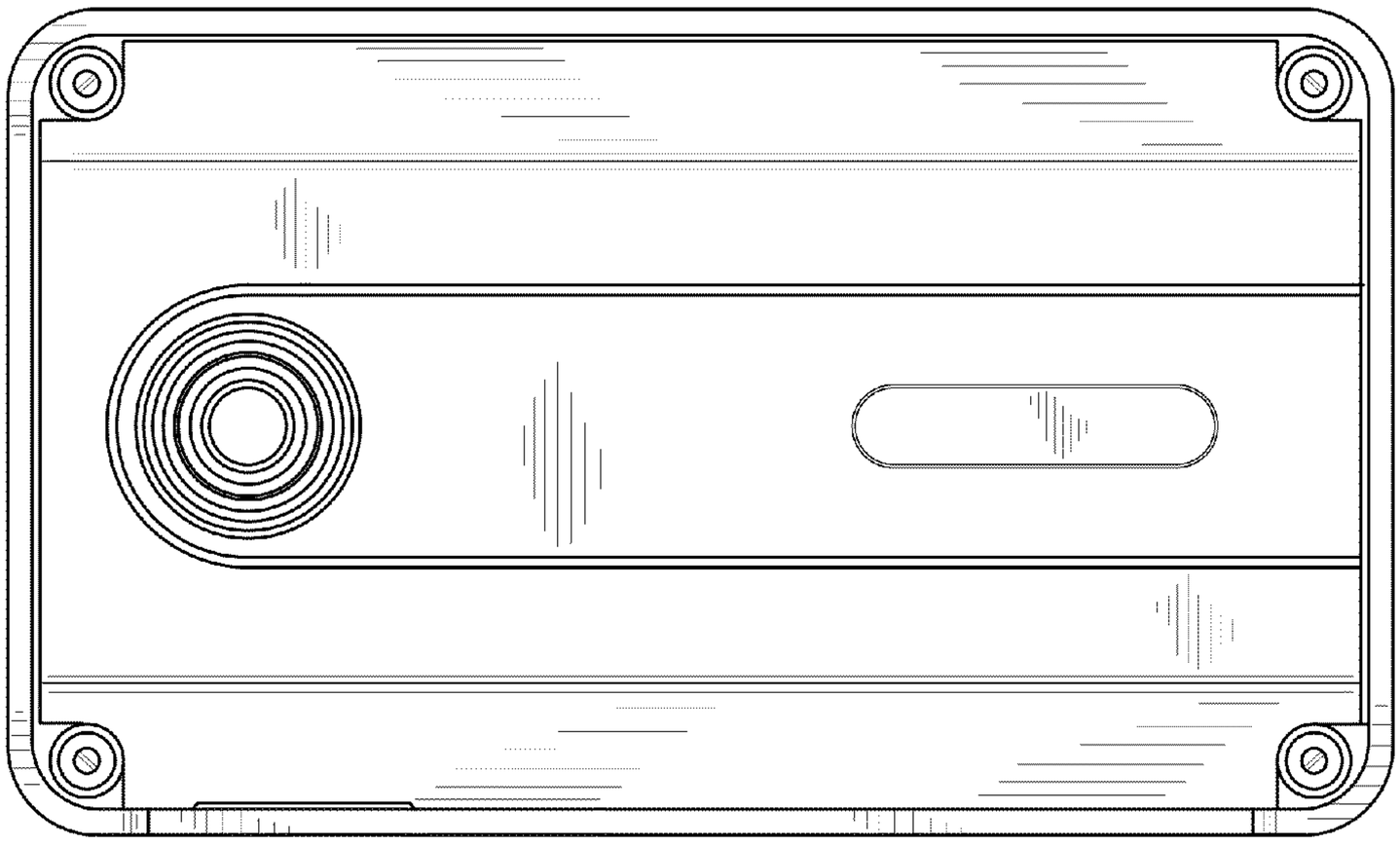


Figure 7



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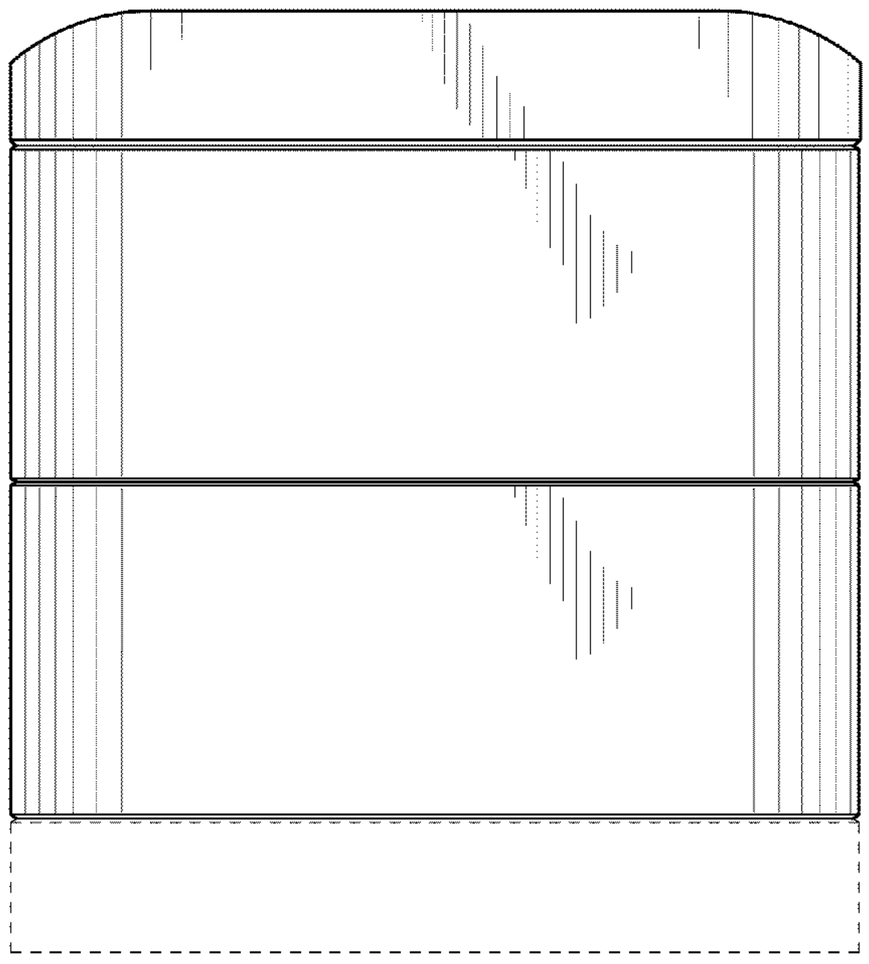

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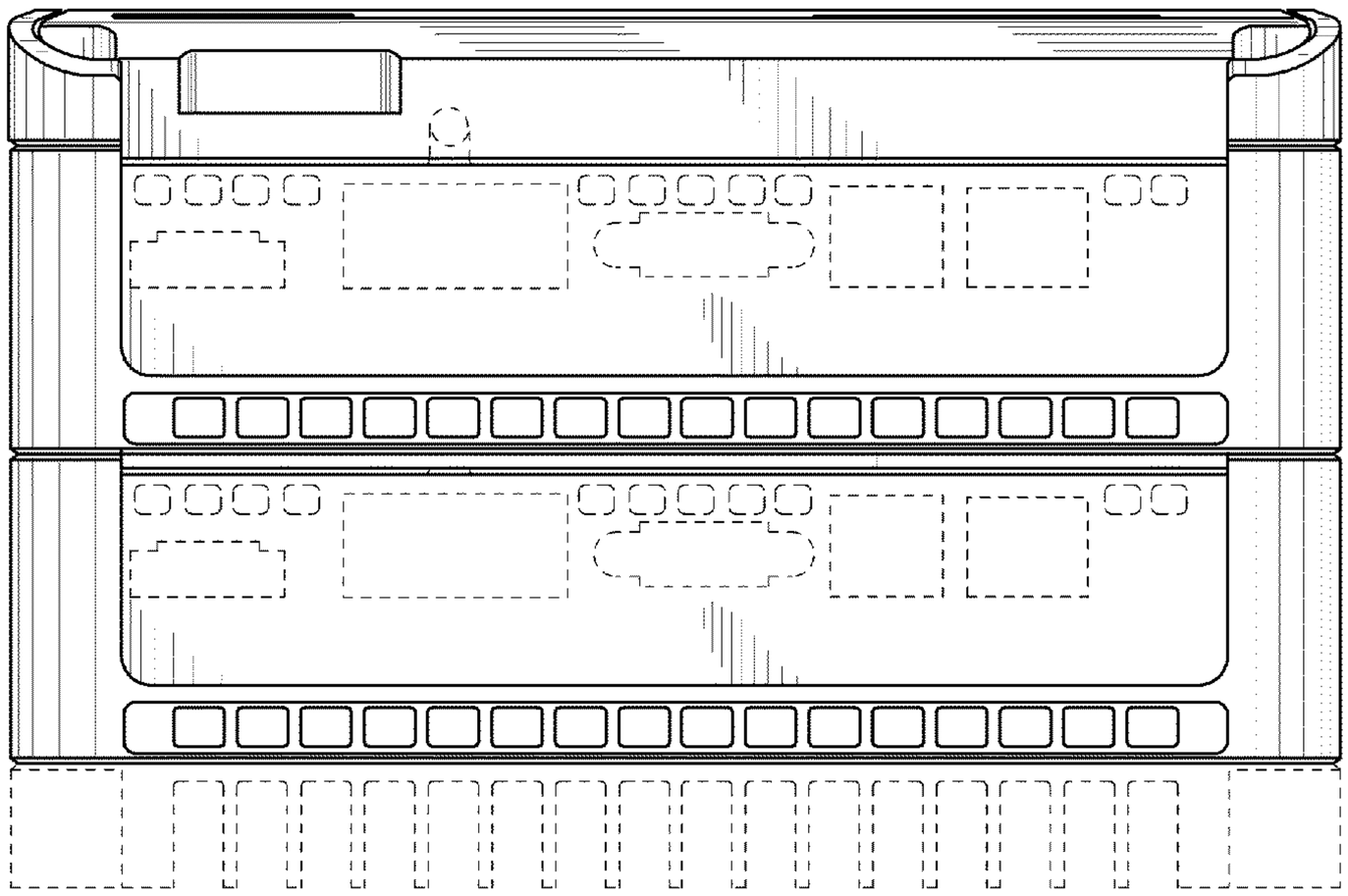

Figure 10

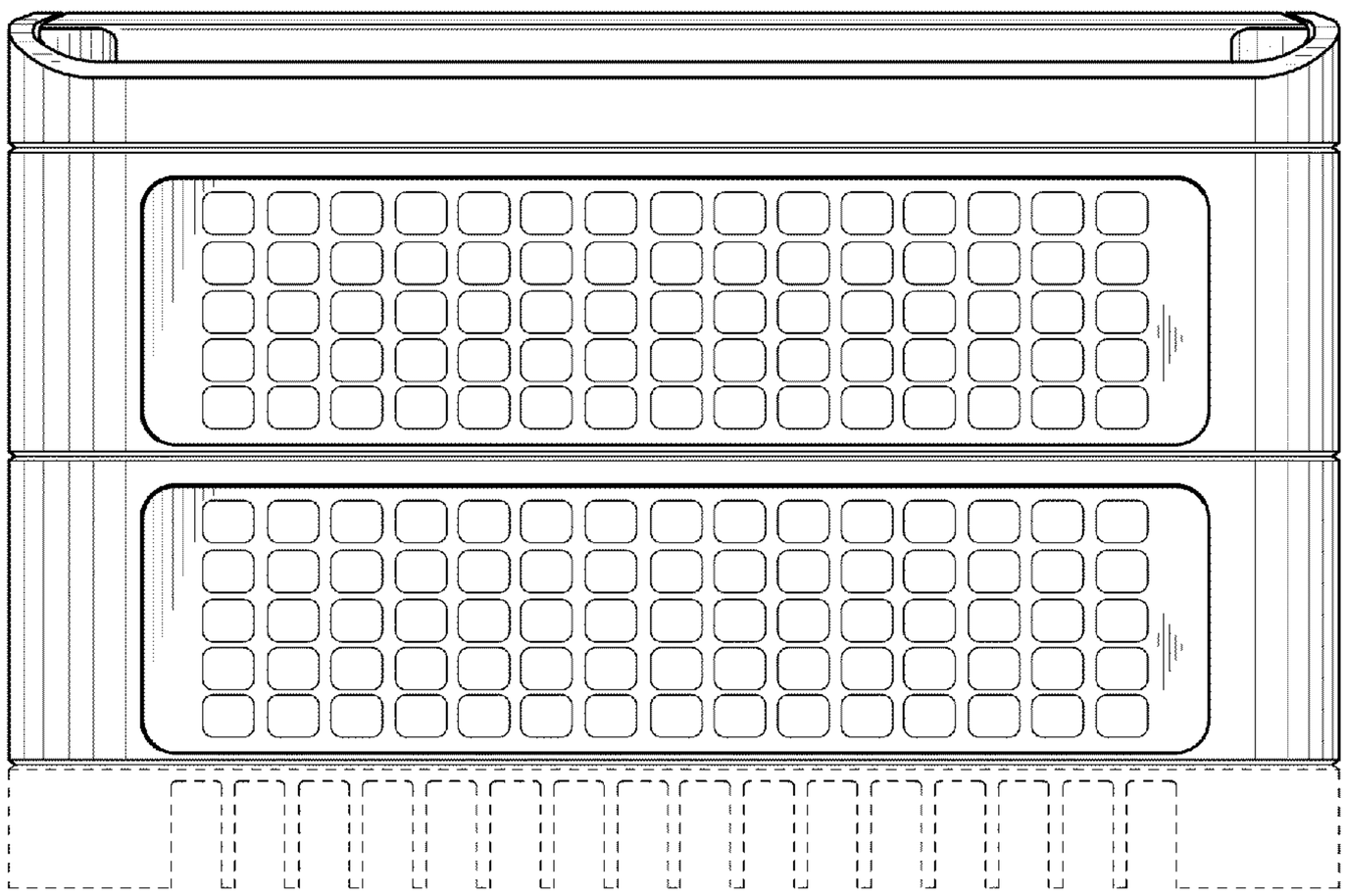

Figure 11

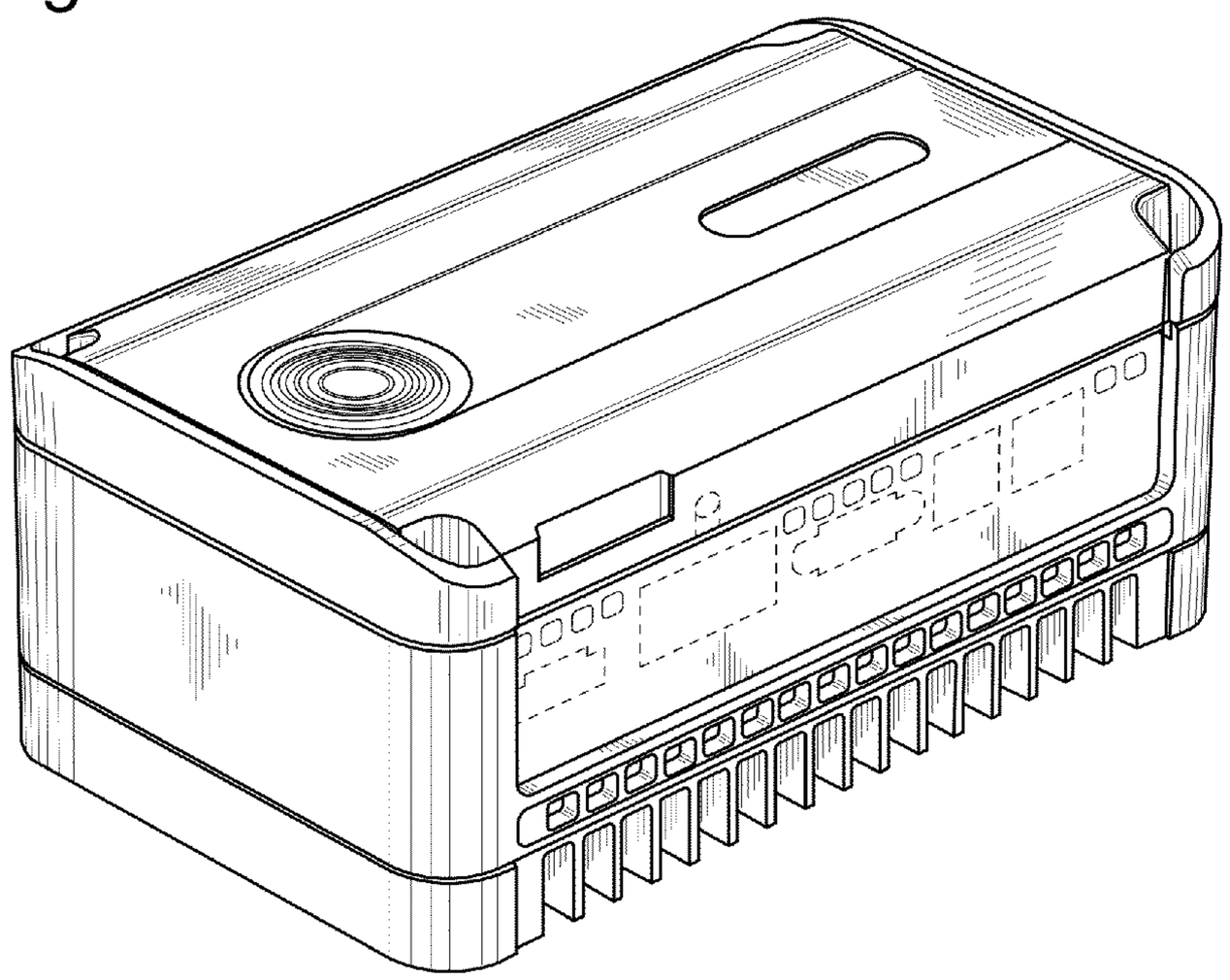

Figure 12

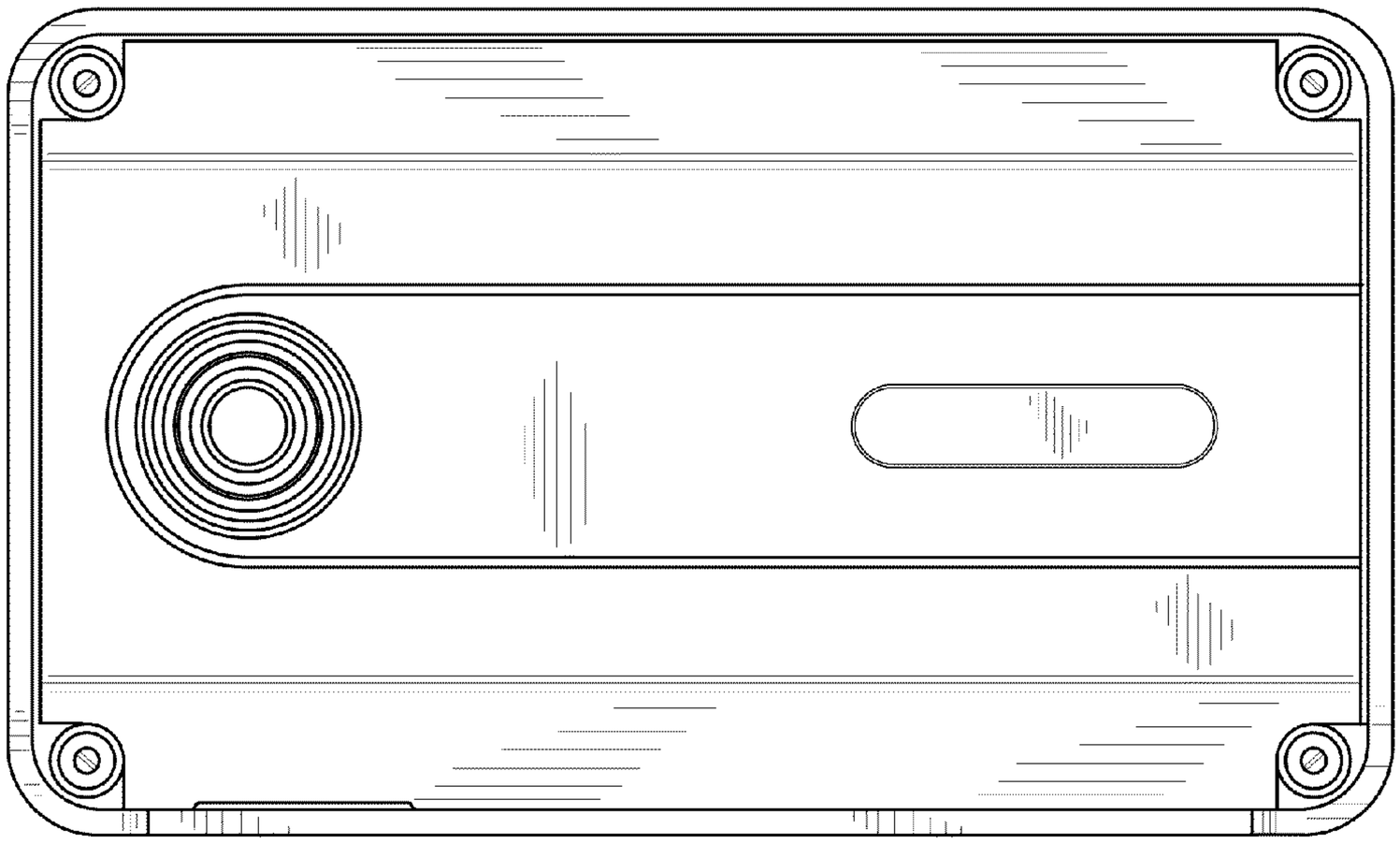

Figure 13

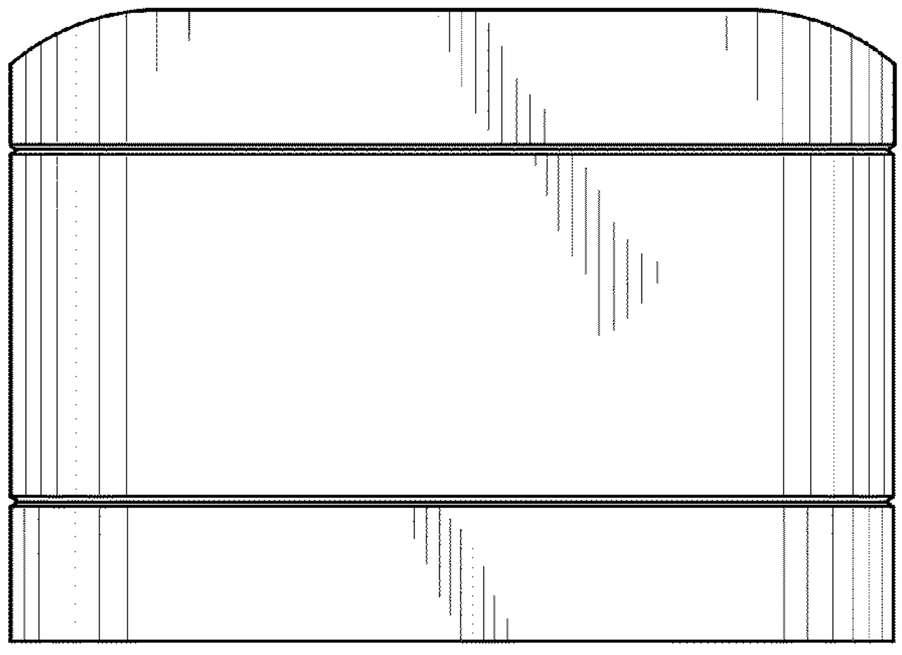

Figure 14

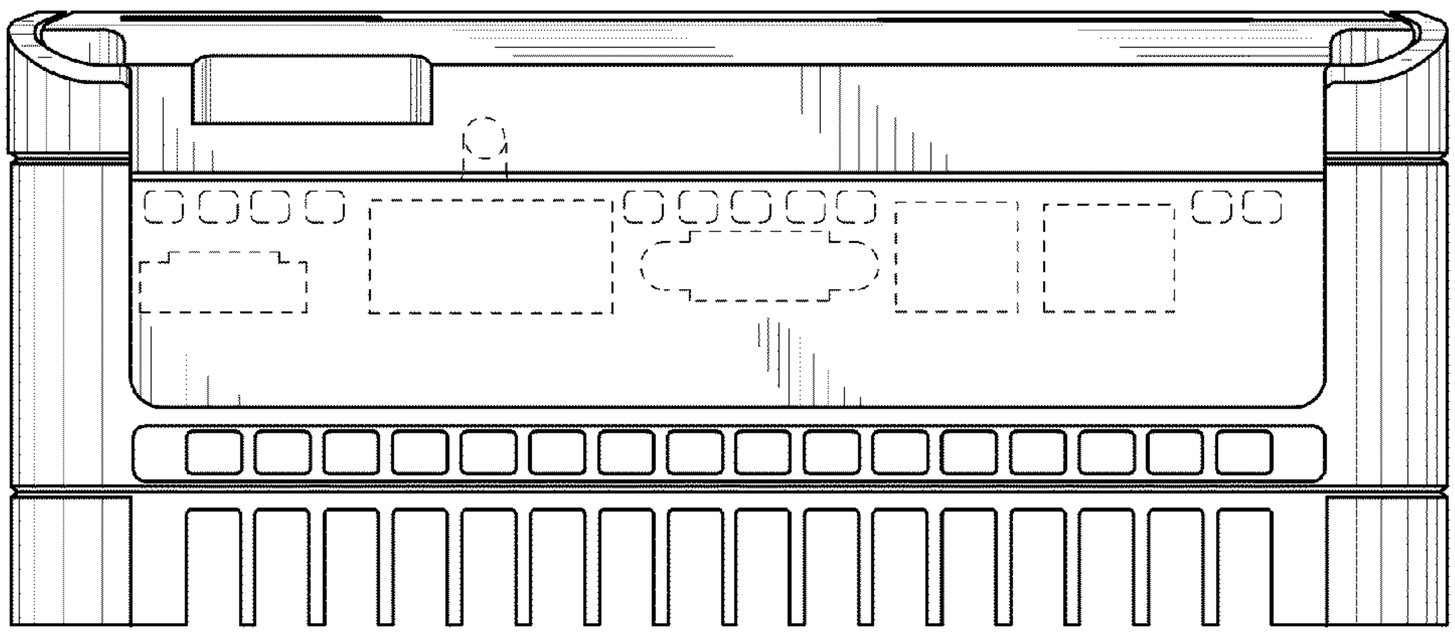

Figure 15