



US00D679272S

(12) **United States Design Patent**  
**Frost et al.**

(10) **Patent No.:** **US D679,272 S**

(45) **Date of Patent:** **\*\* \*Apr. 2, 2013**

(54) **SOLID-STATE MEMORY MODULE**

(75) Inventors: **Holloway H. Frost**, Houston, TX (US);  
**Daniel E. Scheel**, Houston, TX (US);  
**John R. Harris**, Houston, TX (US)

(73) Assignee: **Texas Memory Systems, Inc.**, Houston, TX (US)

(\*) Notice: This patent is subject to a terminal disclaimer.

(\*\*) Term: **14 Years**

(21) Appl. No.: **29/390,914**

(22) Filed: **Apr. 29, 2011**

(51) **LOC (9) Cl.** ..... **14-02**

(52) **U.S. Cl.** ..... **D14/313**

(58) **Field of Classification Search** ..... D14/300–313,  
D14/348–356; 312/223.2; 361/679.39, 690,  
361/695, 724–730, 796

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,744,005	A *	5/1988	Milani	.....	361/679.48
4,931,907	A *	6/1990	Robinson et al.	.....	361/727
D329,641	S *	9/1992	Goff	.....	D14/313
D330,198	S *	10/1992	Lajara et al.	.....	D14/435
D335,651	S *	5/1993	Jones et al.	.....	D14/313
D338,671	S *	8/1993	Ito et al.	.....	D14/160
5,460,571	A *	10/1995	Kato et al.	.....	454/184
5,751,549	A *	5/1998	Eberhardt et al.	.....	361/679.33
6,075,698	A *	6/2000	Hogan et al.	.....	361/695
D485,835	S *	1/2004	Ritson et al.	.....	D14/300
6,714,411	B2 *	3/2004	Thompson et al.	.....	361/695
D504,425	S *	4/2005	Ritson et al.	.....	D14/300
7,110,256	B2 *	9/2006	Hasegawa et al.	.....	361/697

7,290,842	B1 *	11/2007	Lai	.....	312/223.2
7,450,383	B1 *	11/2008	Li et al.	.....	361/695
7,583,507	B2 *	9/2009	Starr et al.	.....	361/727
2003/0030977	A1 *	2/2003	Garnett et al.	.....	361/687
2008/0124234	A1 *	5/2008	Echazarreta	.....	417/423.14
2008/0180920	A1 *	7/2008	Chang	.....	361/728
2010/0284149	A1 *	11/2010	Su	.....	361/695
2011/0090633	A1 *	4/2011	Rabinovitz	.....	361/679.31
2011/0219259	A1 *	9/2011	Frost et al.	.....	714/6.2

\* cited by examiner

*Primary Examiner* — Karen E Kearney

(74) *Attorney, Agent, or Firm* — Locke Lord LLP

(57) **CLAIM**

The ornamental design for a solid-state memory module, as shown and described.

**DESCRIPTION**

FIG. 1 is a perspective view of a solid-state memory module according to my new design;

FIG. 2 is a top view of the solid-state memory module according to my new design;

FIG. 3 is a bottom view of the solid-state memory module according to my new design;

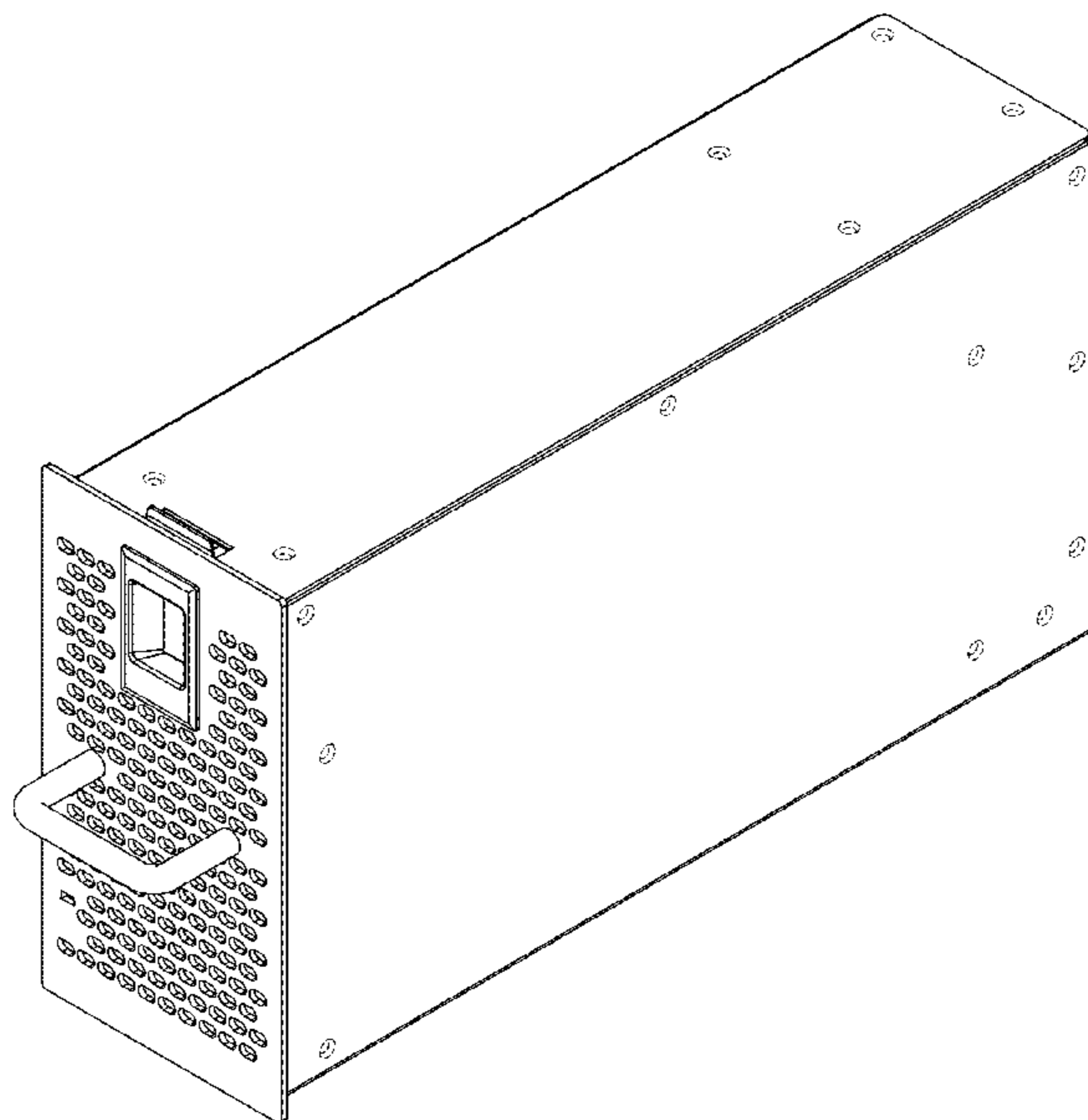
FIG. 4 is a front view of the solid-state memory module according to my new design;

FIG. 5 is a rear view of the solid-state memory module according to my new design; and,

FIG. 6 is a left side view of the solid-state memory module according to my new design, the right side being a mirror image thereof.

The broken line showings of the fastener holes and other portions are for the purpose of illustrating unclaimed portions of the solid-state memory module and form no part of the claimed design.

**1 Claim, 4 Drawing Sheets**



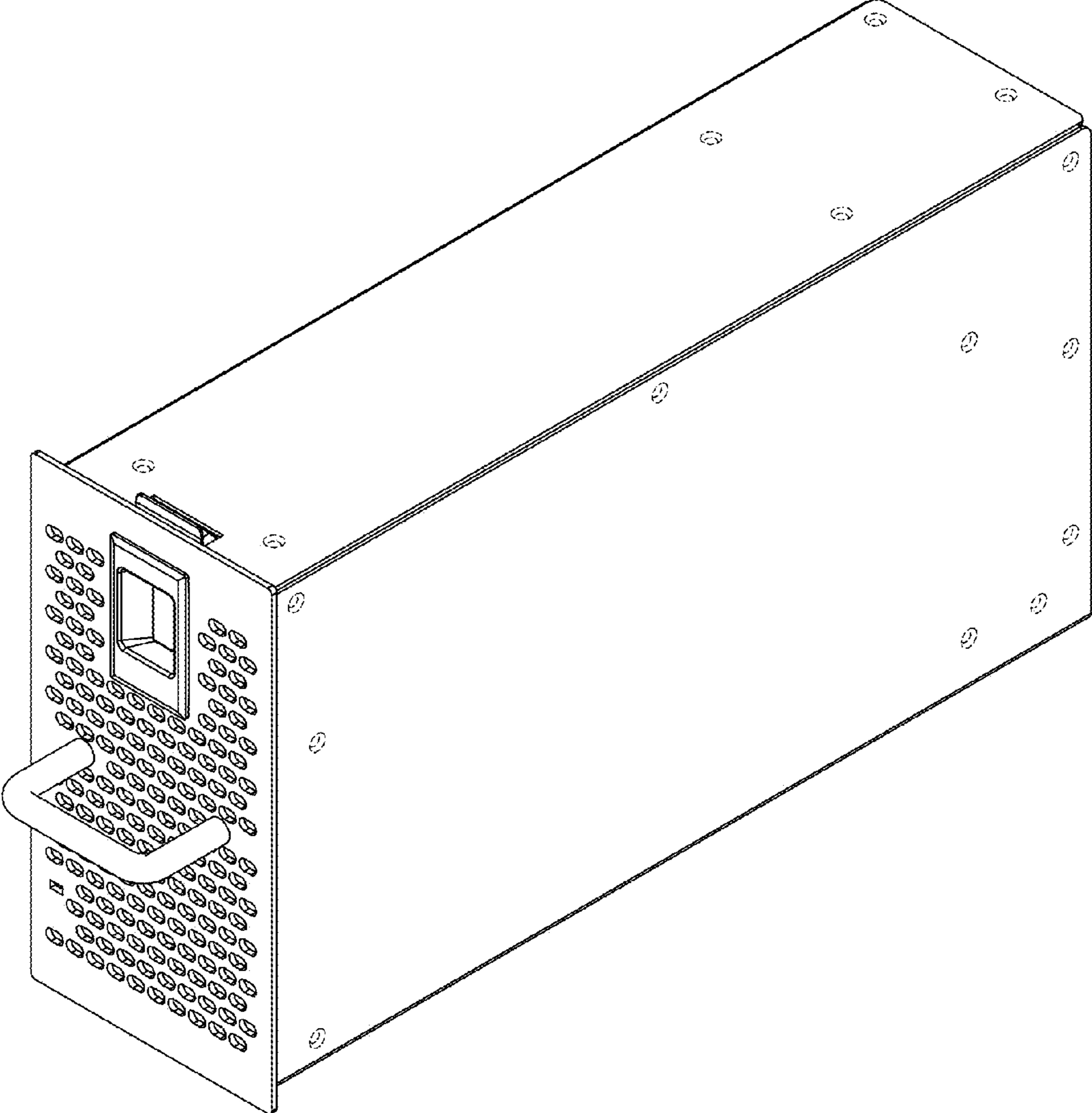
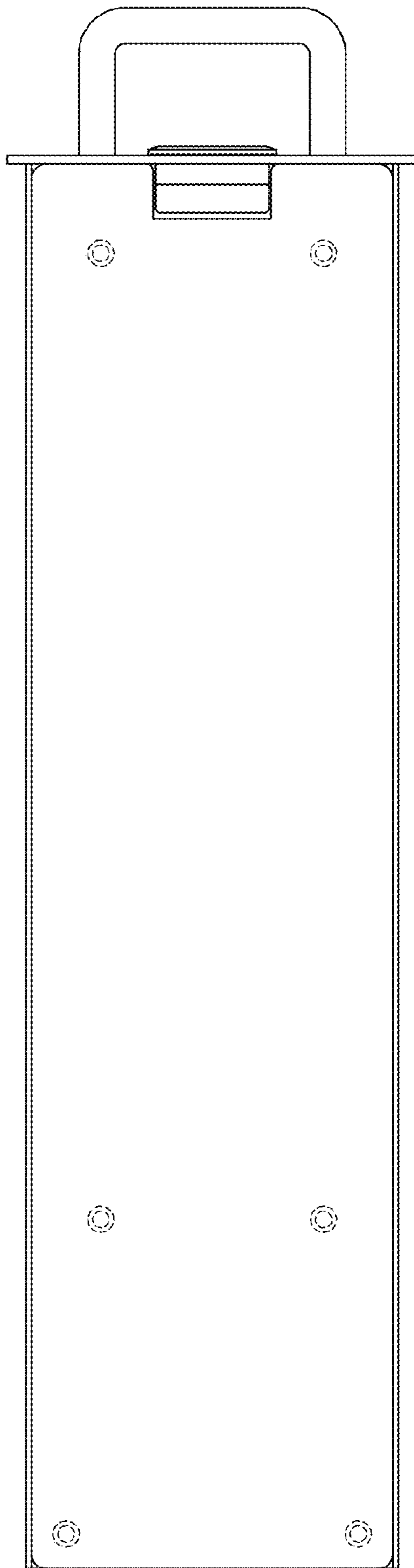
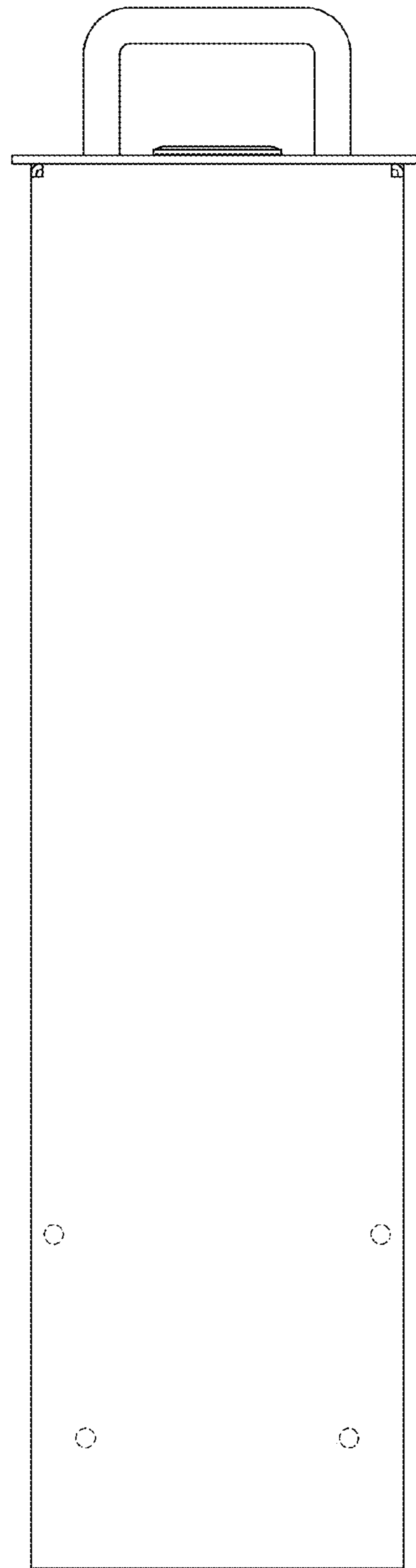


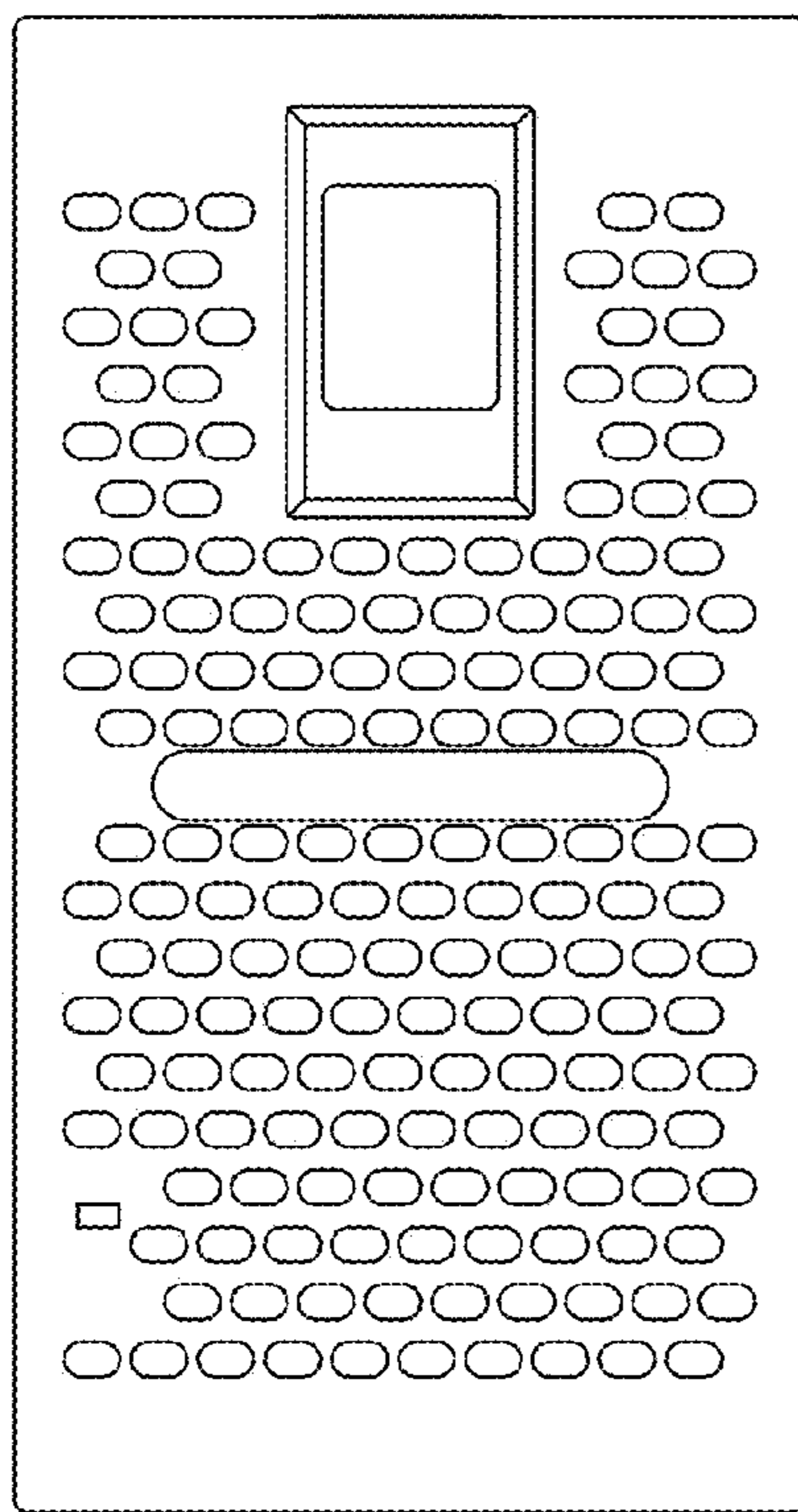
FIG. 1



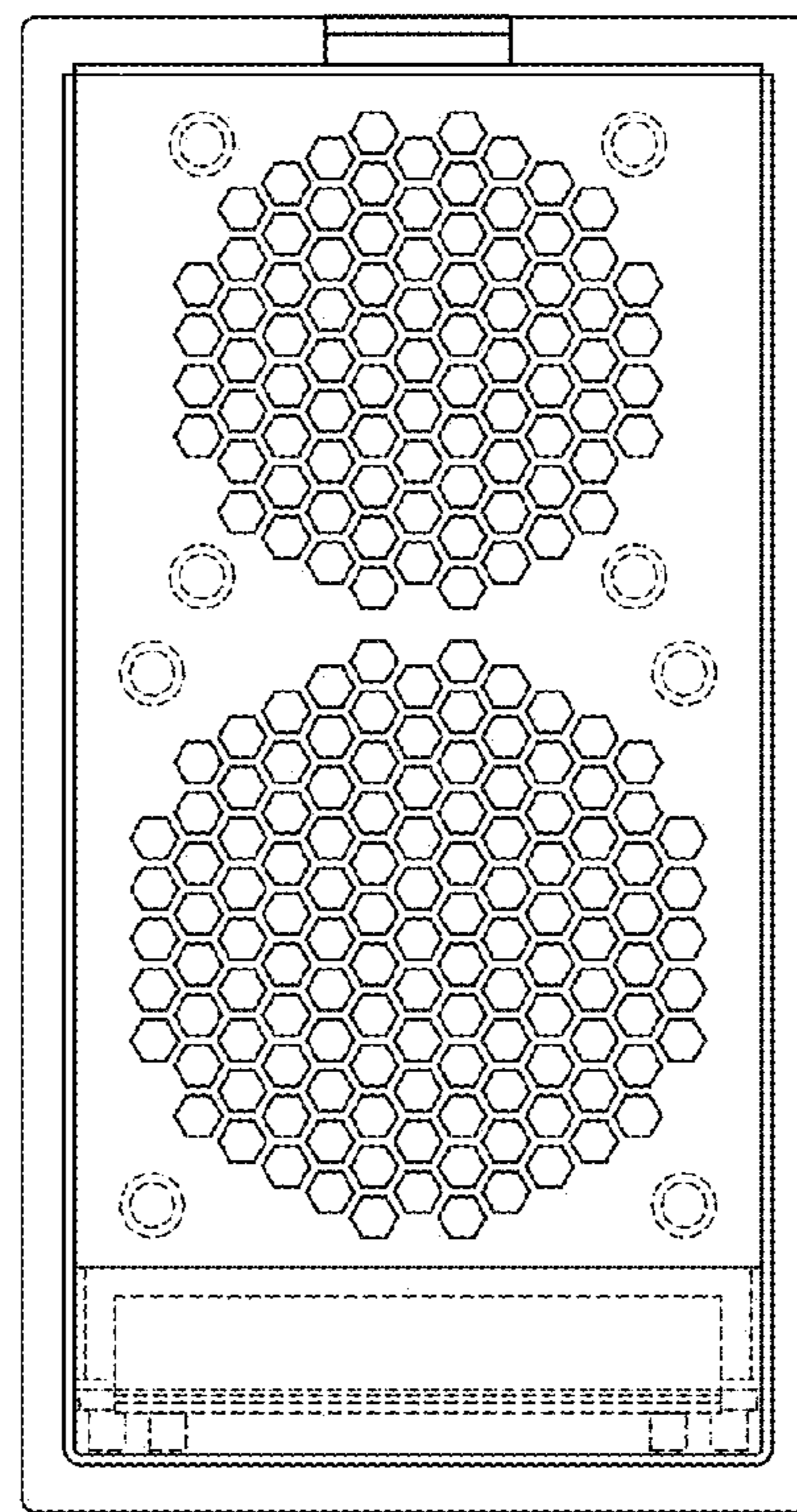
**FIG. 2**



**FIG. 3**

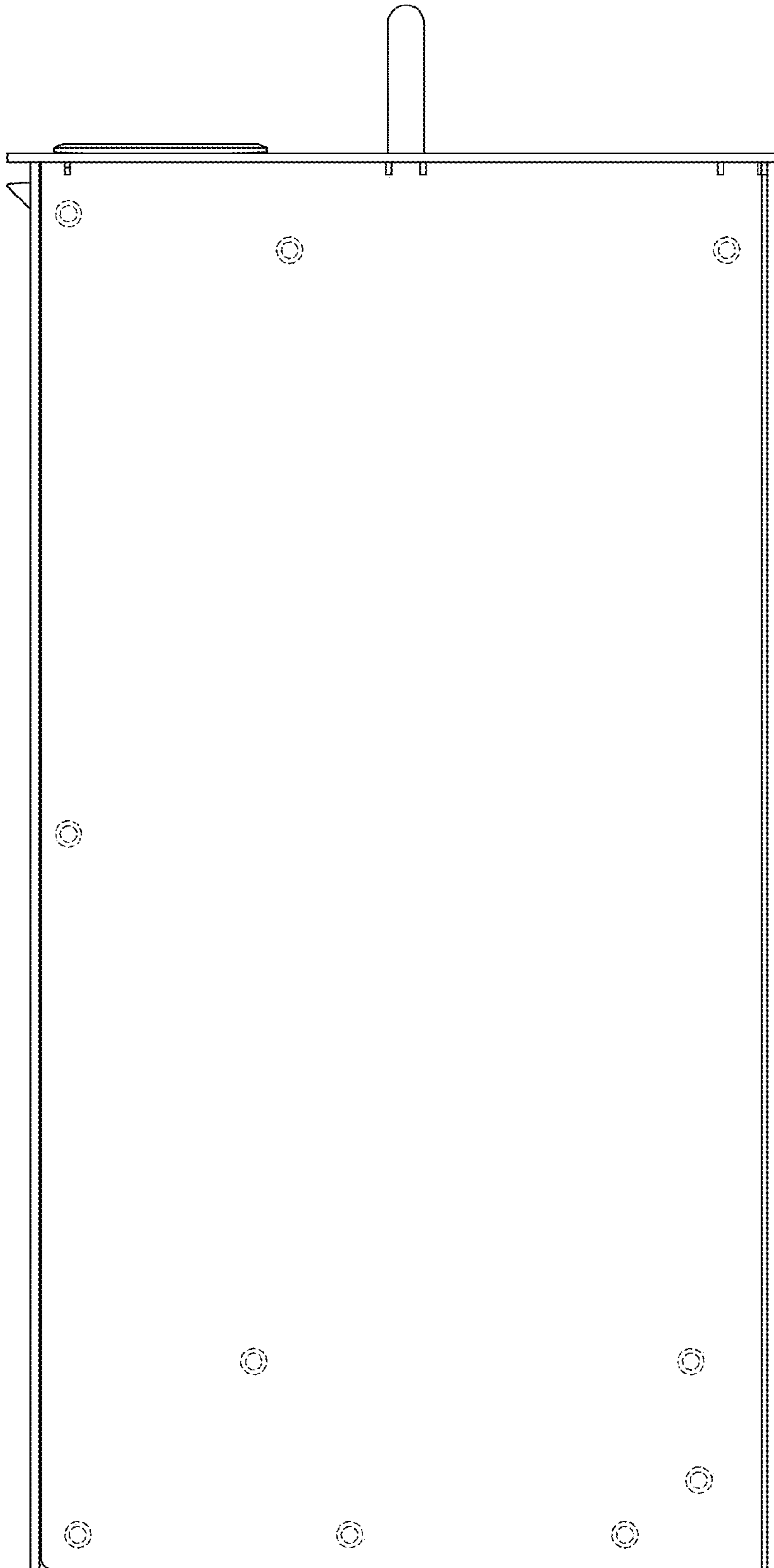


**FIG. 4**



**FIG. 5**





**FIG. 6**