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Moriai et al.

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(54) **PORTION OF A SUBSTRATE FOR AN ELECTRONIC CIRCUIT**

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(30) **Foreign Application Priority Data**

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(58) **Field of Classification Search** D13/182; 257/678, 690; 361/679.31, 719, 720, 752, 361/777, 820
See application file for complete search history.

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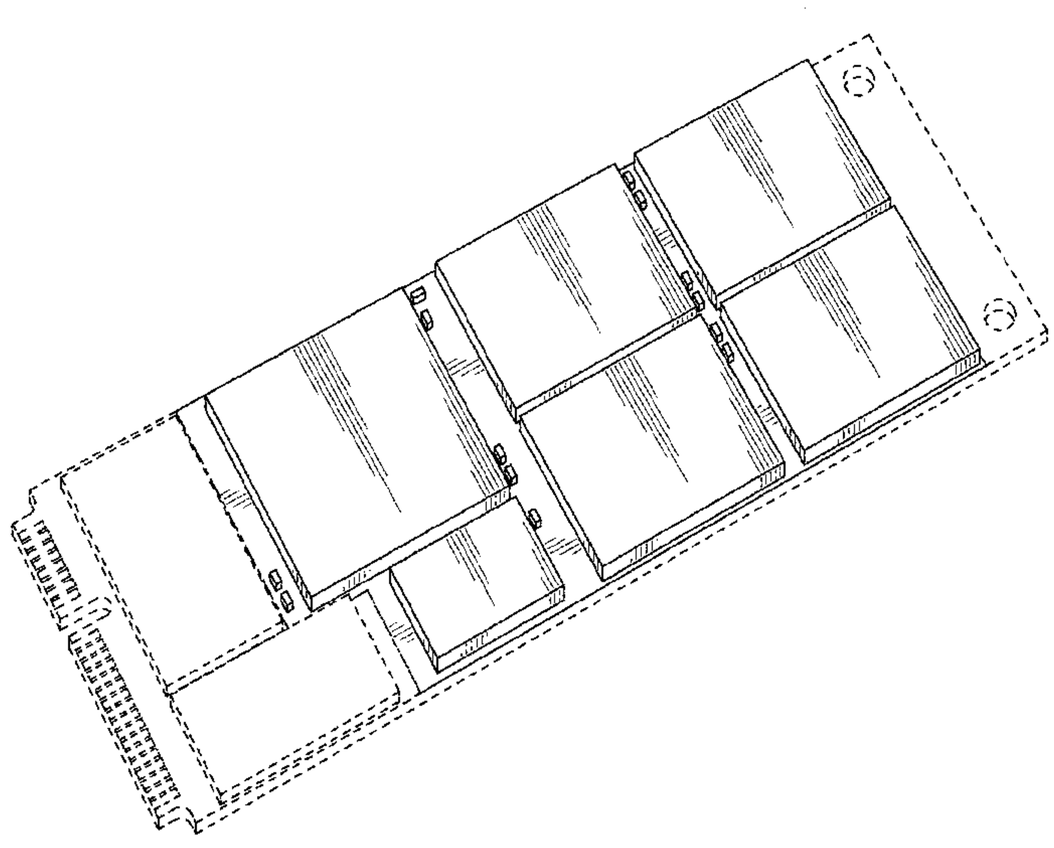
(57) **CLAIM**

The ornamental design for a portion of a substrate for an electronic circuit, as shown and described.

DESCRIPTION

FIG. **1** is a front, bottom and left side perspective view of a portion of a substrate for an electronic circuit, showing our new design;
FIG. **2** is a top plan view thereof;
FIG. **3** is a left side elevational view thereof;
FIG. **4** is a front elevational view thereof;
FIG. **5** is a right side elevational view thereof;
FIG. **6** is a bottom plan view thereof; and,
FIG. **7** is a rear elevational view thereof.
The uneven spaced broken lines define the bounds of the claimed design and form no part thereof. The even spaced broken line showing of the substrate for an electronic circuit is for illustrative purpose only and forms no part of the claimed design.

1 Claim, 3 Drawing Sheets



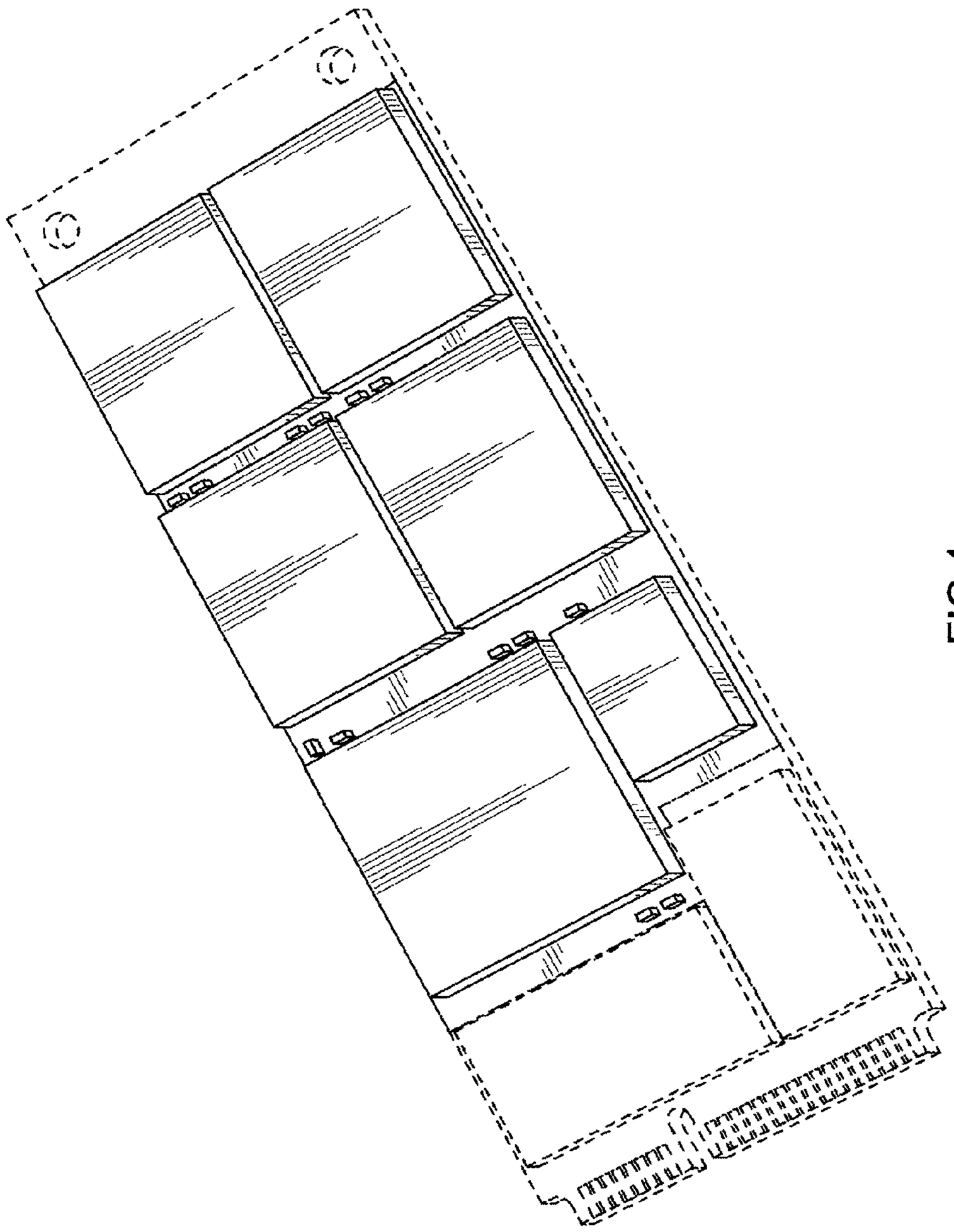


FIG.1

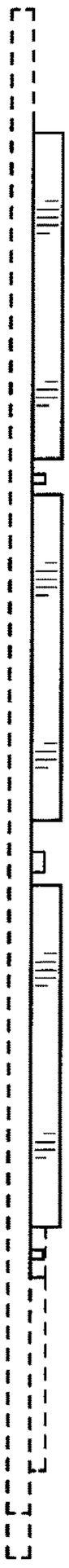


FIG.2

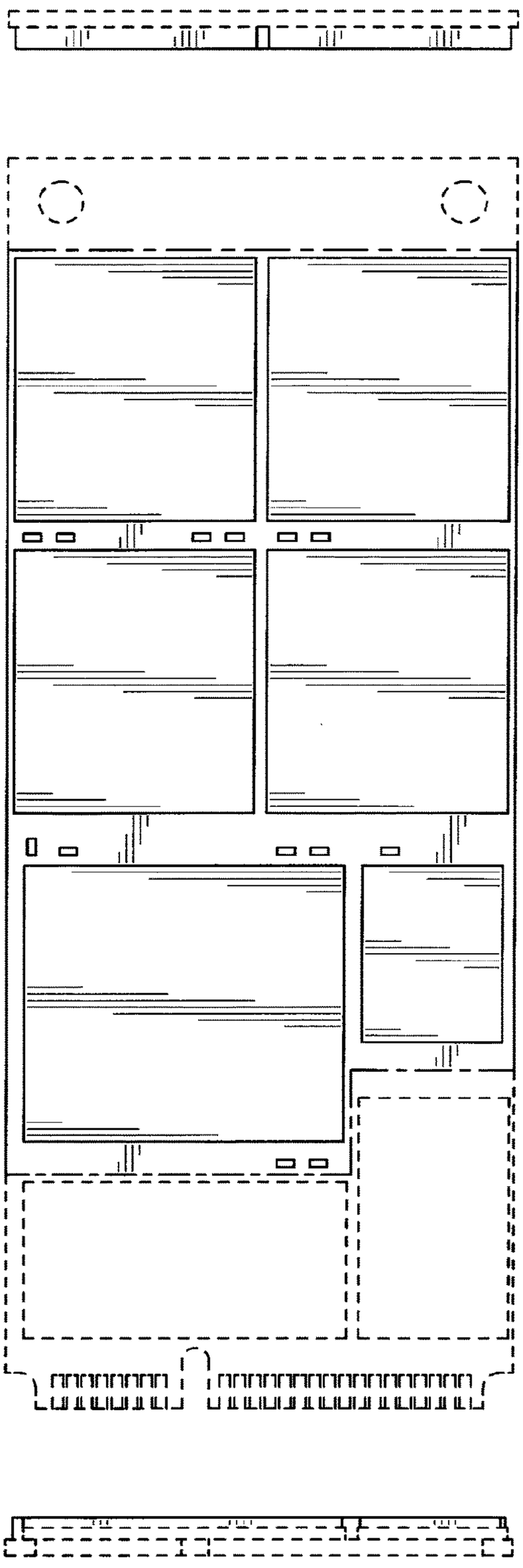


FIG.4

FIG.6

FIG.3

FIG.5

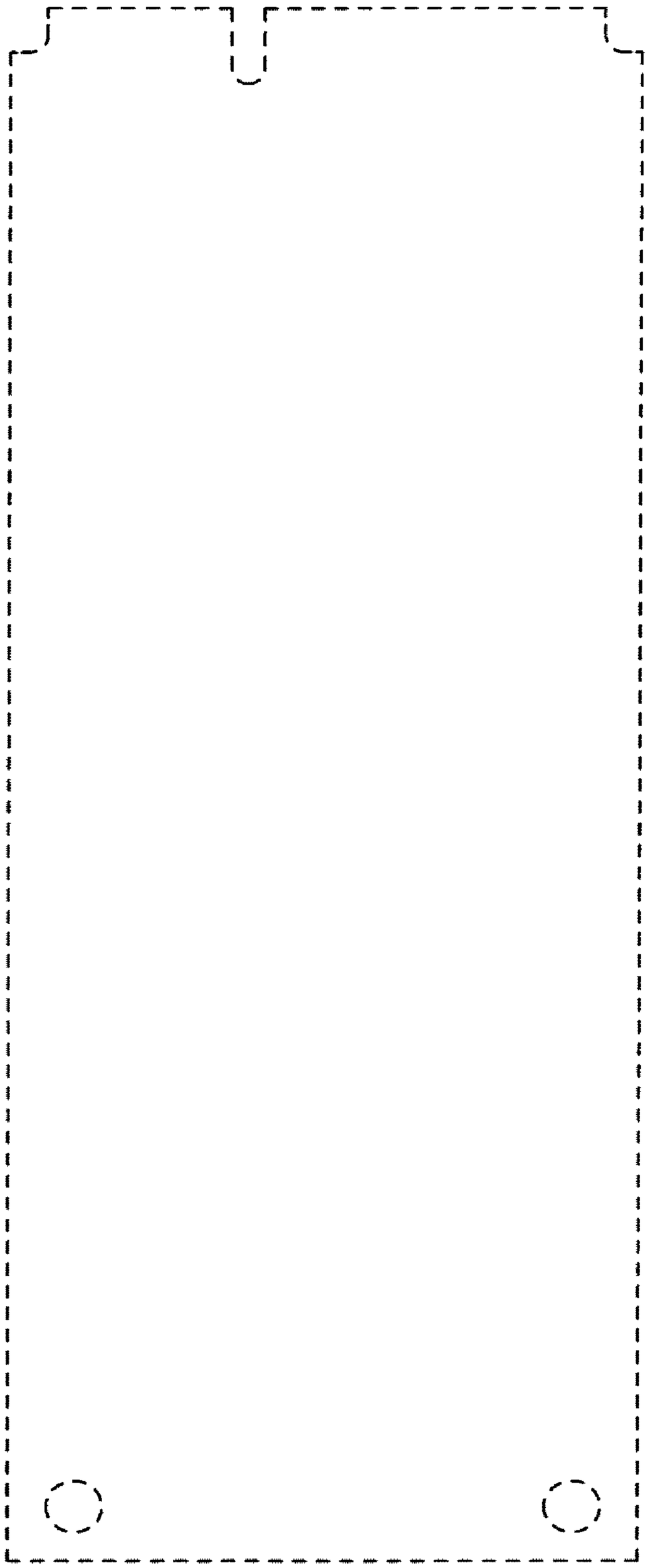


FIG.7