US00D673287S

(12) United States Design Patent

Akiyama et al.

(10) Patent No.: US D673,287 S
(45) Date of Patent: ** Dec. 25, 2012

(54) **MICRO FLOW CHANNEL CHIP**

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(**) Term: **14 Years**

(21) Appl. No.: **29/371,203**

(22) Filed: **Nov. 24, 2010**

(51) **LOC (9) Cl.** **24-01**
(52) **U.S. Cl.** **D24/216**
(58) **Field of Classification Search** D24/216–217, D24/219, 222–226, 227, 231, 232, 107, 169, D24/186; D10/81; 422/400–404, 408, 430, 422/68.1, 69, 500, 502, 503; 435/287.1, 435/287.3, 287.4, 288.1, 288.3, 288.7
See application file for complete search history.

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(74) *Attorney, Agent, or Firm* — Rader, Fishman & Grauer PLLC

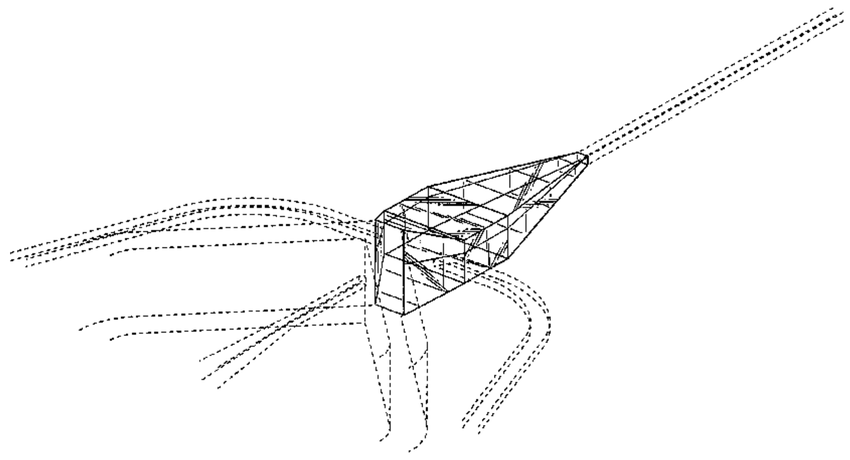
(57) **CLAIM**

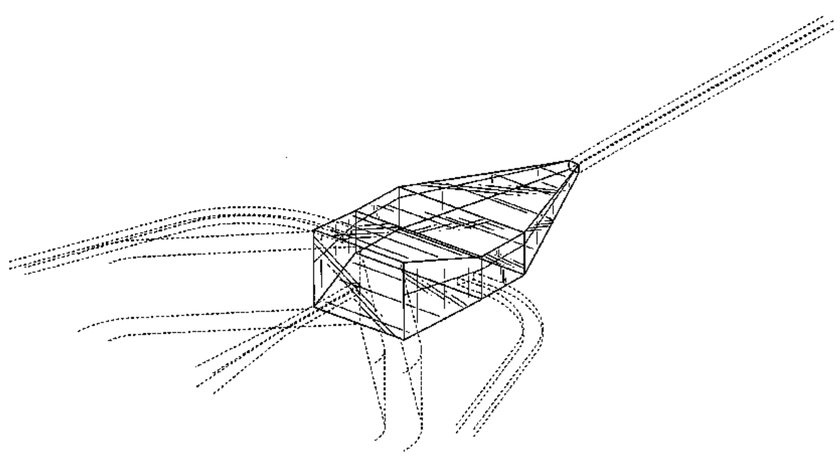
The ornamental design for a micro flow channel chip, as shown and described.

DESCRIPTION

FIG. **1** is a top plan view of a first embodiment of a micro flow channel chip showing our new design, a bottom plan view thereof being a mirror image;
FIG. **2** is a front elevational view thereof, a rear elevational view being a mirror image;
FIG. **3** is a right side elevational view thereof;
FIG. **4** is an enlarged partial front, top, left perspective view thereof;
FIG. **5** is an enlarged partial top plan view thereof;
FIG. **6** is an enlarged partial front elevational view thereof;
FIG. **7** is a top plan view of a second embodiment of a micro flow channel chip showing our new design, a bottom plan view thereof being a mirror image;
FIG. **8** is a front elevational view thereof, a rear elevational view being a mirror image;
FIG. **9** is a right side elevational view thereof;
FIG. **10** is an enlarged partial front, top, left perspective view thereof;
FIG. **11** is an enlarged partial top plan view thereof; and,
FIG. **12** is an enlarged partial front elevational view thereof.
In the drawing views, the broken lines are included for the purpose of illustrating portions of the micro flow channel chip that form no part of the claimed design.

1 Claim, 10 Drawing Sheets





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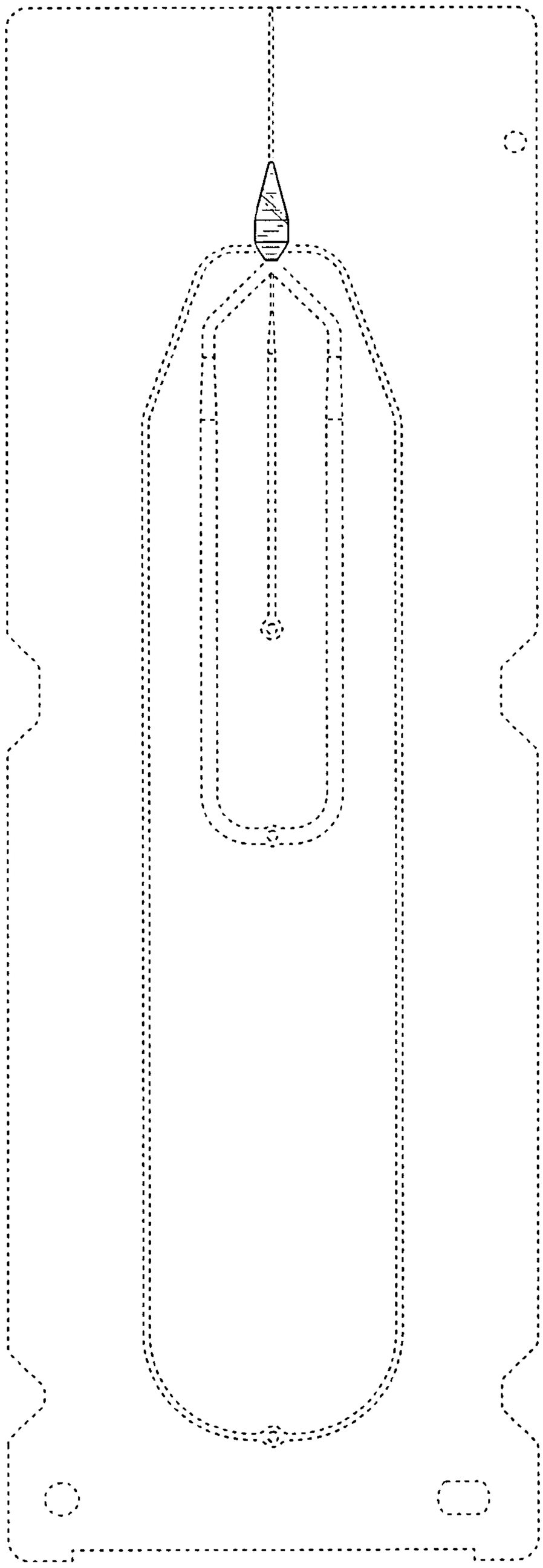


FIG.1

FIG.2

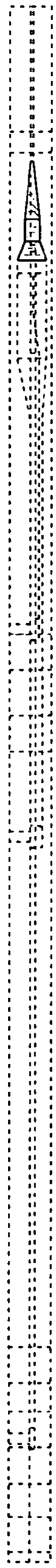


FIG.3

FIG.4

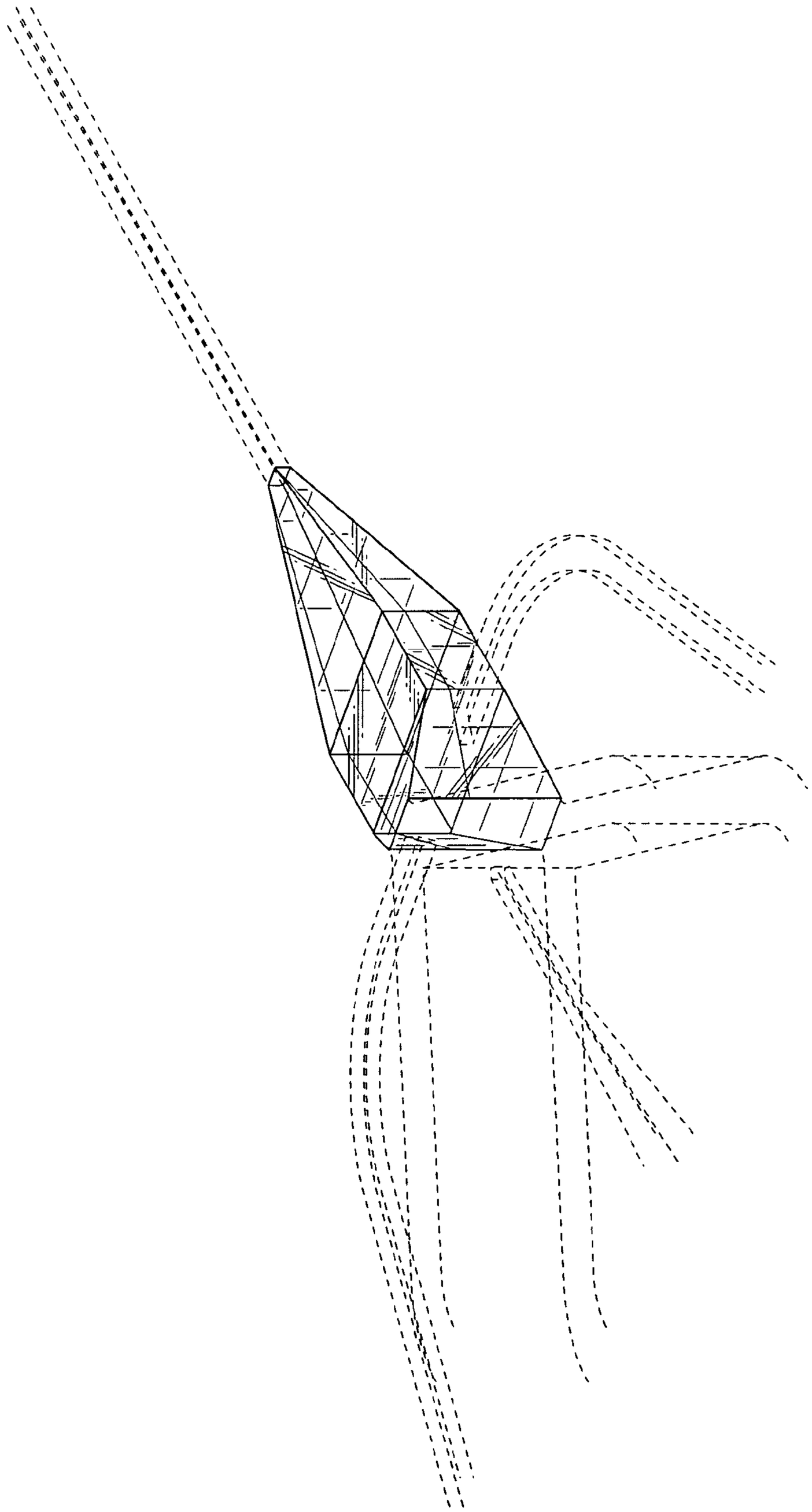


FIG.5

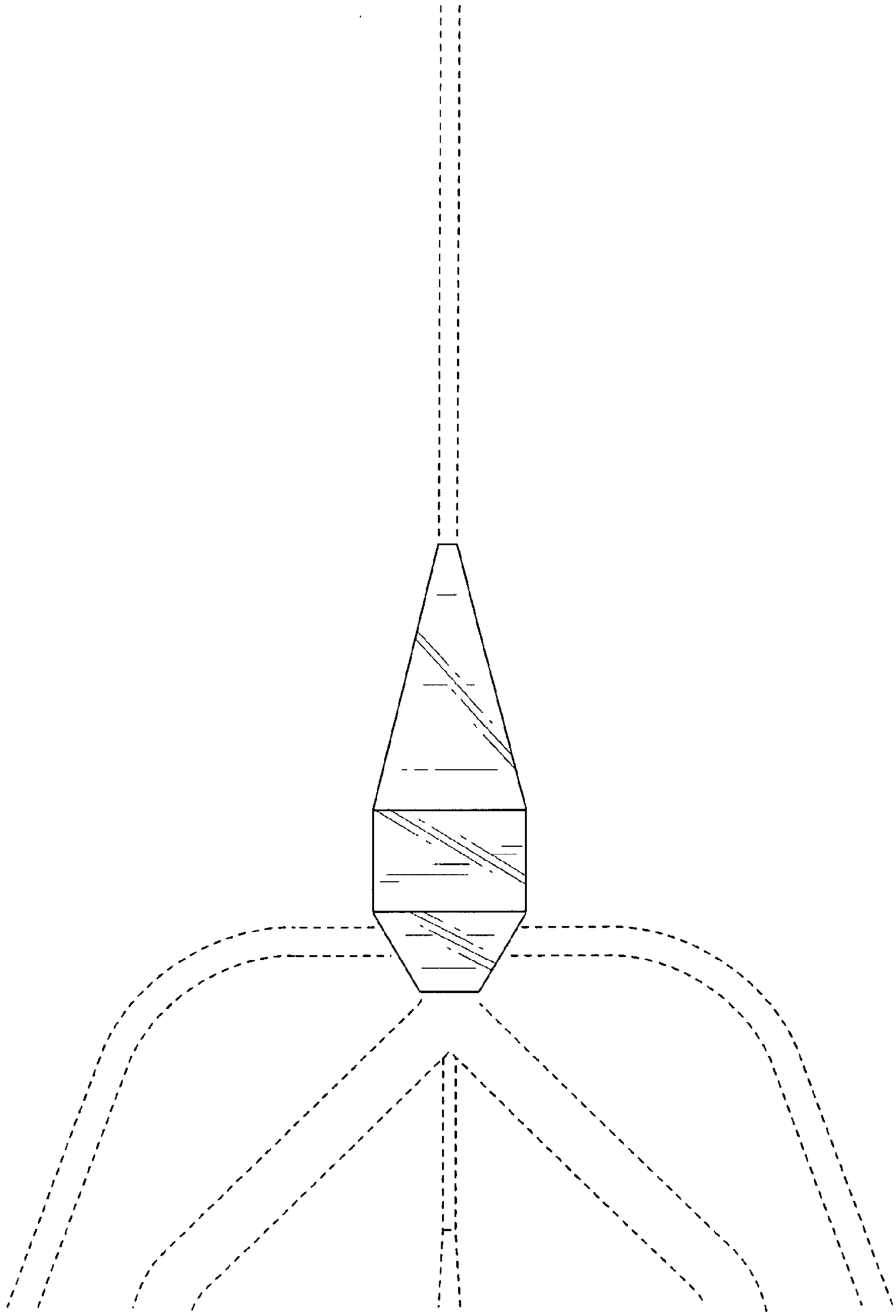
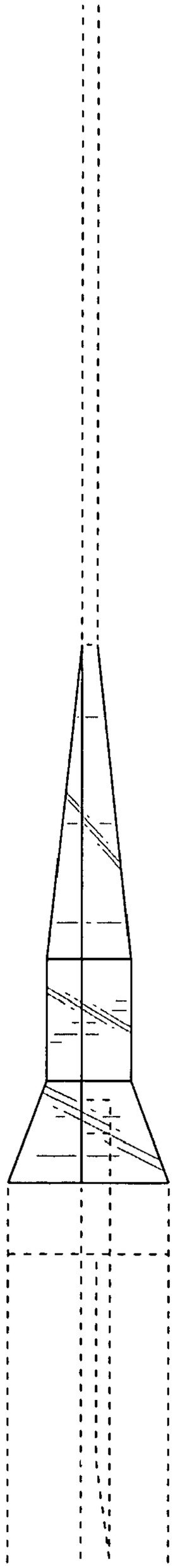


FIG.6



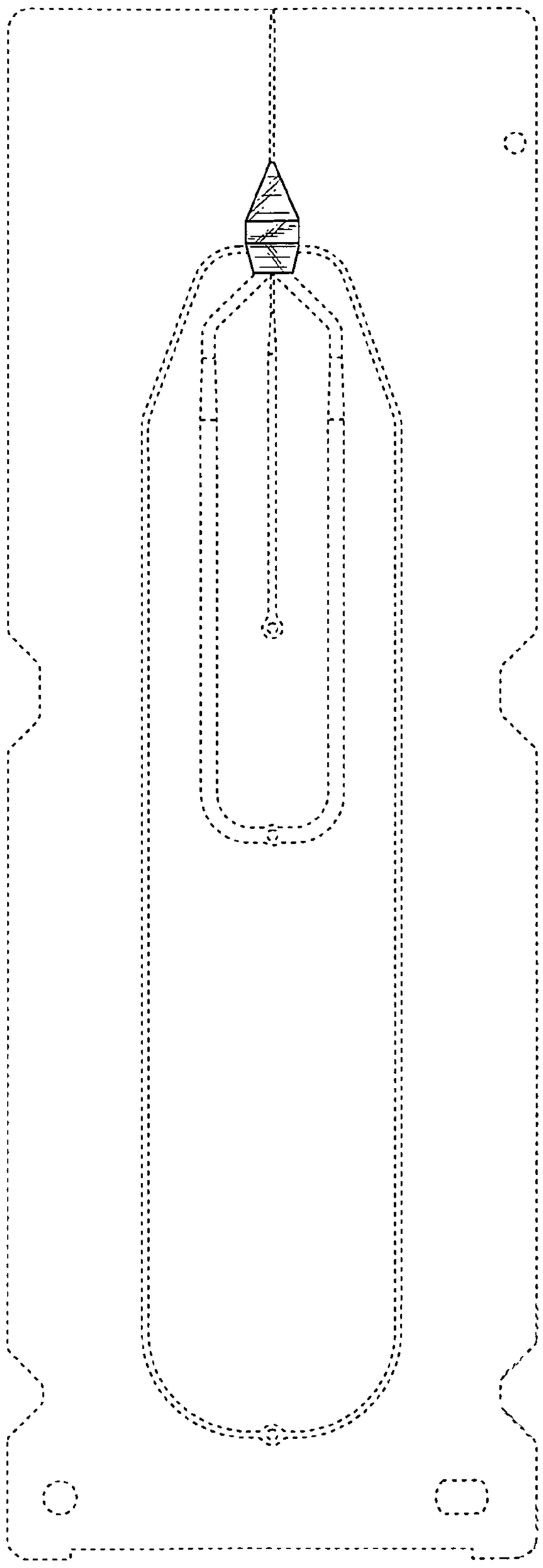


FIG.7

FIG.8

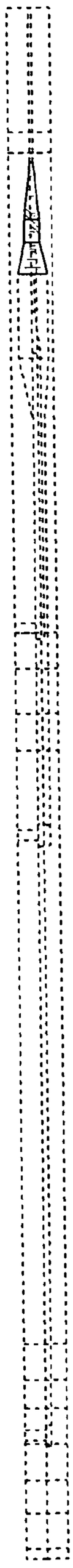


FIG.9

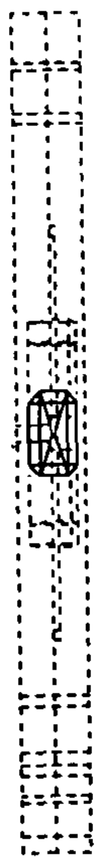


FIG.10

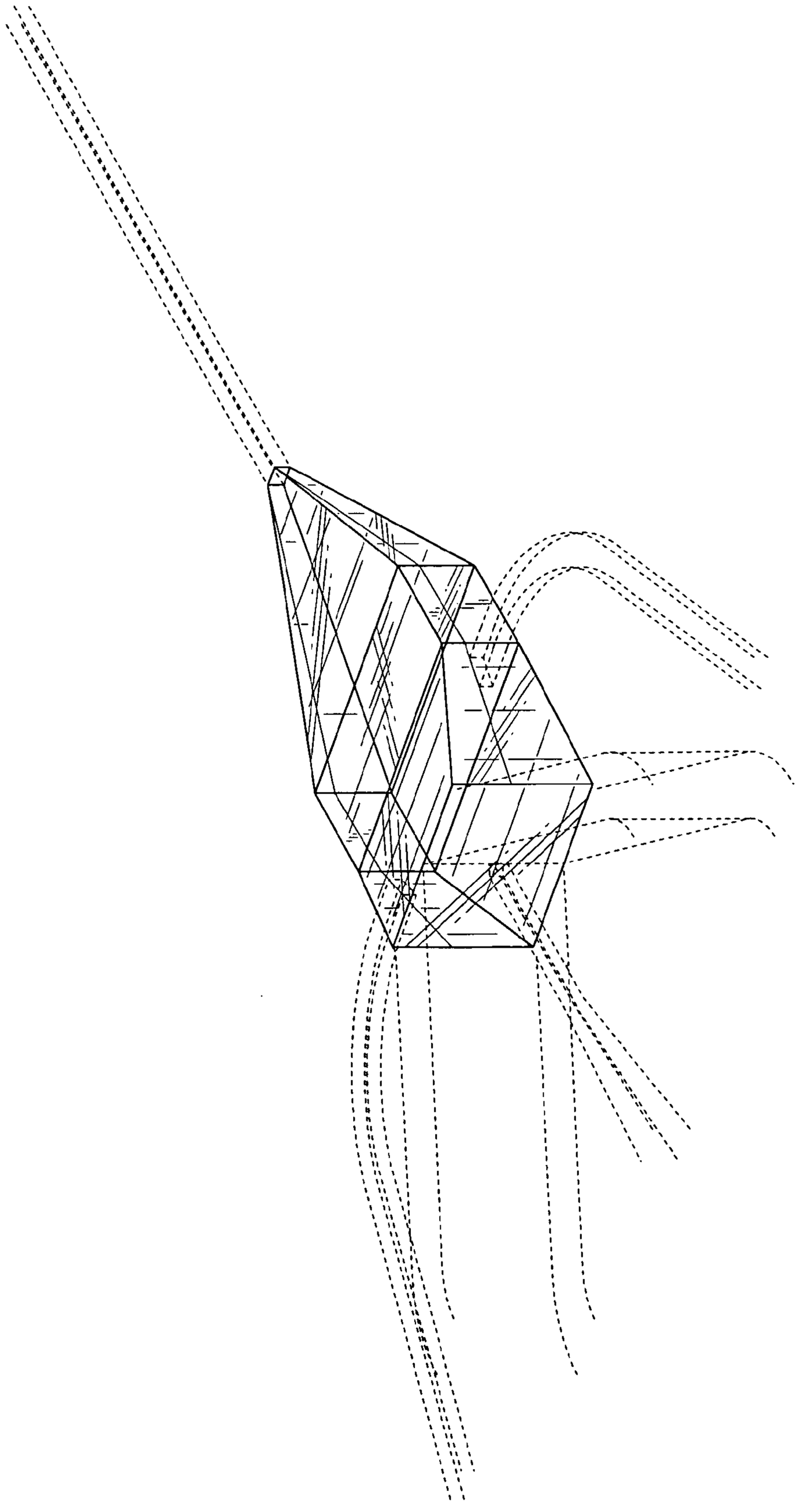


FIG.11

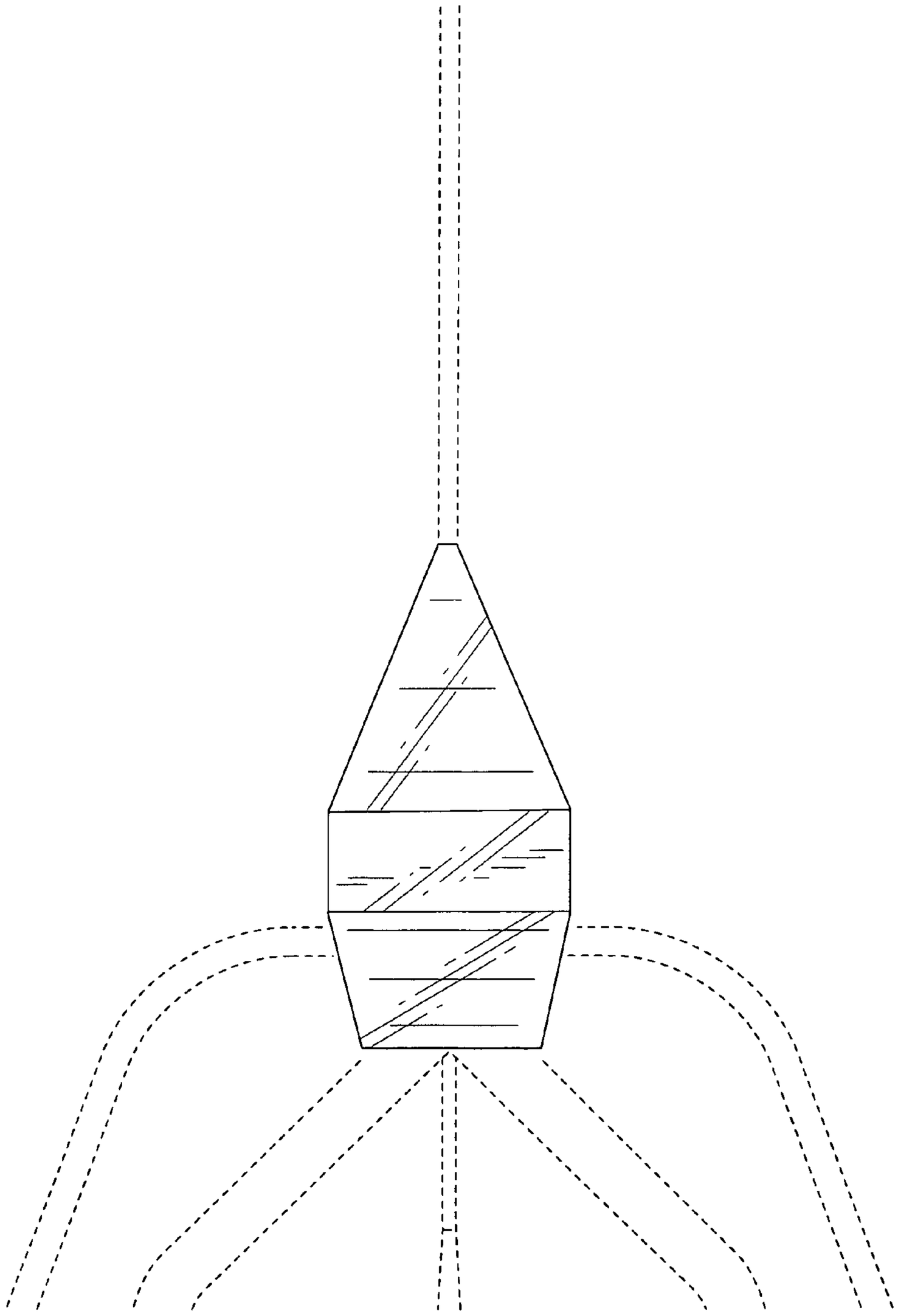


FIG.12