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(12) **United States Design Patent**  
**Shinoda**

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(54) **MICRO FLOW CHANNEL CHIP**  
(75) Inventor: **Masataka Shinoda**, Tokyo (JP)  
(73) Assignee: **Sony Corporation**, Tokyo (JP)  
(\*\*) Term: **14 Years**

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(51) **LOC (9) Cl.** ..... **24-01**  
(52) **U.S. Cl.** ..... **D24/216**  
(58) **Field of Classification Search** ..... D24/216–217,  
D24/219, 222–226, 227, 231, 232, 107, 169,  
D24/186; D10/81; 422/400–404, 408, 430,  
422/68.1, 69, 500, 502, 503; 435/287.1,  
435/287.3, 287.4, 288.1, 288.3, 288.7  
See application file for complete search history.

(57) **CLAIM**

The ornamental design for a micro flow channel chip, as shown and described.

**DESCRIPTION**

FIG. 1 is a top plan view of a micro flow channel chip showing my new design, a bottom plan view thereof being a mirror image;

FIG. 2 is a front elevational view thereof, a rear elevational view being a mirror image;

FIG. 3 is a right side elevational view thereof;

FIG. 4 is an enlarged partial front, top, left perspective view thereof;

FIG. 5 is an enlarged partial top plan view thereof;

FIG. 6 is an enlarged partial front elevational view thereof; and,

FIG. 7 is an enlarged partial right side elevational view thereof.

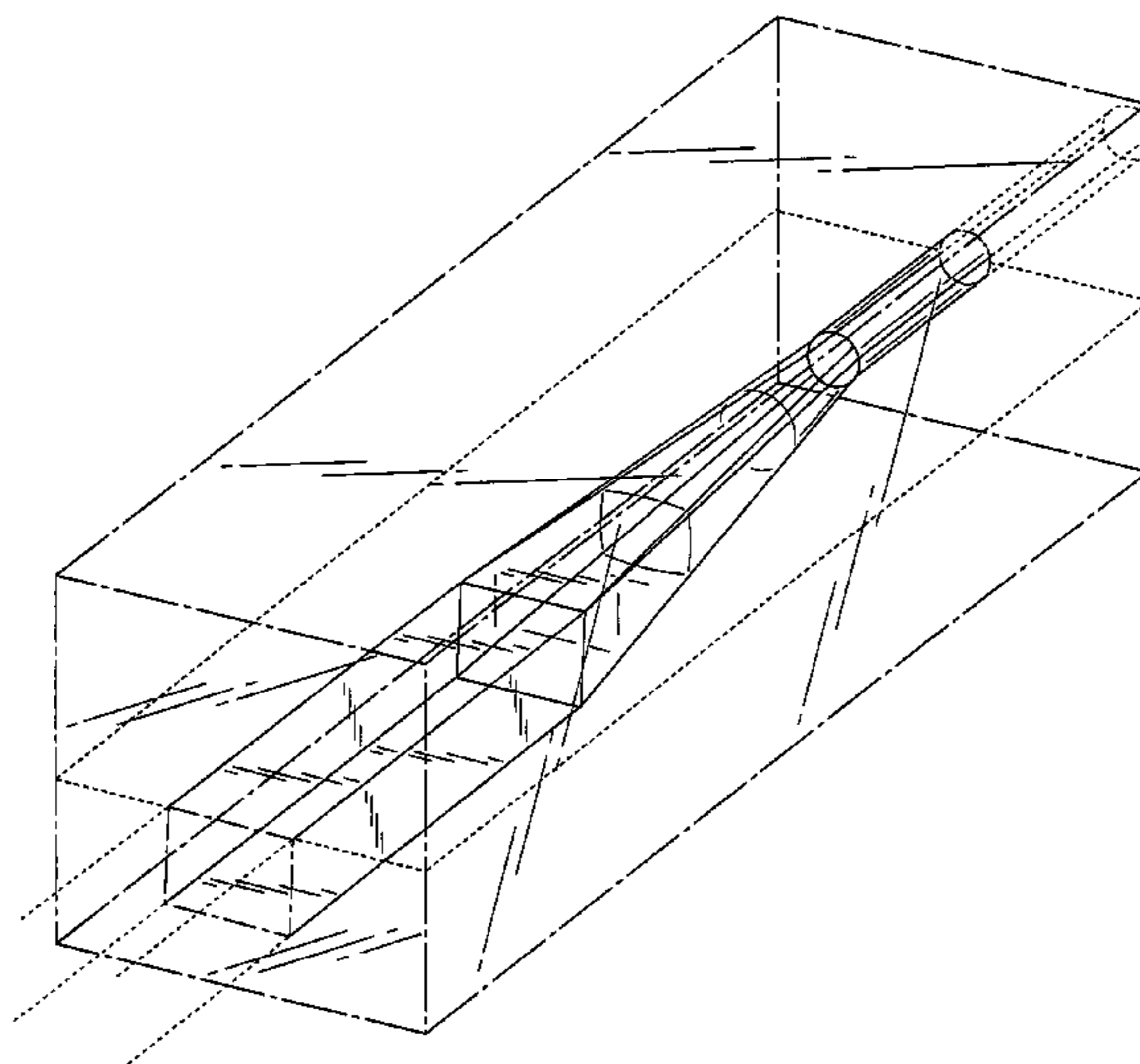
In the drawing views, the dot-dash broken lines represent the bounds of the claim, and all other broken lines are included for the purpose of illustrating portions of the micro flow channel chip that form no part of the claimed design. None of the broken lines form a part of the claimed design.

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**1 Claim, 4 Drawing Sheets**



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FIG.1

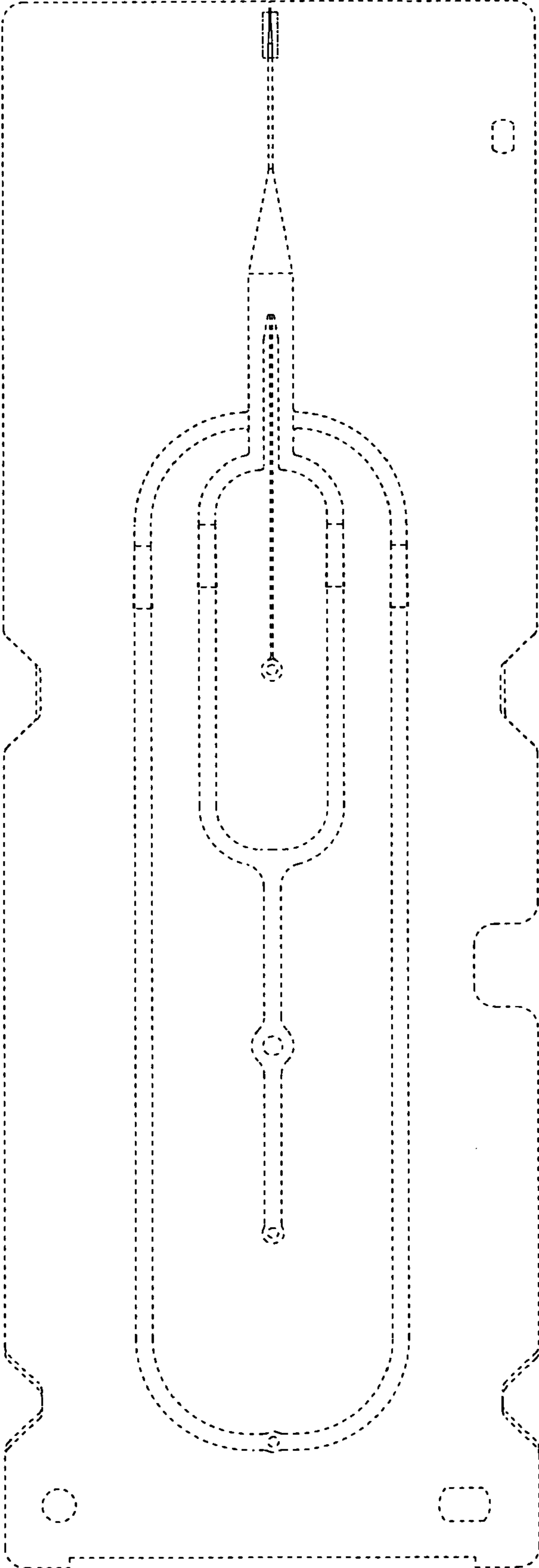


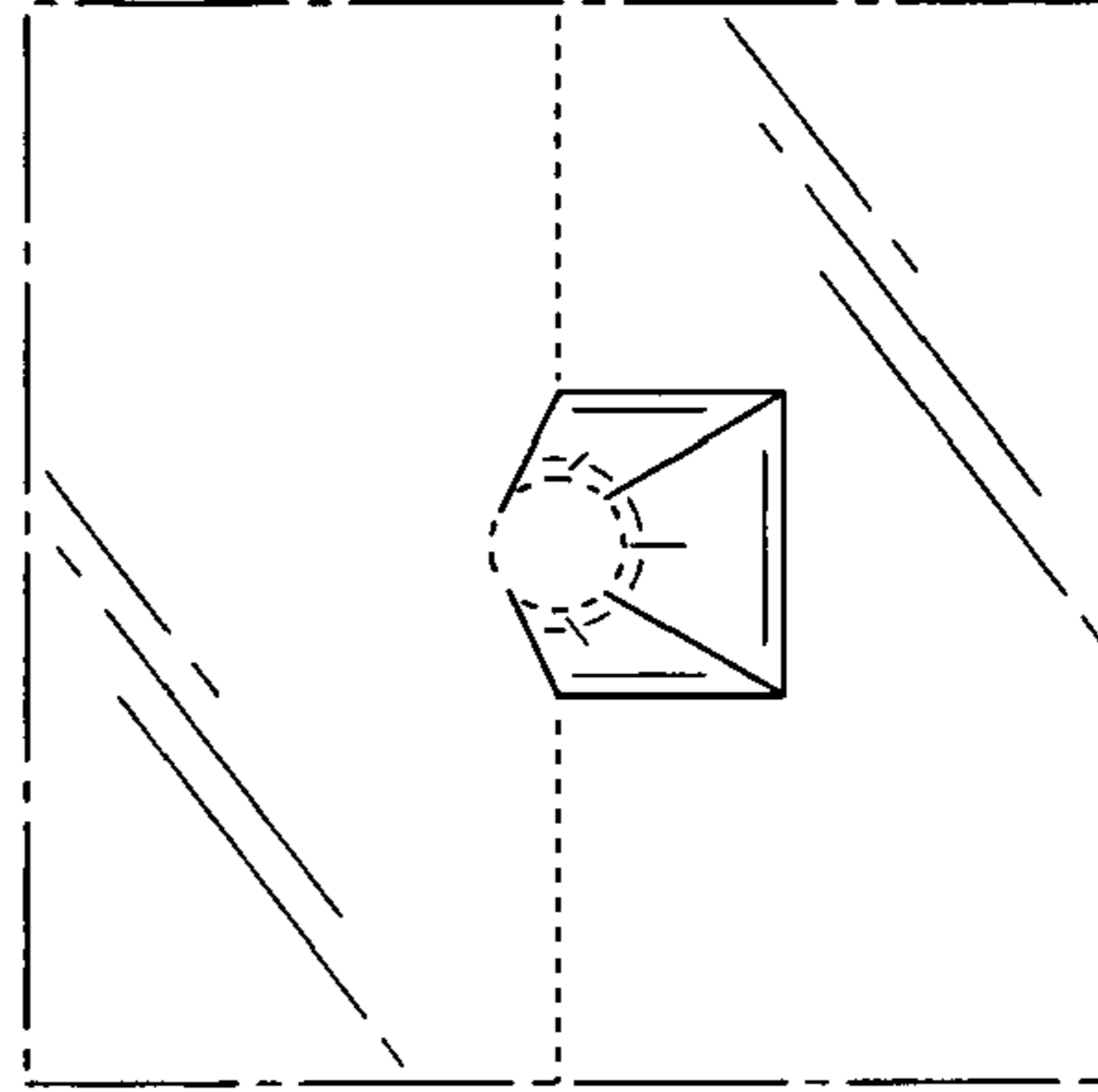
FIG.2



FIG.3



FIG.7



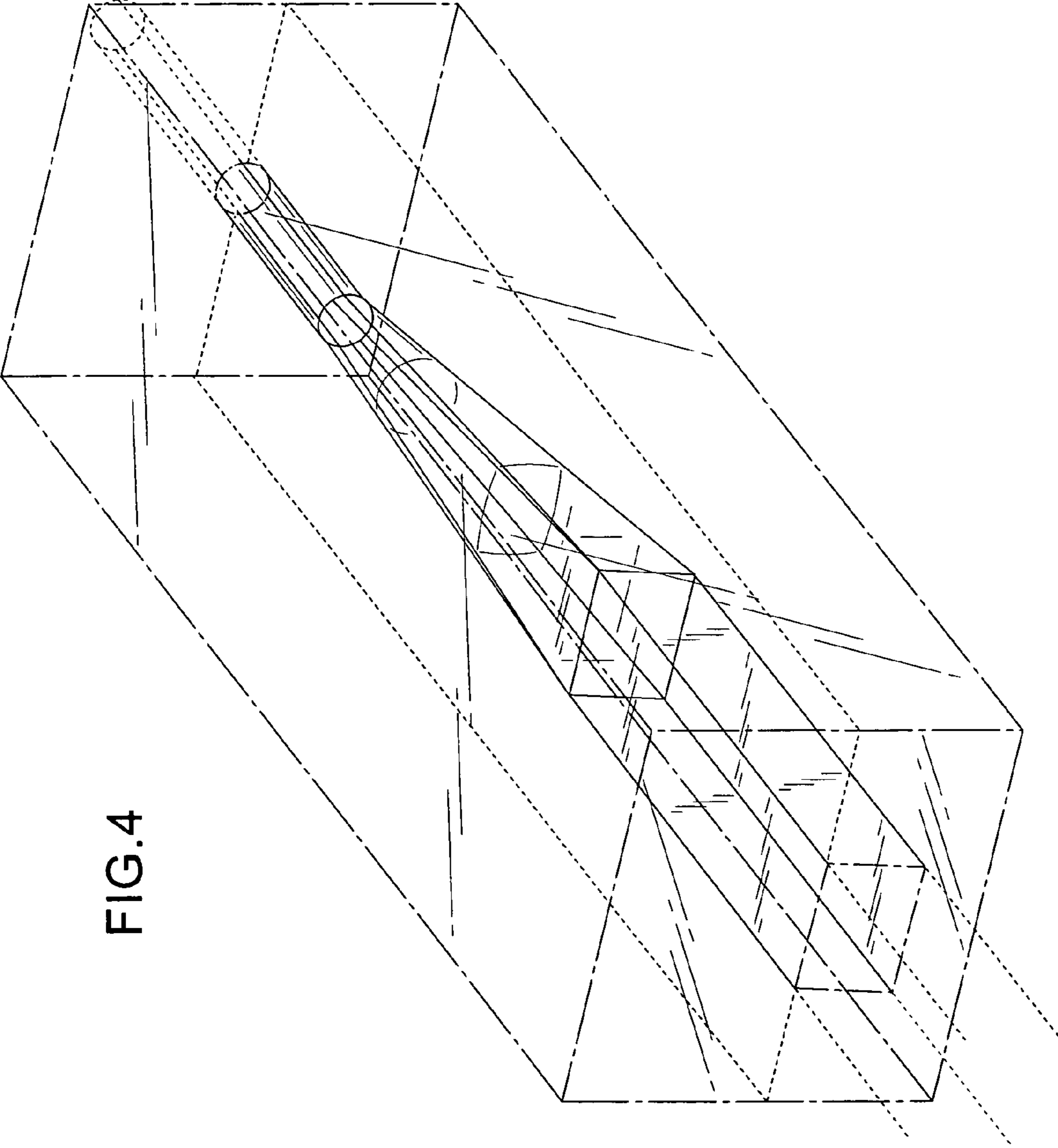


FIG.4

FIG.5

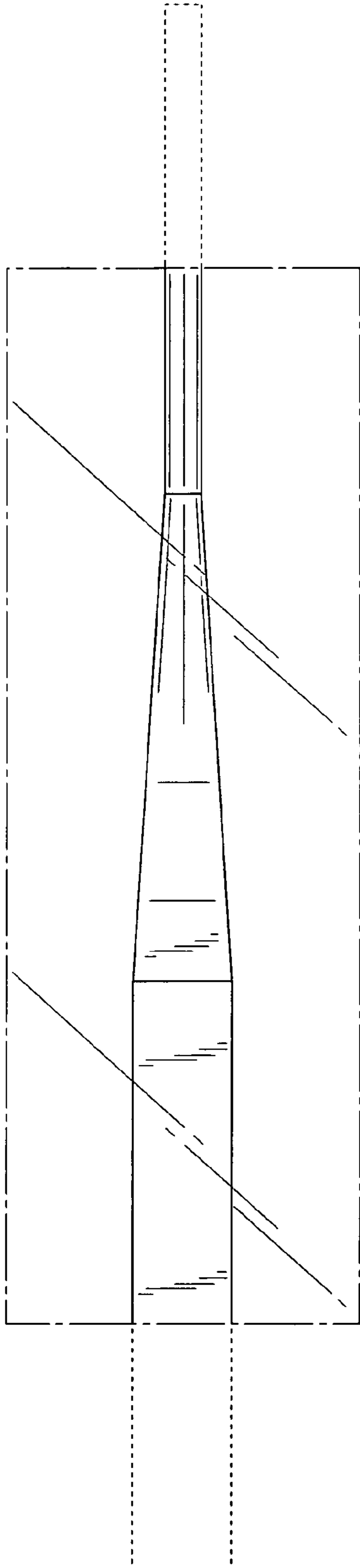


FIG.6

