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(12) **United States Design Patent**
Laurino et al.

(10) **Patent No.:** **US D661,605 S**
(45) **Date of Patent:** **** Jun. 12, 2012**

- (54) **VOLTAGE DETECTOR**
- (75) Inventors: **Ferdinand Laurino**, Seattle, WA (US);
Jeff Worones, Seattle, WA (US)
- (73) Assignee: **Fluke Corporation**, Everett, WA (US)
- (**) Term: **14 Years**
- (21) Appl. No.: **29/397,647**
- (22) Filed: **Jul. 19, 2011**

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Related U.S. Application Data

- (62) Division of application No. 29/359,070, filed on Apr. 5, 2010, now Pat. No. Des. 642,943.
- (51) **LOC (9) Cl.** **10-04**
- (52) **U.S. Cl.** **D10/78**
- (58) **Field of Classification Search** D10/78;
324/555, 66, 72, 754, 114, 115, 141, 145,
324/156, 508, 72.5, 556, 133, 149, 503, 543;
340/635, 687, 654; 379/21; 73/866.5
See application file for complete search history.

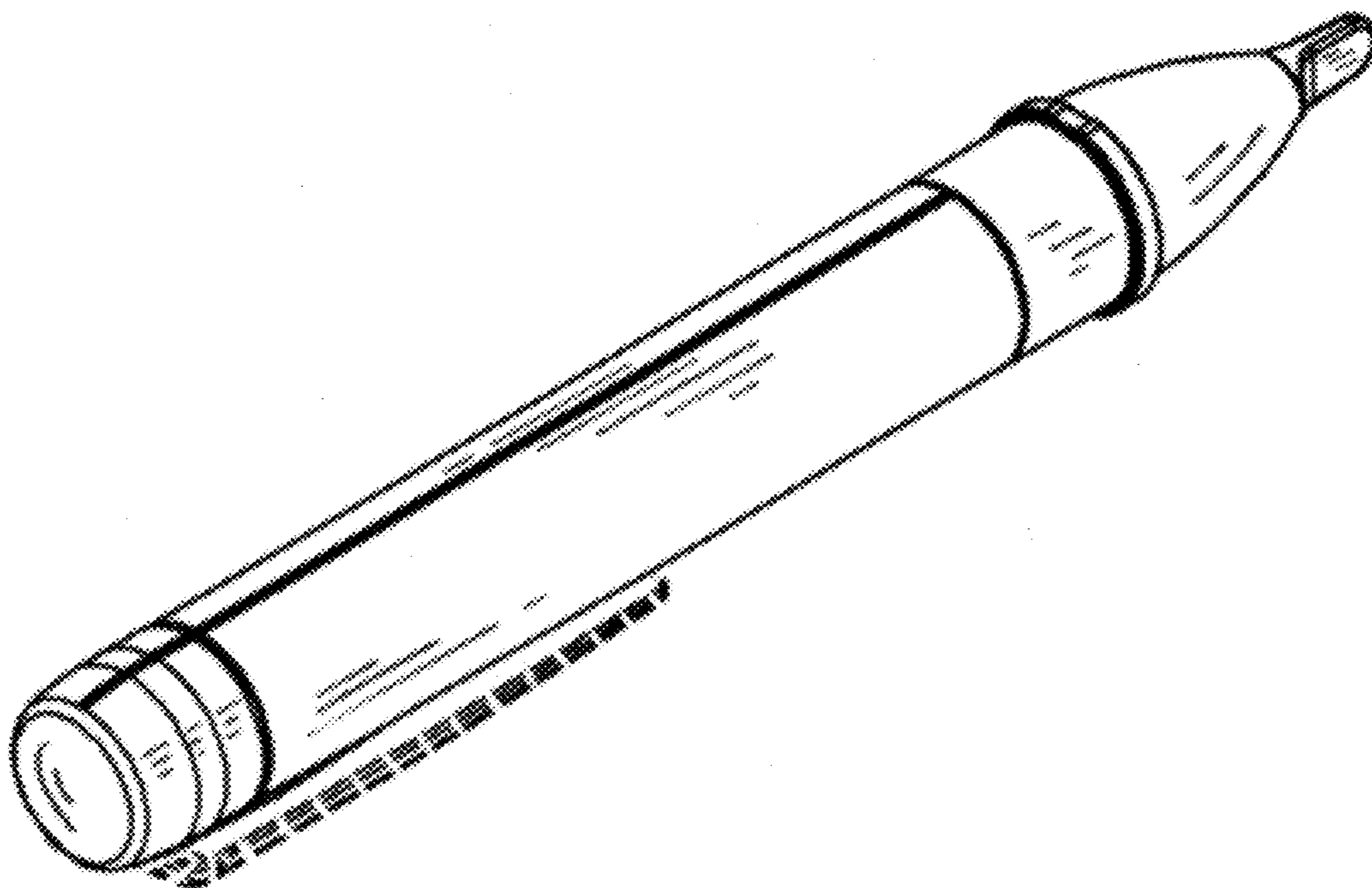
(57) **CLAIM**
The ornamental design for a voltage detector, as shown and described.

DESCRIPTION

FIG. 1 is a back view of a voltage detector.
FIG. 2 is a left side view thereof.
FIG. 3 is a front view thereof.
FIG. 4 is a right side view thereof.
FIG. 5 is a top view thereof.
FIG. 6 is a bottom view thereof.
FIG. 7 is a first perspective view thereof; and,
FIG. 8 is a second perspective view thereof.
The broken line showing of structural features is included for the purpose of illustrating non-claimed subject matter and forms no part of the claimed design.

- (56) **References Cited**
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1 Claim, 4 Drawing Sheets



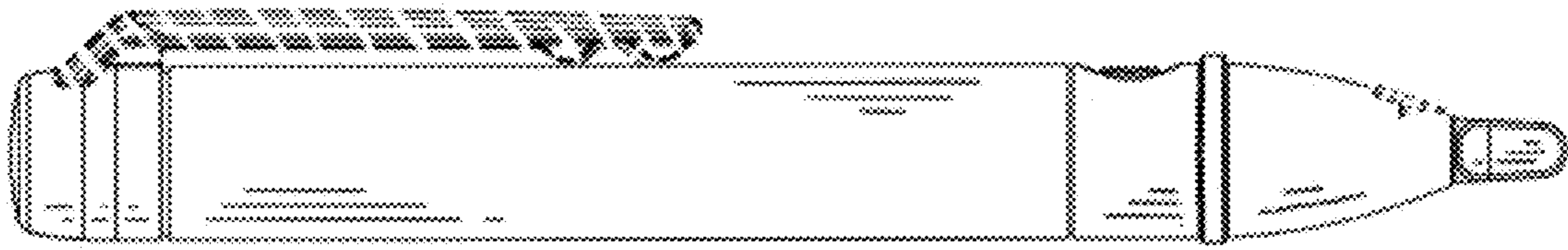


Figure 1

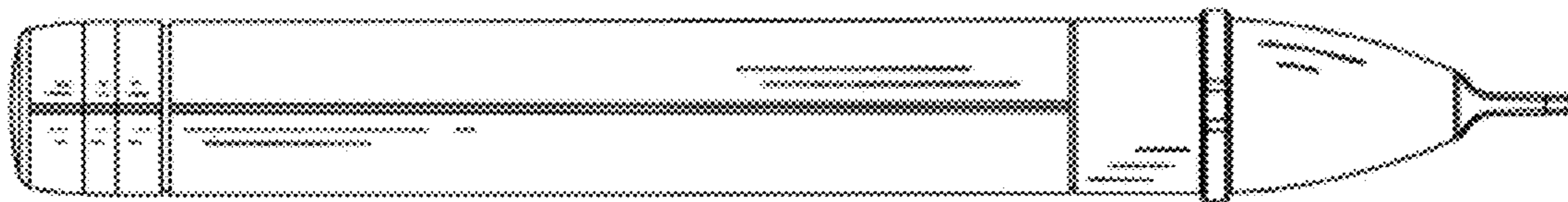


Figure 2

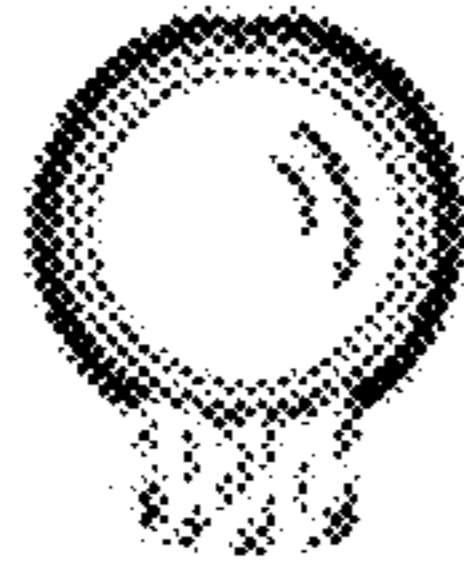


Figure 3

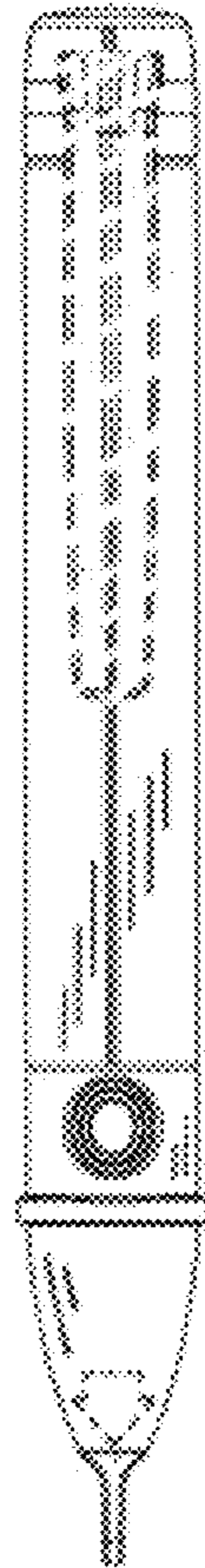


Figure 4

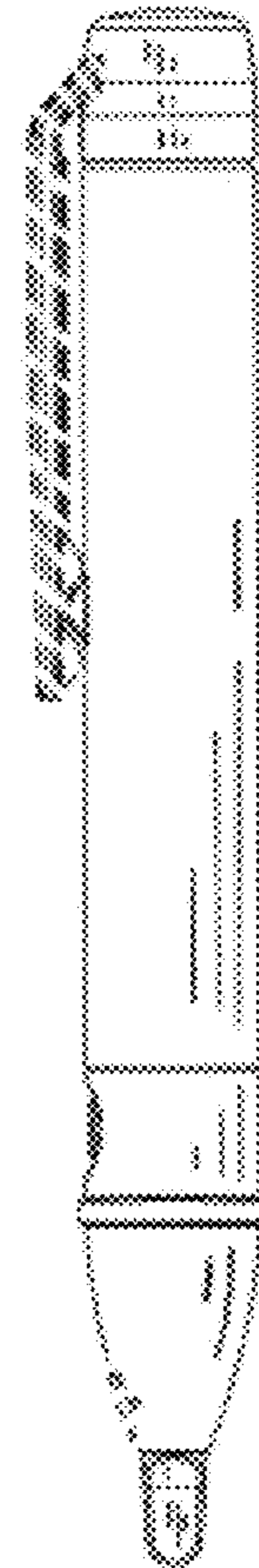
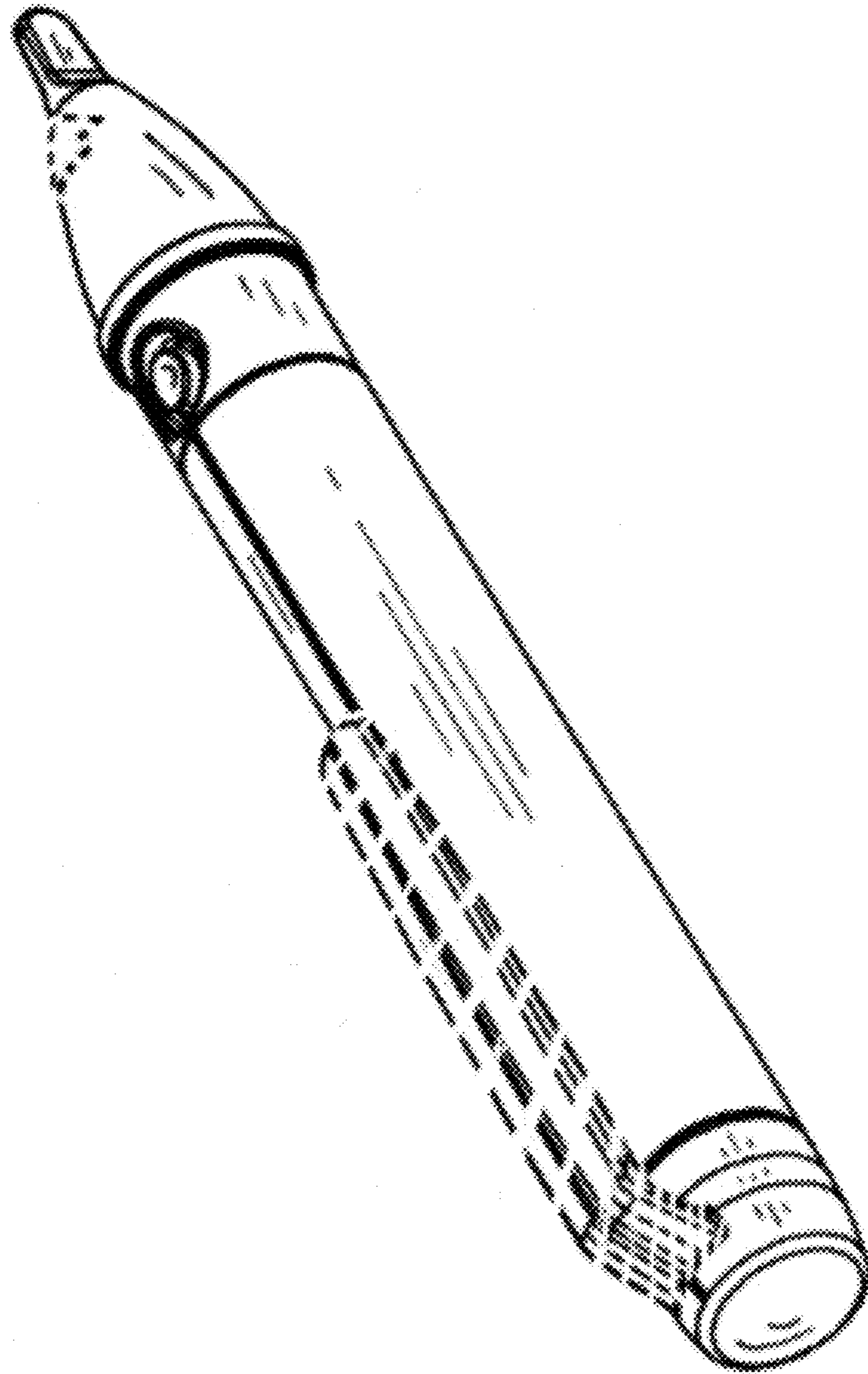


Figure 5



Figure 6

Figure 7



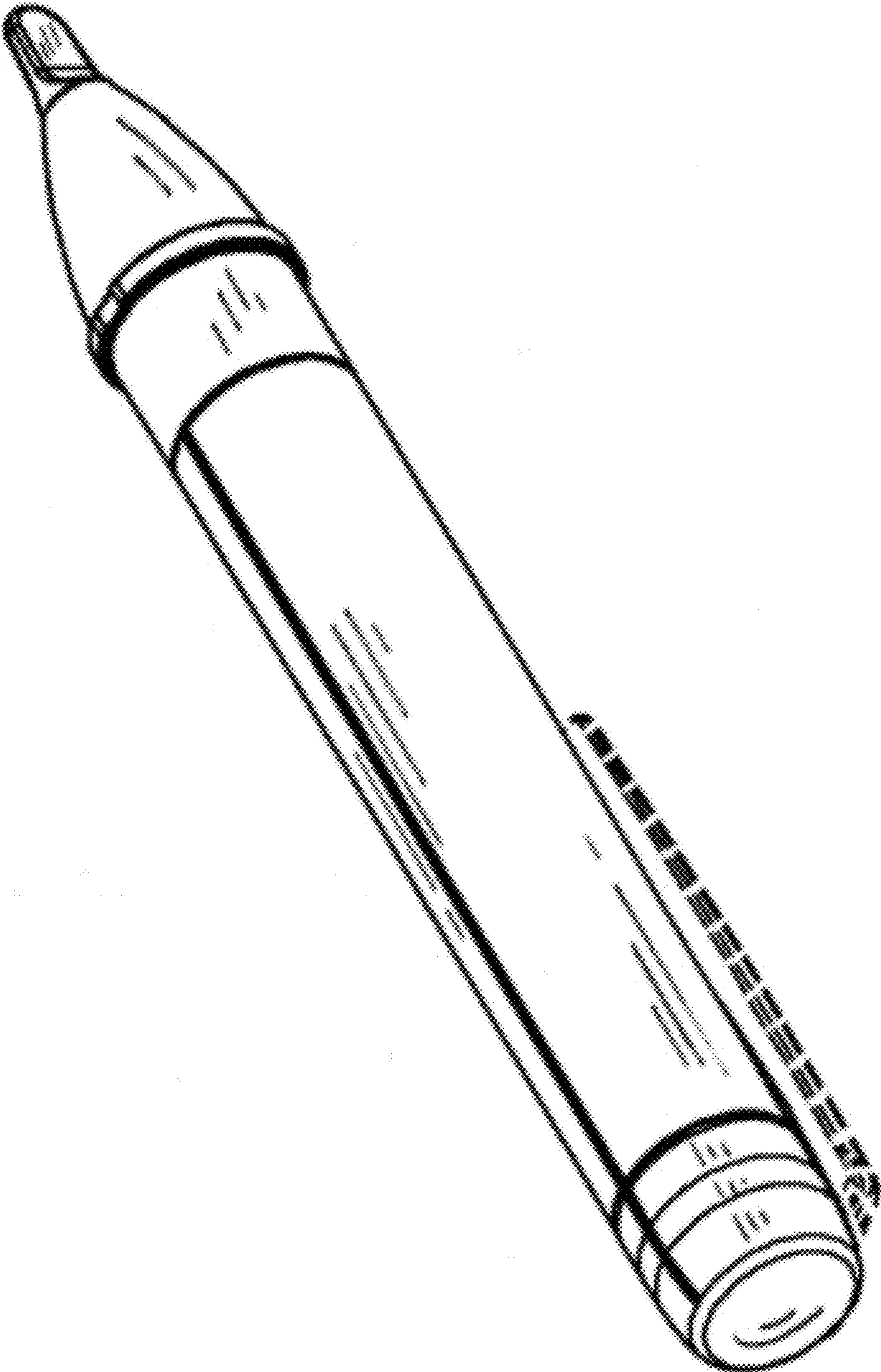


Figure 8