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(12) **United States Design Patent**
Honma et al.

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(45) **Date of Patent:** **** Feb. 28, 2012**

(54) **TOP PLATE FOR REACTOR FOR
MANUFACTURING SEMICONDUCTOR**

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D639,757 S * 6/2011 Root et al. D13/182

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* cited by examiner

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(**) Term: **14 Years**

(57) **CLAIM**

The ornamental design for top plate for reactor for manufacturing semiconductor, as shown and described.

(21) Appl. No.: **29/389,558**

(22) Filed: **Apr. 13, 2011**

DESCRIPTION

(30) **Foreign Application Priority Data**

Oct. 21, 2010 (JP) 2010-025238

(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
D7/585; 174/250, 253, 255; 257/690, 692,
257/697, 695, 748, 786, 773; 361/777; 29/829
See application file for complete search history.

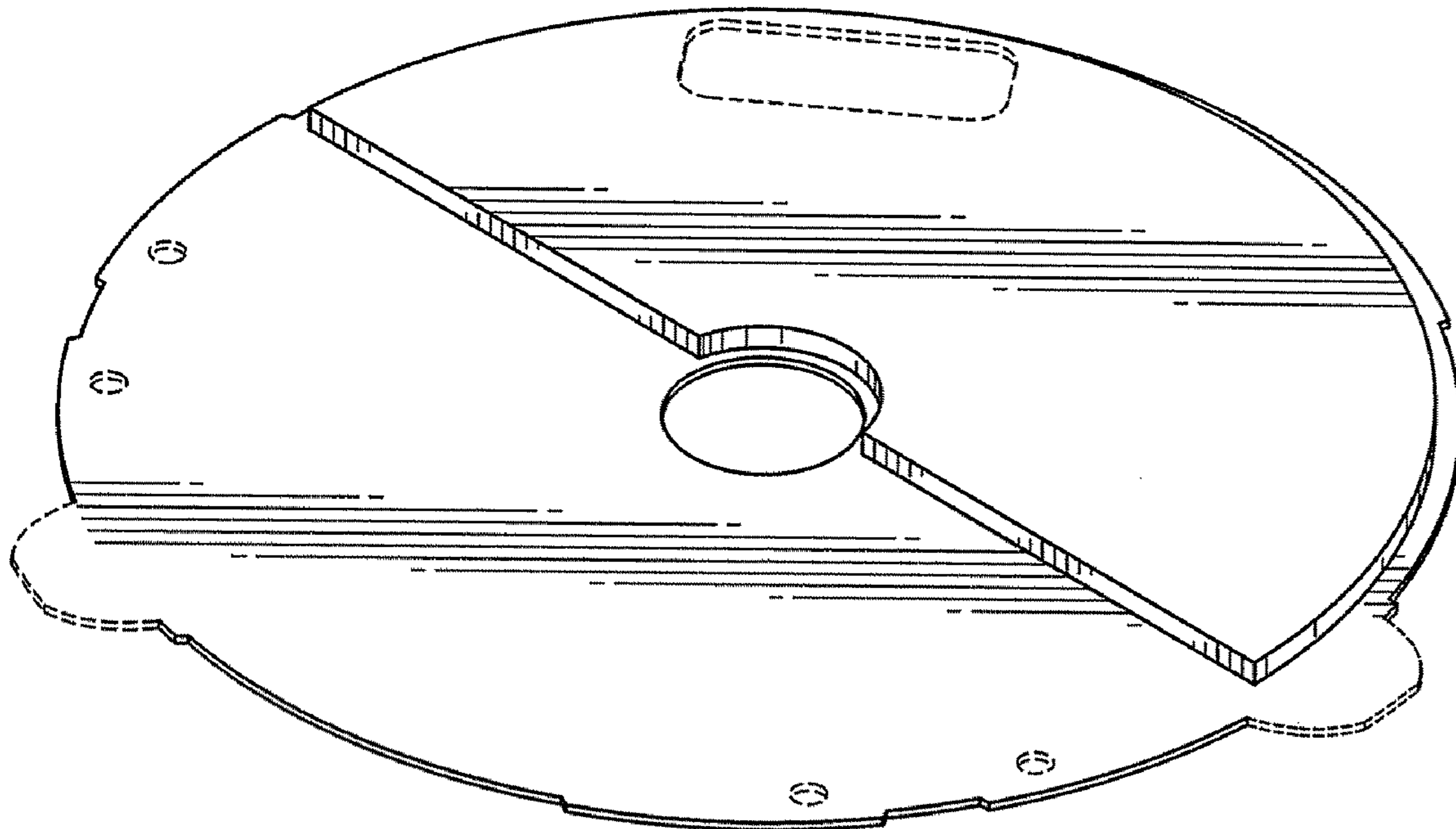
FIG. 1 is front perspective view of a top plate for reactor for manufacturing semiconductor illustrating our new design; FIG. 2 is a front view thereof; FIG. 3 is a rear view thereof; FIG. 4 is a right side view thereof; FIG. 5 is a left side view thereof; FIG. 6 is a top plan view thereof; FIG. 7 is a bottom view thereof; FIG. 8 is a reference front view indicating the plane upon which a sectional view is taken; and, FIG. 9 is a sectional view taken along line 9-9-9 of FIG. 8. The broken lines are shown for illustrative purposes only and form no part of the claimed design.

(56) **References Cited**

U.S. PATENT DOCUMENTS

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D614,593 S * 4/2010 Lee et al. D13/182

1 Claim, 5 Drawing Sheets



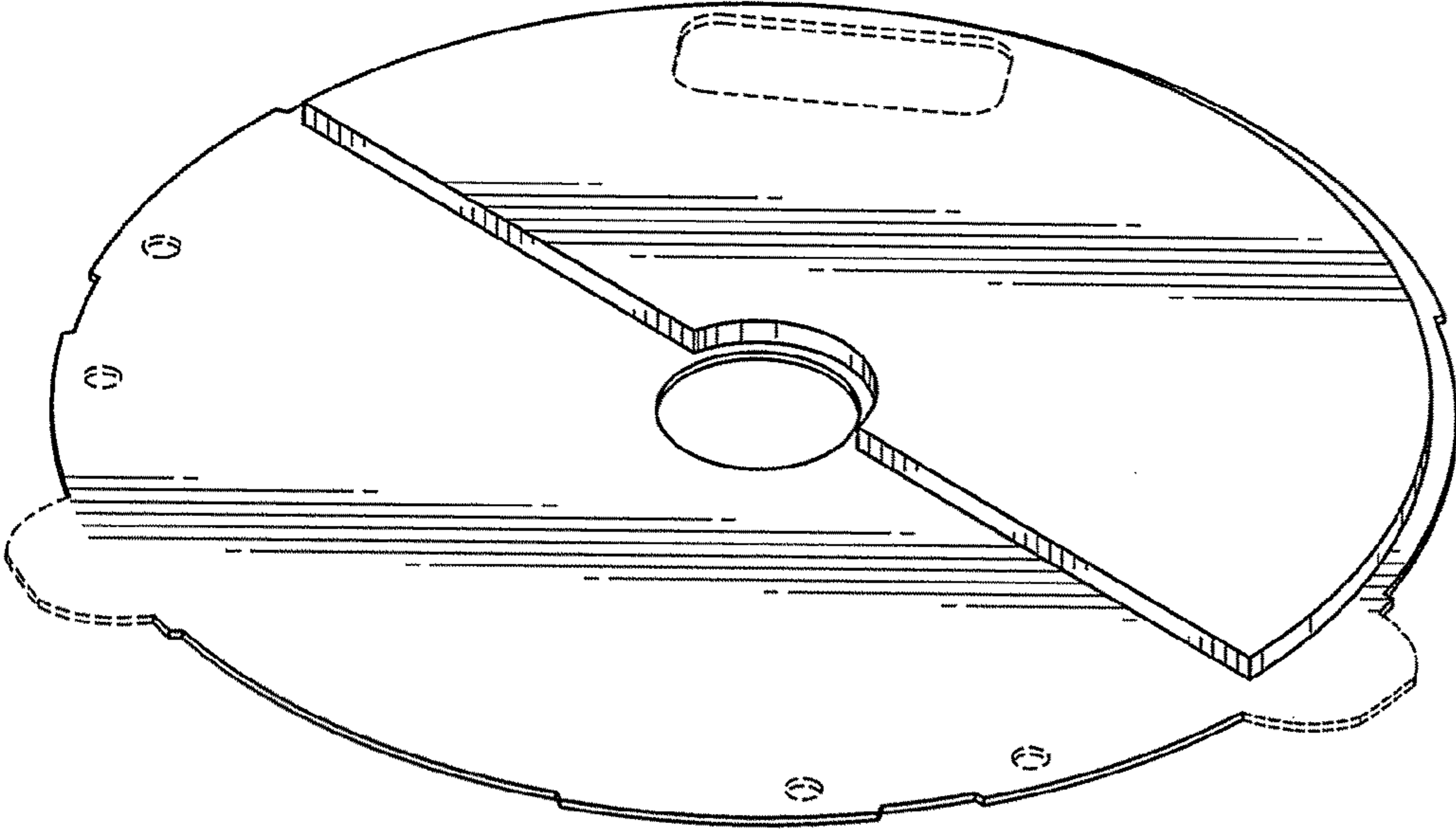


FIG. 1

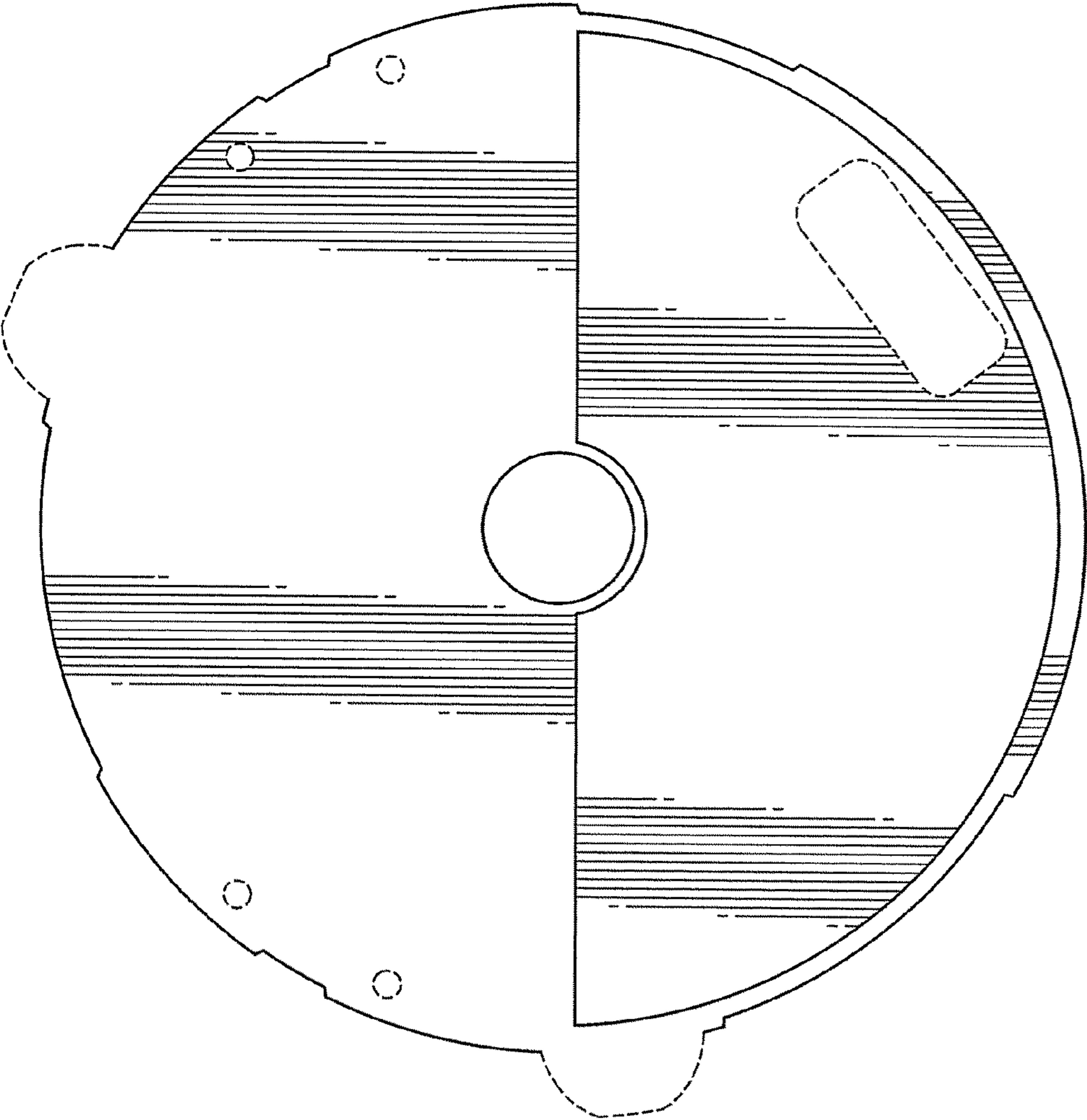


FIG. 2

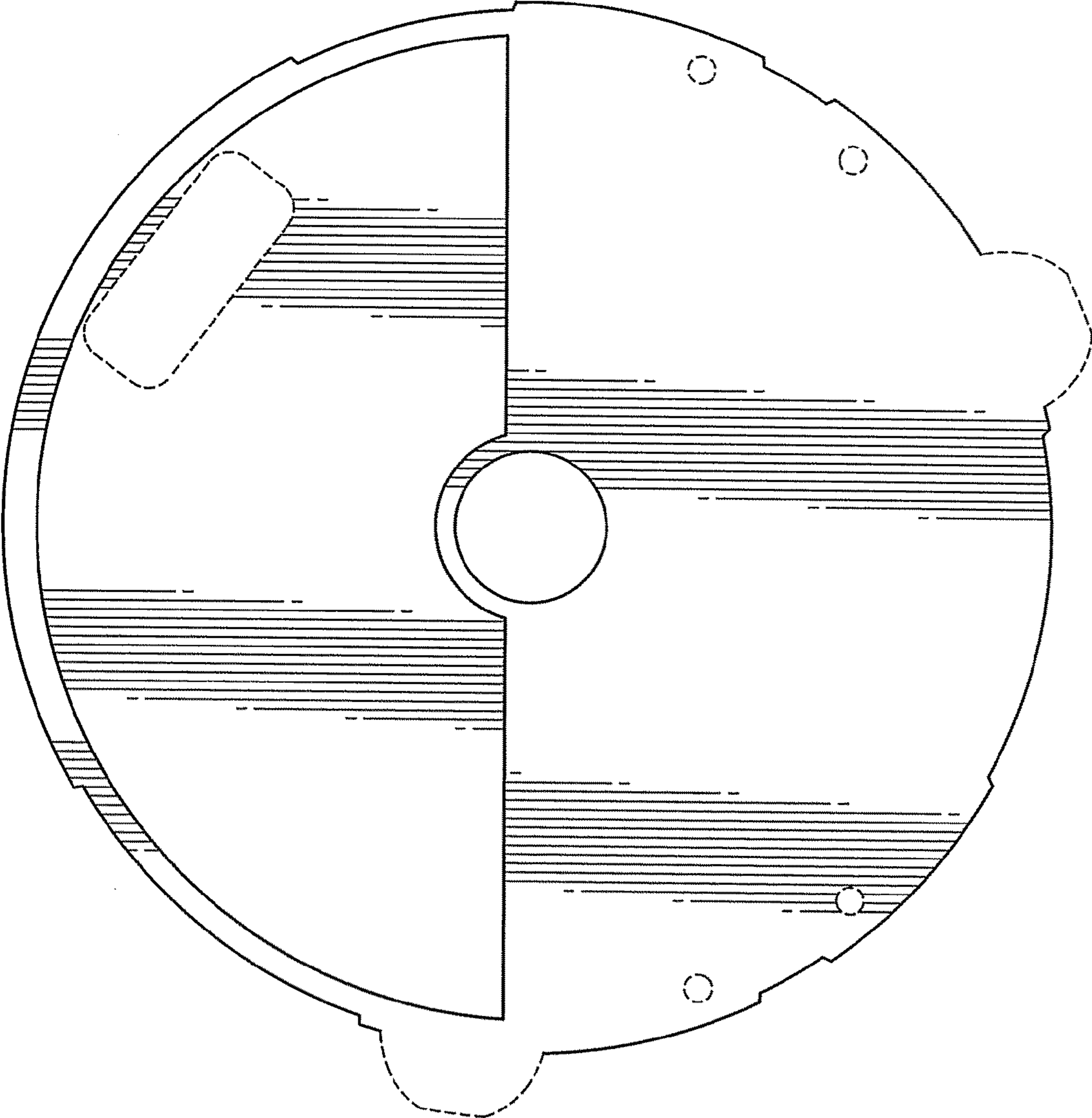


FIG. 3



FIG. 4



FIG. 5

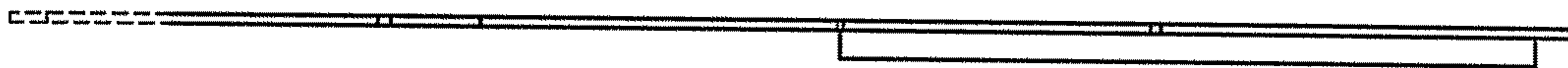


FIG. 6

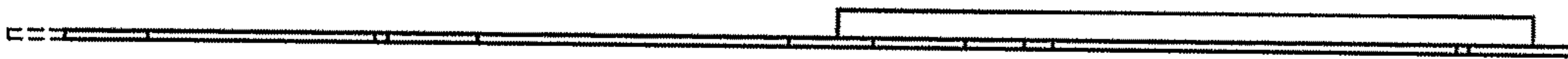


FIG. 7

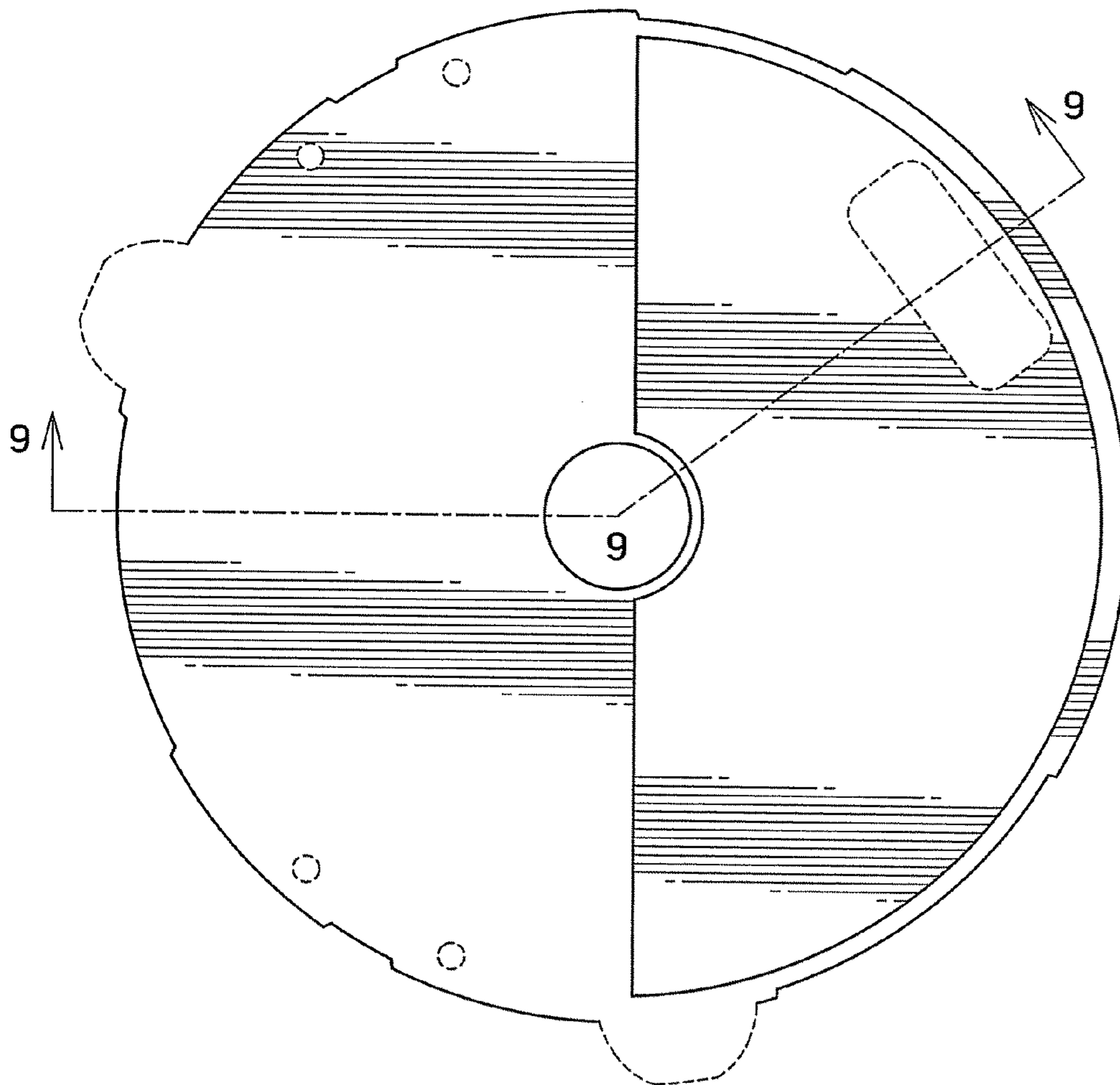


FIG. 8

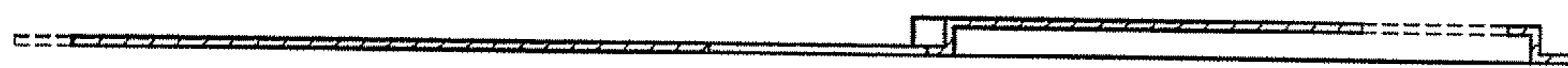


FIG. 9