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(12) **United States Design Patent**  
**Nishiguchi et al.**

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(54) **SEMICONDUCTOR SUBSTRATE**

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(\*\*) Term: **14 Years**

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(51) **LOC (9) Cl.** ..... **13-03**

(52) **U.S. Cl.** ..... **D13/182**

(58) **Field of Classification Search** ..... D13/182;  
D6/300, 309; D7/541; D9/428, 433, 456;  
D25/103, 109, 138-140, 155-157; 117/95;  
257/77, 255, 627, 628; 438/149, 150, 689-692,  
438/697

See application file for complete search history.

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(57) **CLAIM**

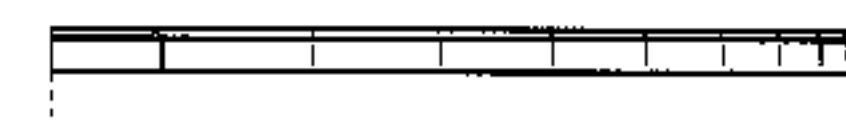
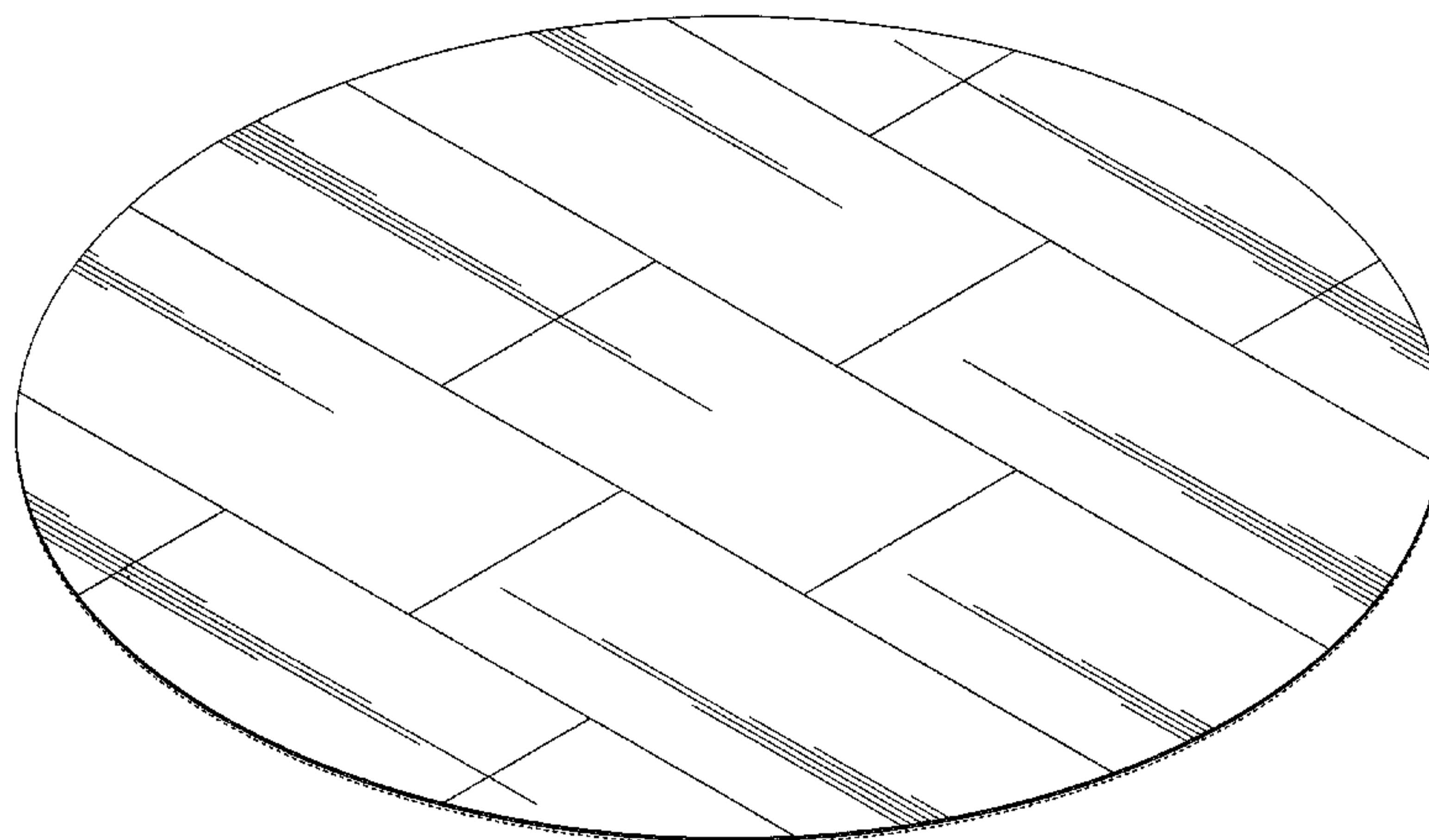
The ornamental design for a semiconductor substrate, as shown and described.

**DESCRIPTION**

FIG. 1 is a front, right, and top perspective view of a semiconductor substrate showing our new design;  
 FIG. 2 is a front view thereof, a rear view being a mirror image thereof;  
 FIG. 3 is a top plan view thereof;  
 FIG. 4 is a bottom plan view thereof;  
 FIG. 5 is a right-side view thereof, a left side view being a mirror image thereof;  
 FIG. 6 is a partially enlarged view at 6 shown in FIG. 2 thereof;  
 FIG. 7 is a partially enlarged view at 7 shown in FIG. 2 thereof;  
 FIG. 8 is an enlarged ended view at 8-8 shown in FIG. 3 thereof; and,  
 FIG. 9 is a partially enlarged sectional view at 9 shown in FIG. 8 thereof.

The broken line showing of the semiconductor substrate is for the purpose of illustrating environmental structure and forms no part of the claimed design.

**1 Claim, 5 Drawing Sheets**



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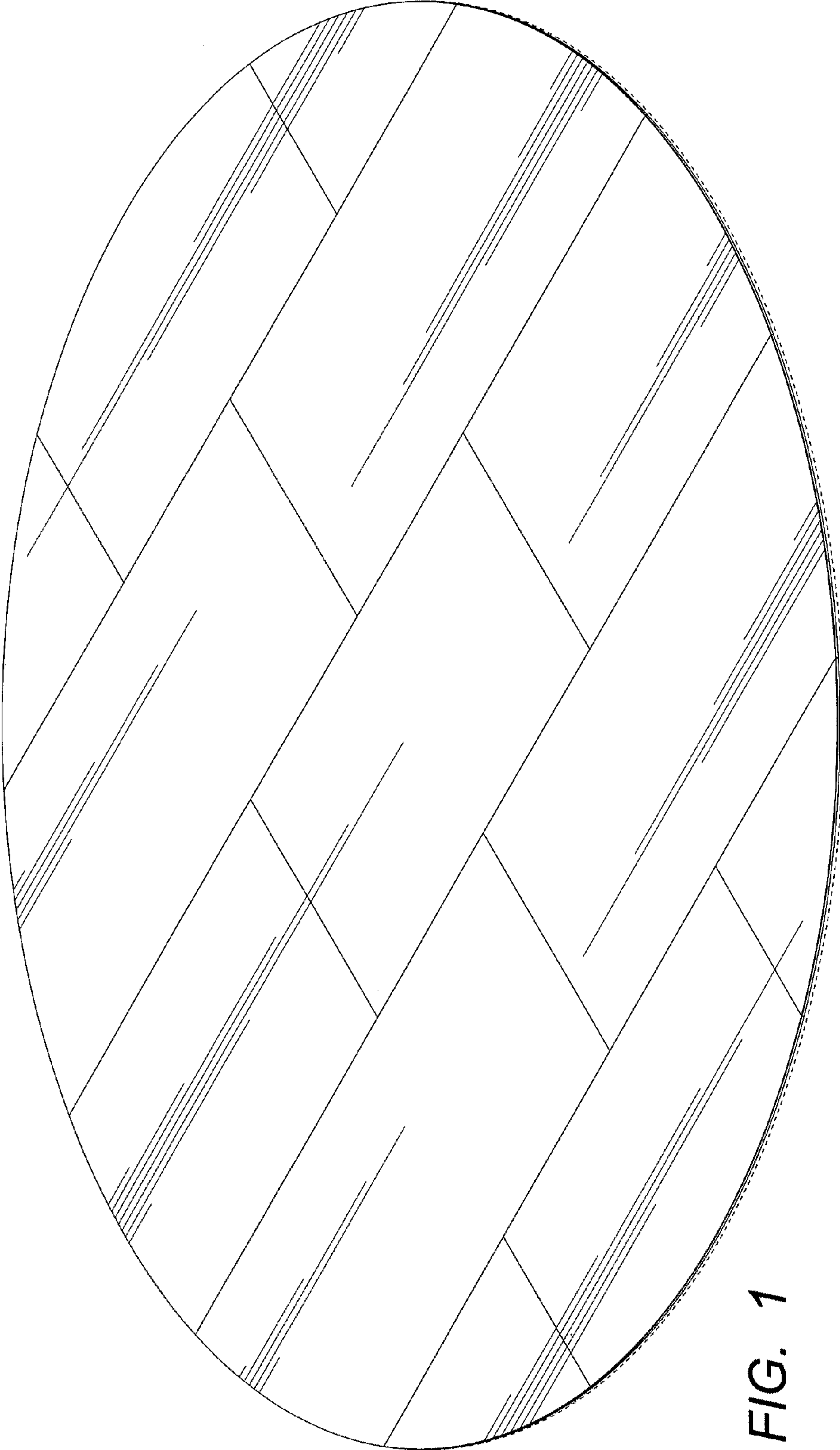


FIG. 1

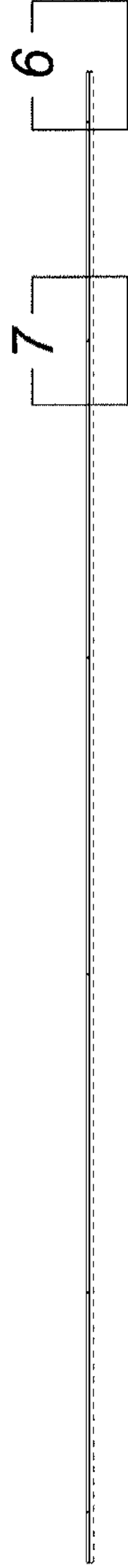


FIG. 2

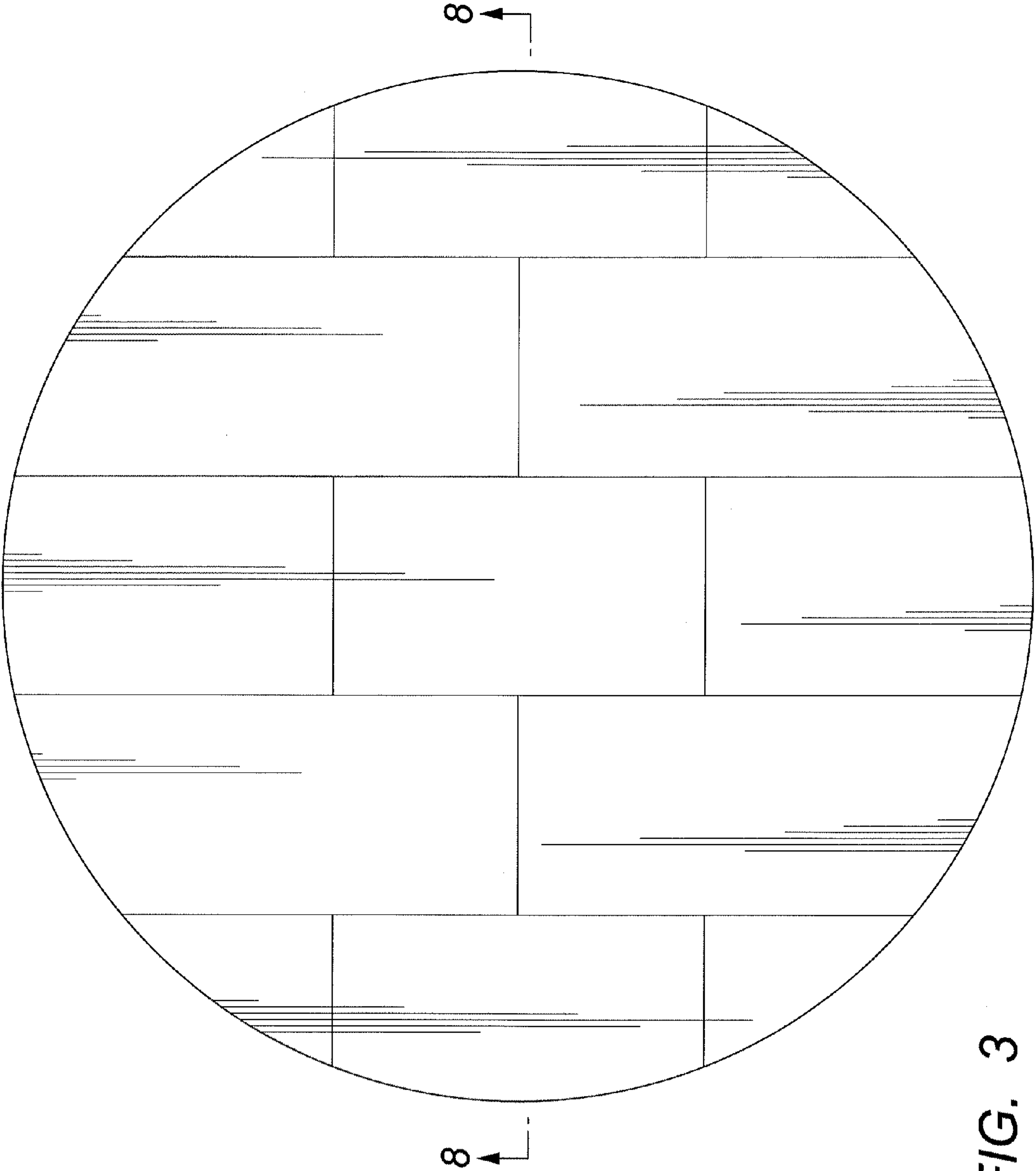
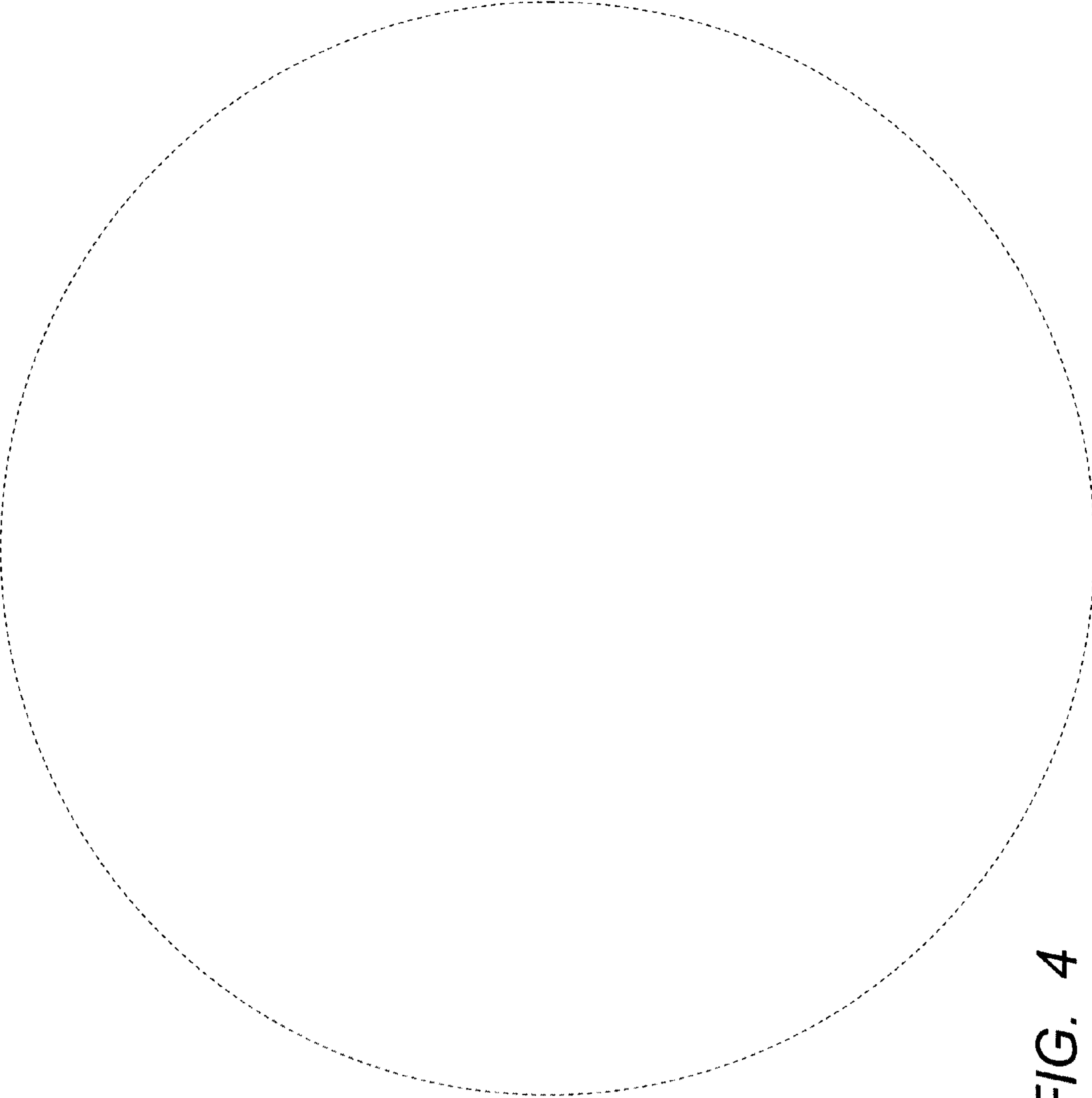


FIG. 3



**FIG. 4**



FIG. 5



FIG. 6

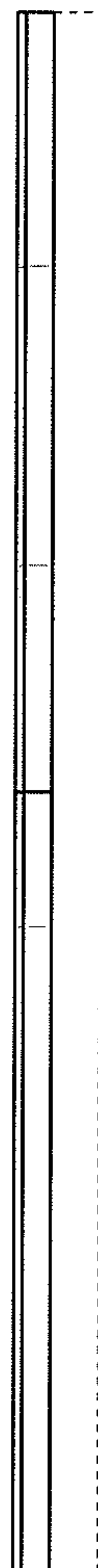


FIG. 7



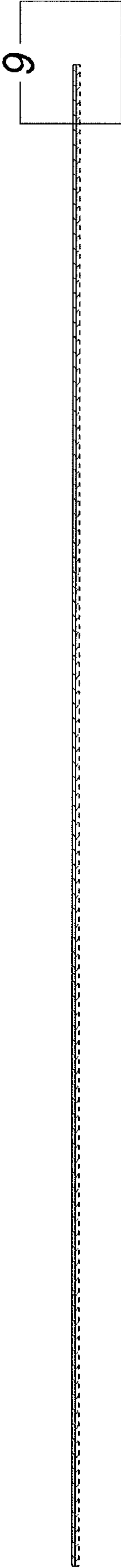


FIG. 8

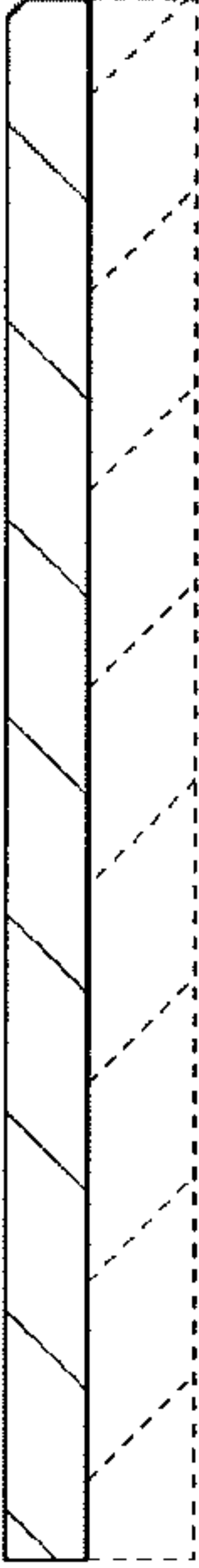


FIG. 9