



US00D648290S

(12) **United States Design Patent**
Mori

(10) **Patent No.:** **US D648,290 S**

(45) **Date of Patent:** **** Nov. 8, 2011**

(54) **SEMICONDUCTOR DEVICE**

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Hiroshima (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/380,499**

(22) Filed: **Dec. 7, 2010**

(30) **Foreign Application Priority Data**

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Jun. 8, 2010 (JP) 2010-014092

(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
174/528, 531, 533, 536, 537; 257/666, 670,
257/678, 690, 692, 734, 735

See application file for complete search history.

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Birch, LLP

(57) **CLAIM**

The ornamental design for a semiconductor device, as shown.

DESCRIPTION

FIG. 1 is a front view of a semiconductor device of a first embodiment showing my new design;

FIG. 2 is a rear view thereof;

FIG. 3 is a top plan view thereof;

FIG. 4 is a bottom plan view thereof;

FIG. 5 is a right side view thereof;

FIG. 6 is a left side view thereof;

FIG. 7 is a view showing front, left side and top plan thereof;

FIG. 8 is a view showing front, right side and bottom plan thereof;

FIG. 9 is a front view of a semiconductor device of a second embodiment showing my new design;

FIG. 10 is a rear view thereof;

FIG. 11 is a top plan view thereof;

FIG. 12 is a bottom plan view thereof;

FIG. 13 is a right side view thereof;

FIG. 14 is a left side view thereof;

FIG. 15 is a view showing front, left side and top plan thereof; and,

FIG. 16 is a view showing front, right side and bottom plan thereof.

1 Claim, 6 Drawing Sheets

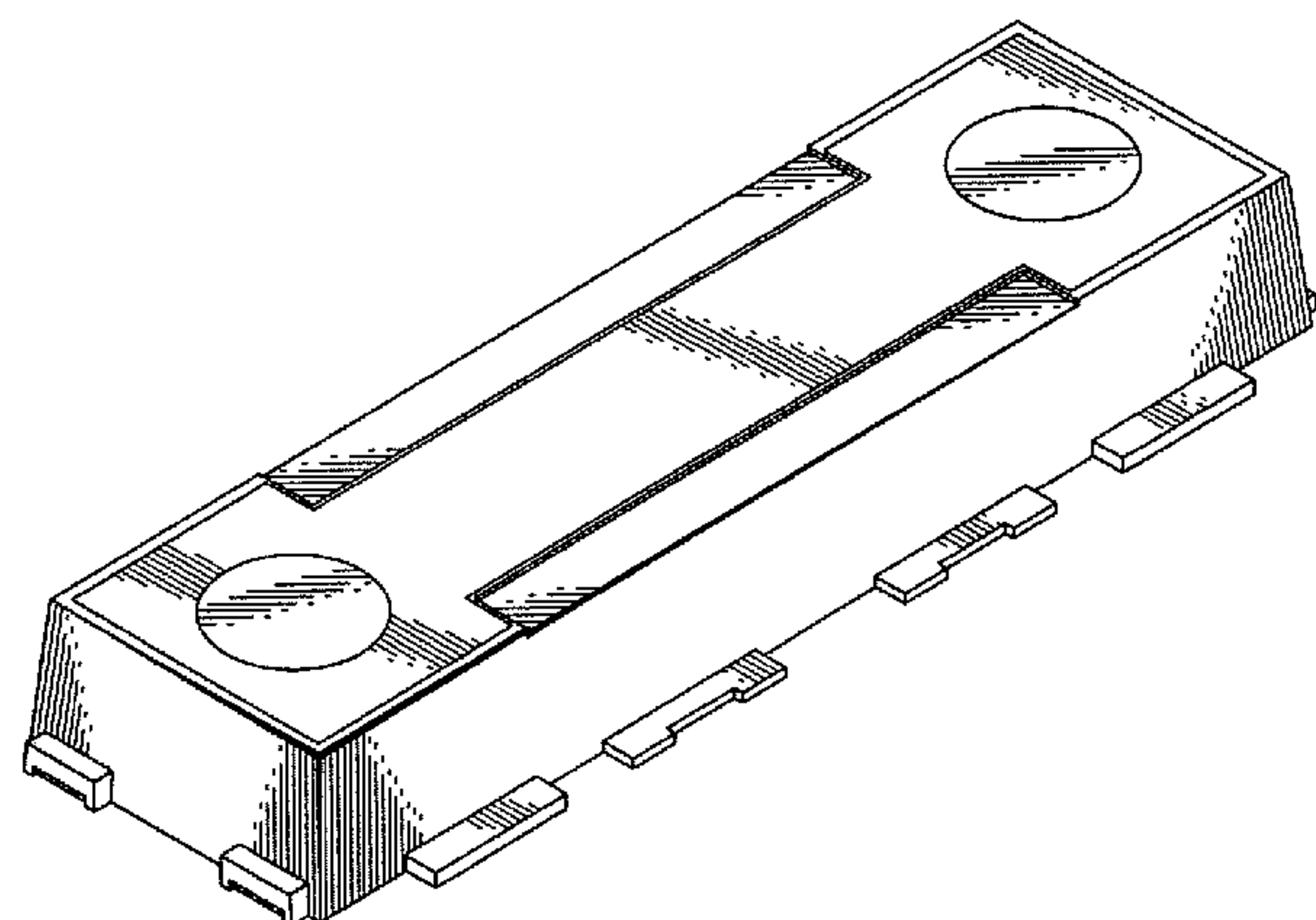
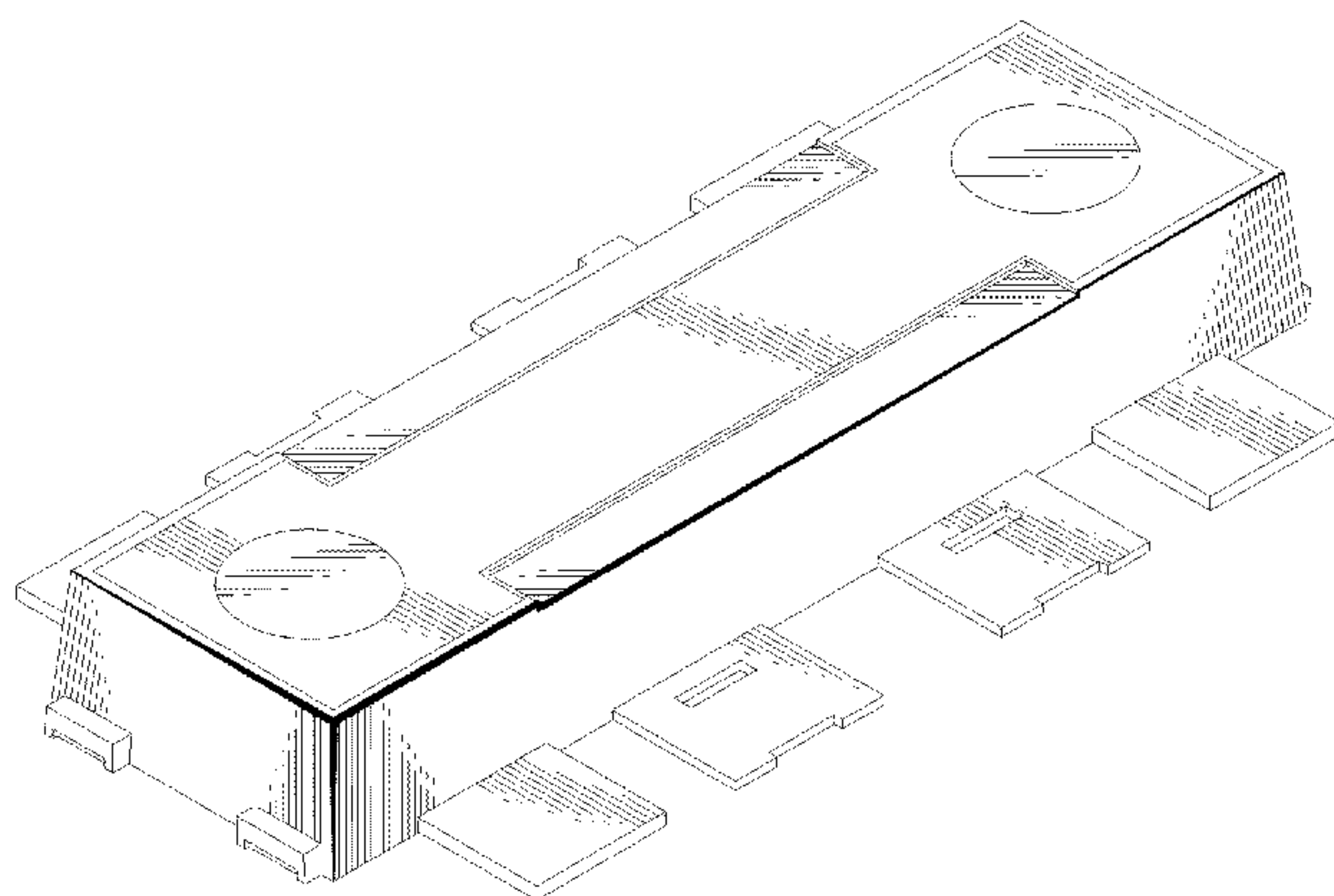


FIG.1

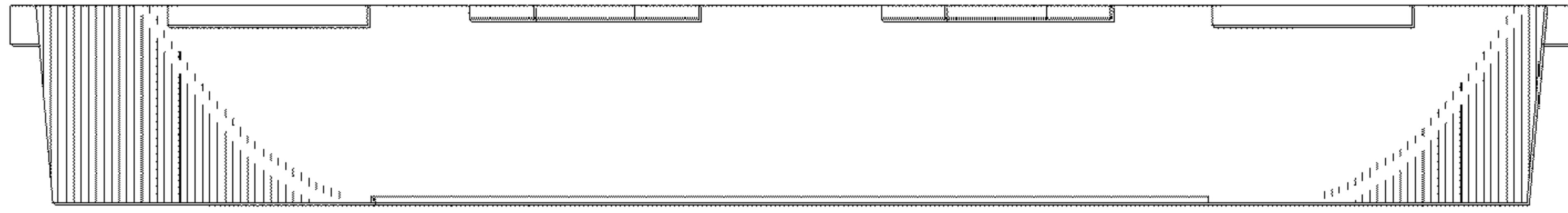


FIG.2

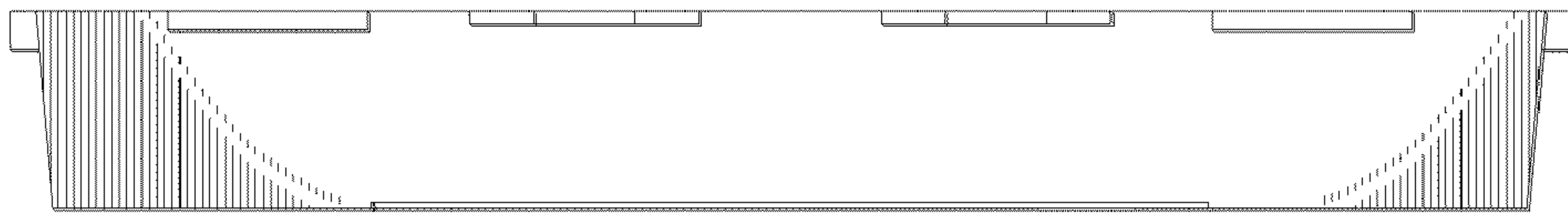


FIG.3

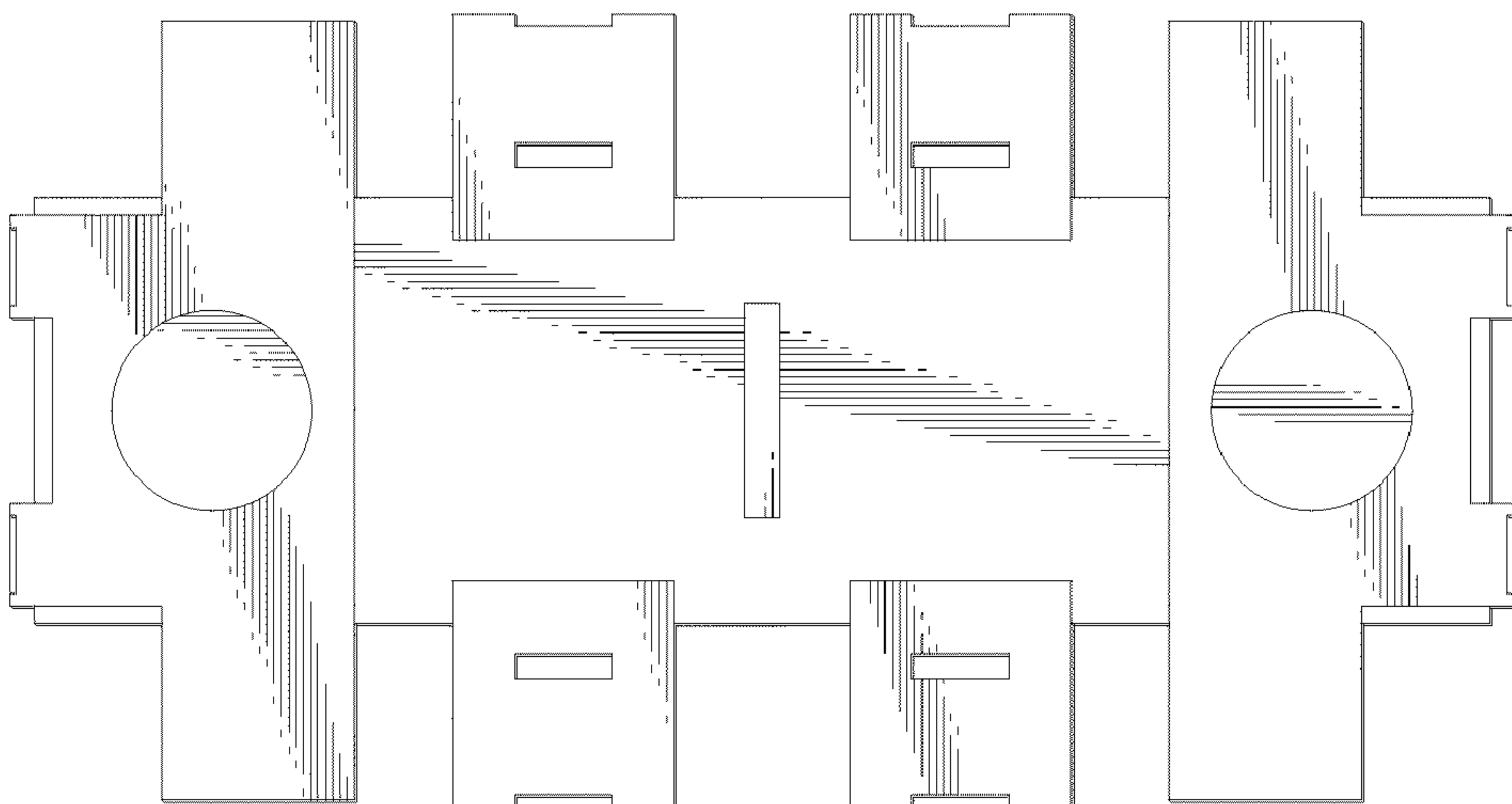


FIG.4

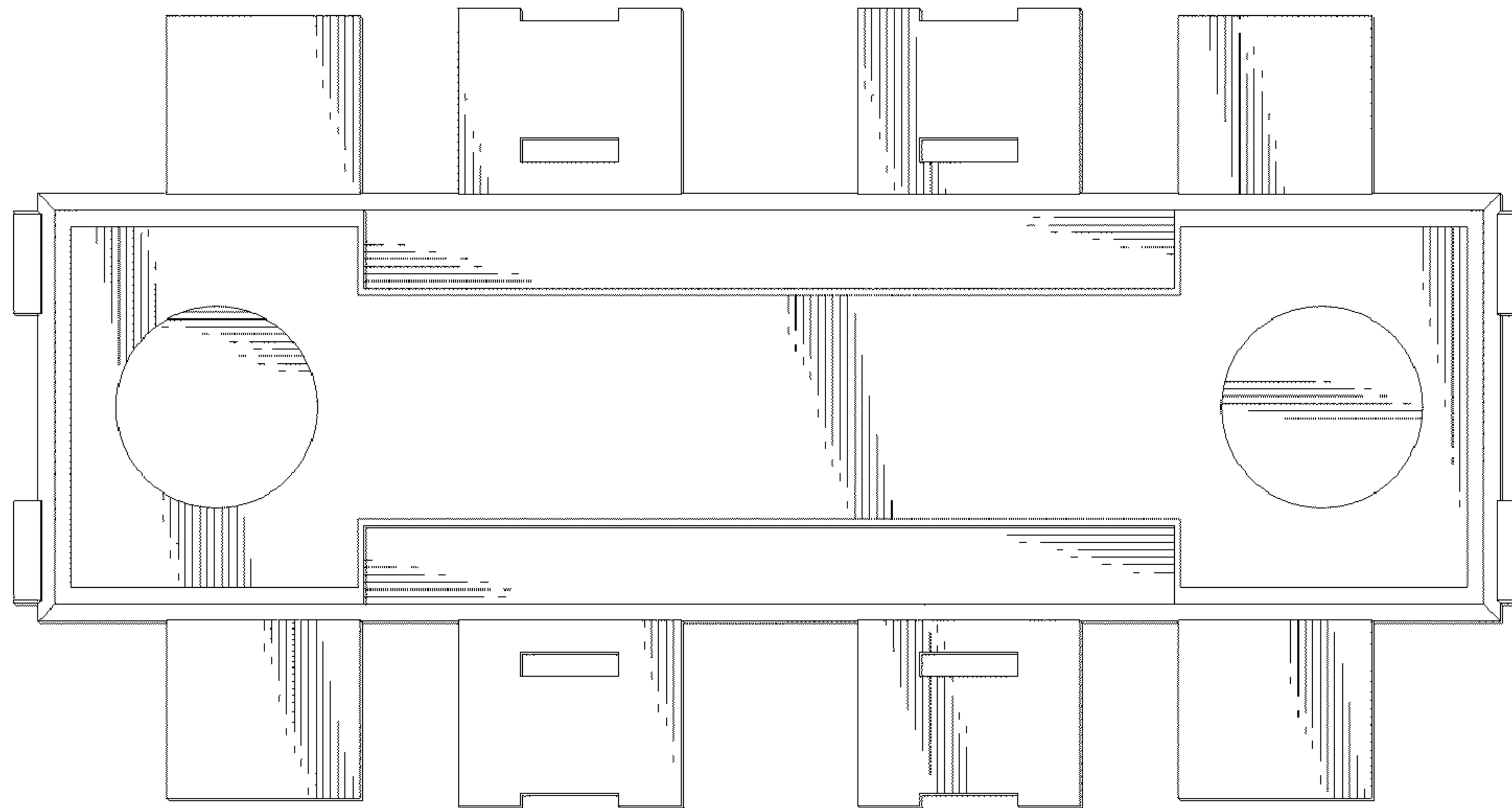


FIG.5

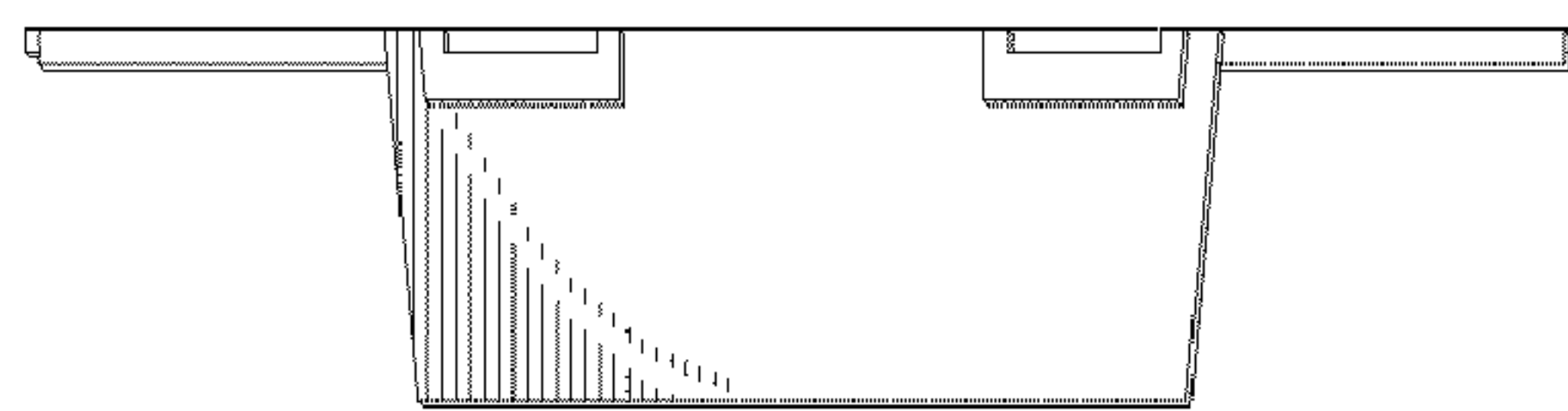


FIG.6

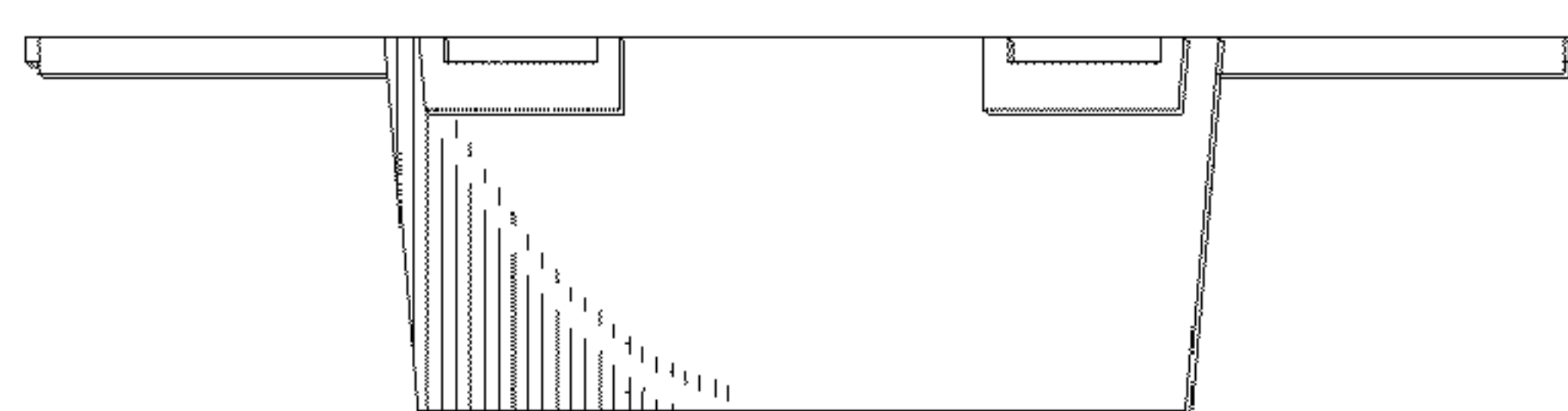


FIG.7

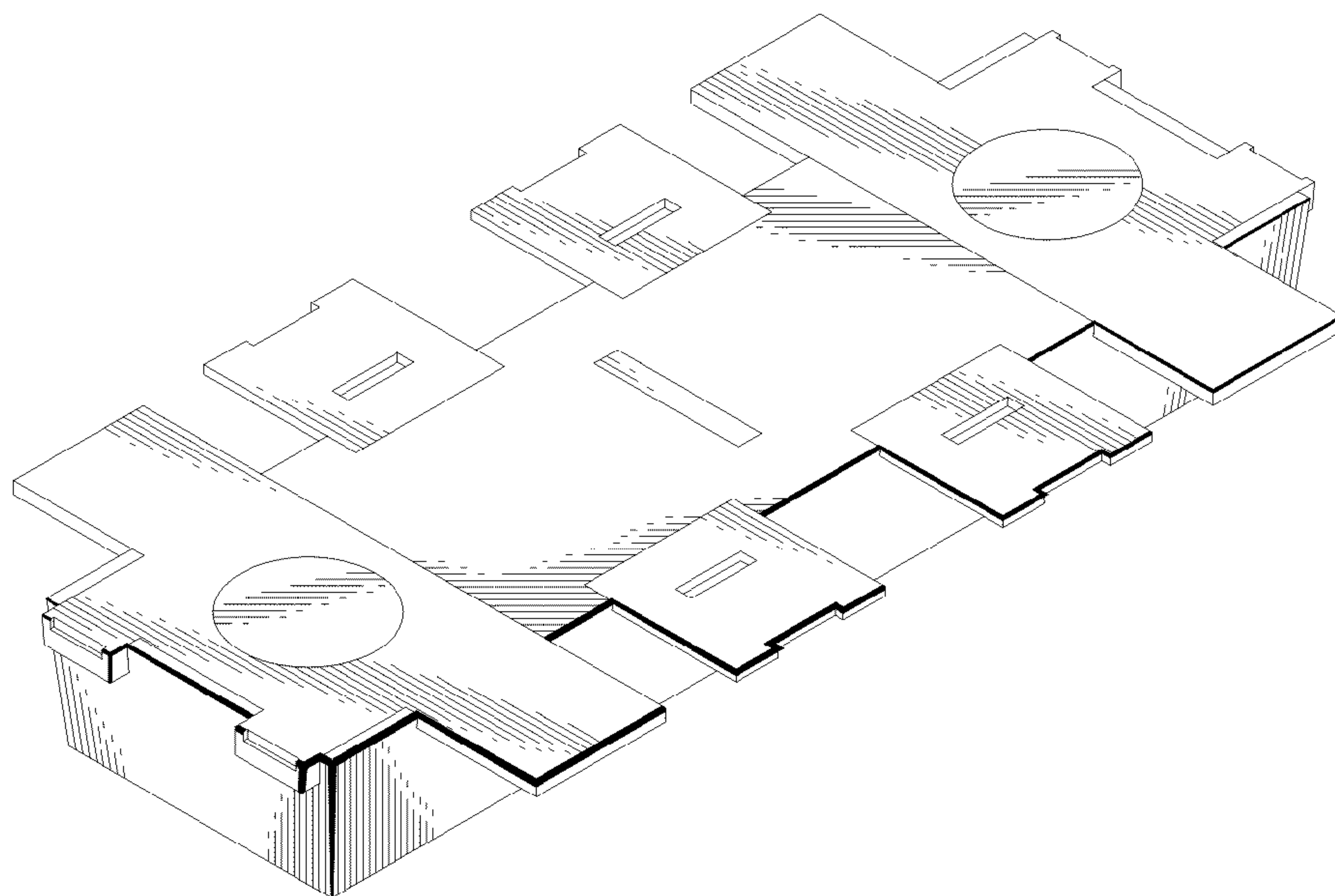


FIG.8

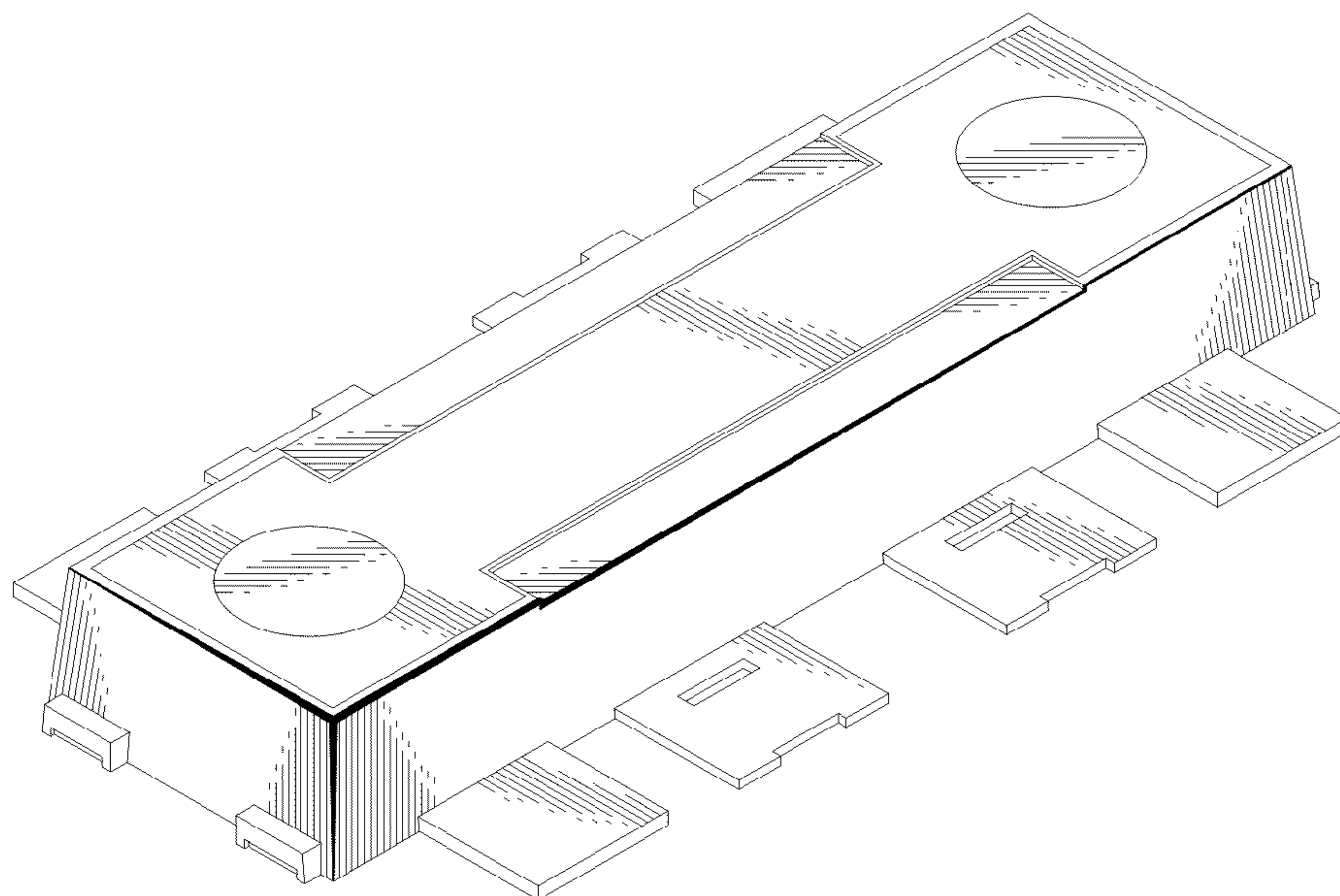


FIG.9

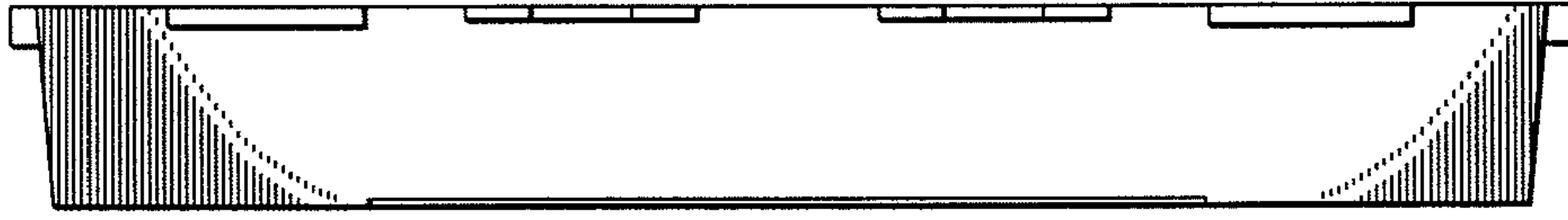


FIG.10

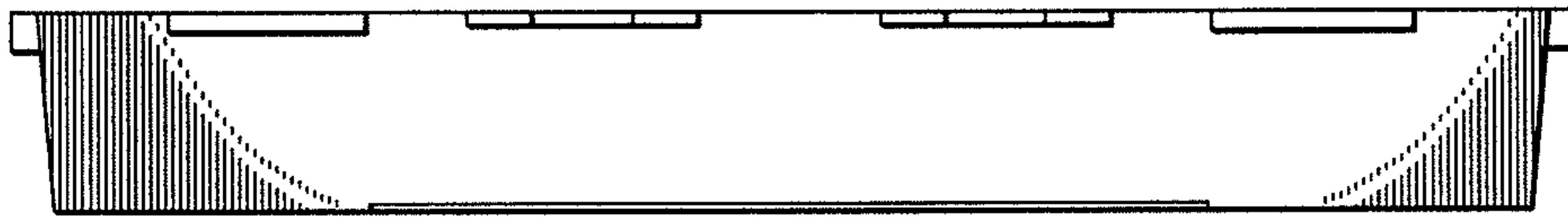


FIG.11

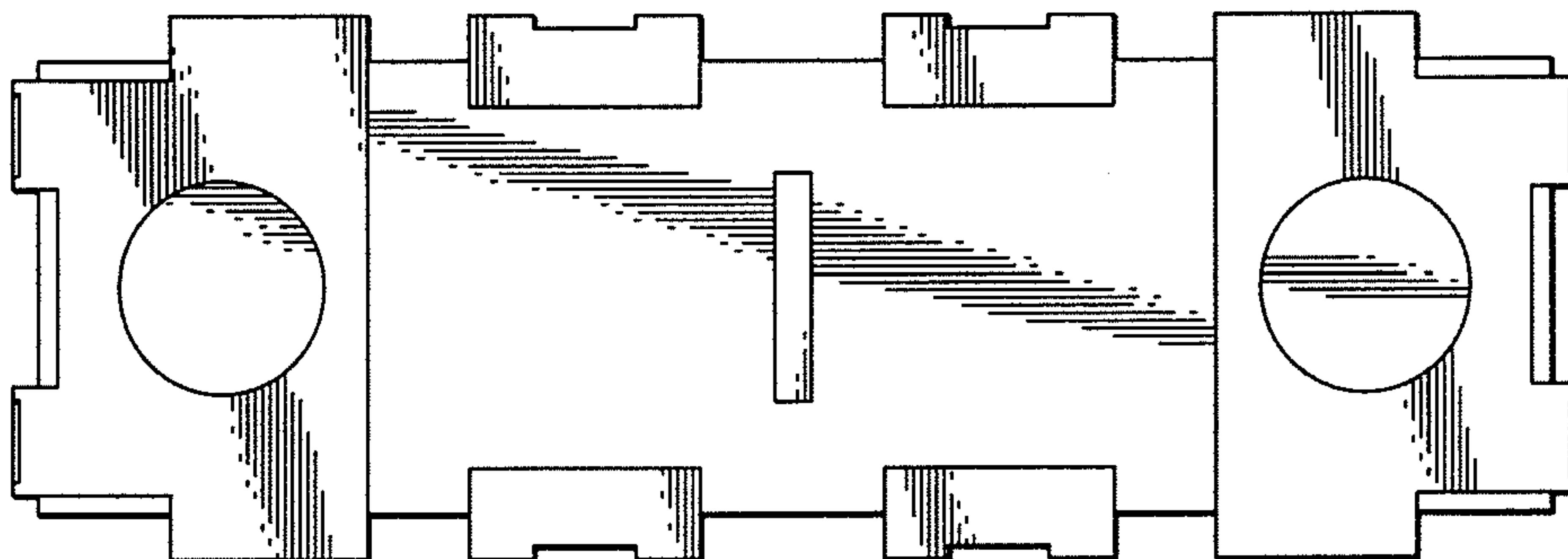


FIG.12

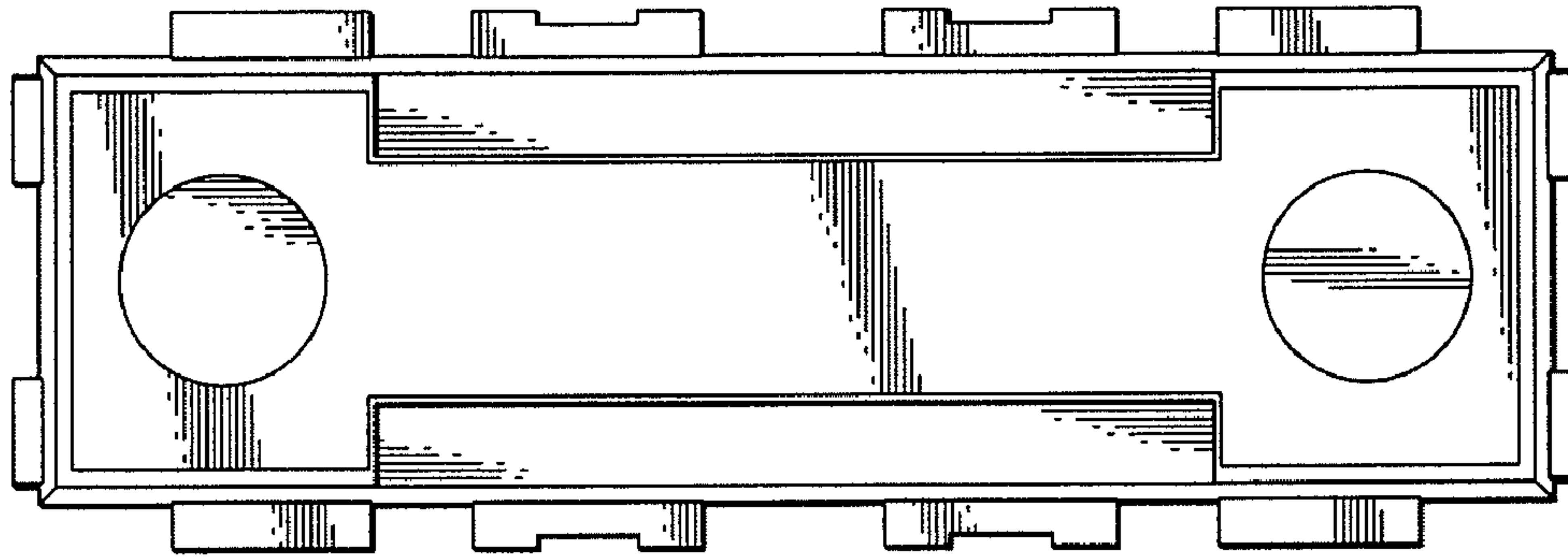


FIG.13

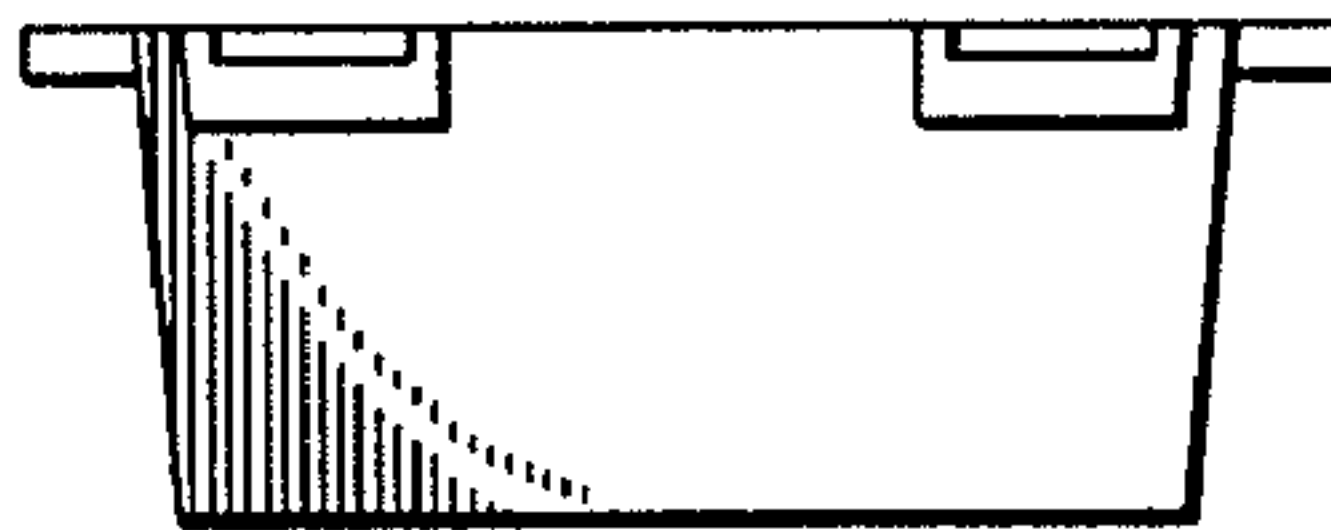


FIG.14

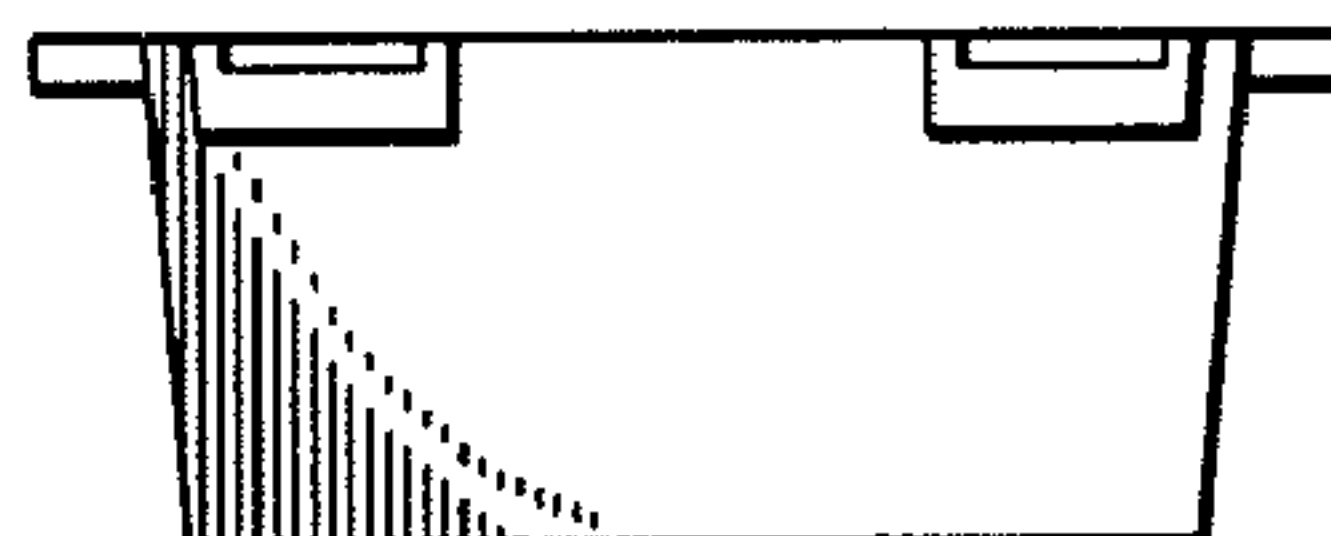


FIG.15

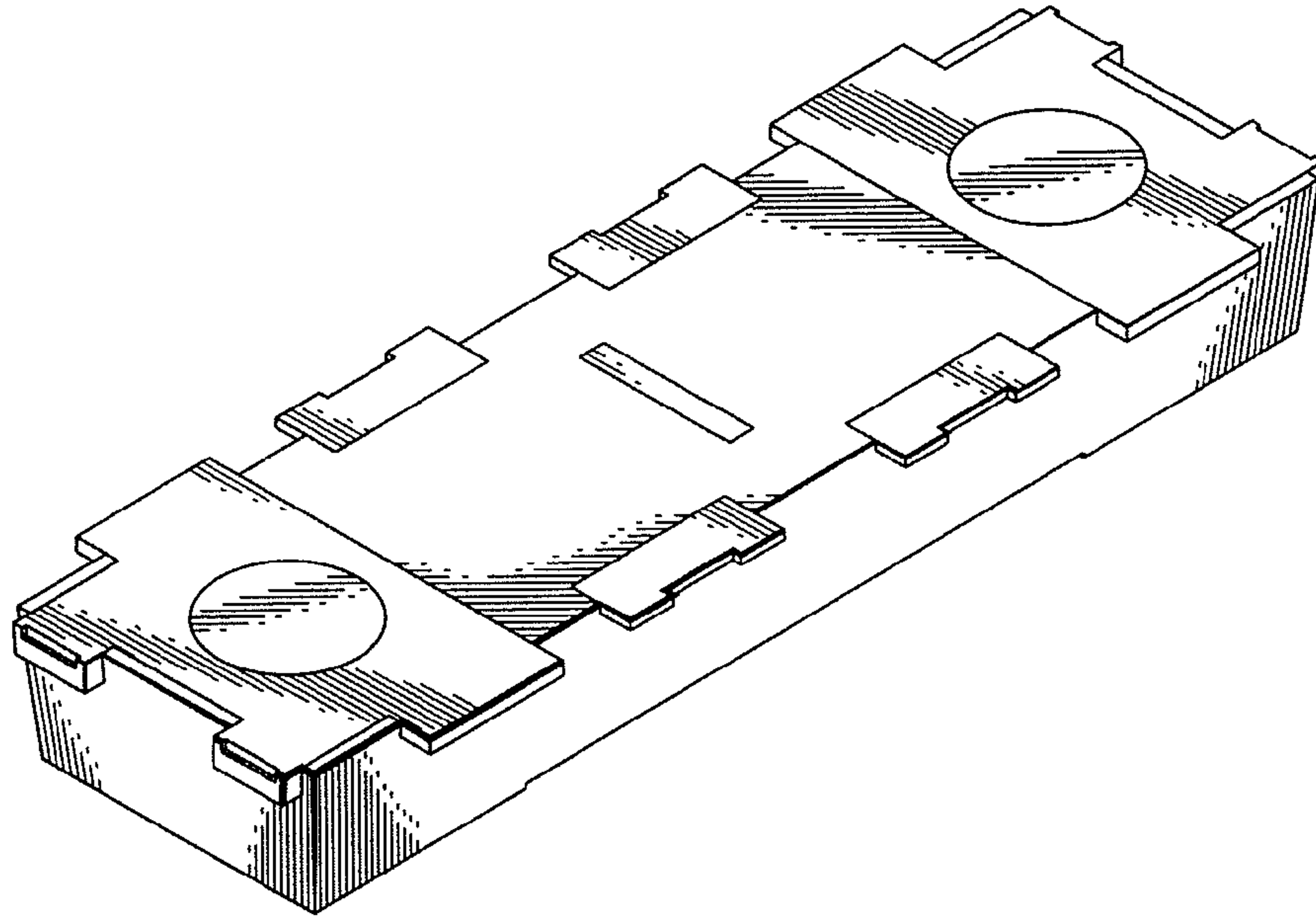


FIG.16

