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Lim et al.

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(54) **JUNCTION PHOTOVOLTAGE PROBE FACE**

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(73) Assignee: **Abhee 1, L.P.**, Los Altos, CA (US)

(**) Term: **14 Years**

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(51) **LOC (9) Cl.** **10-04**
(52) **U.S. Cl.** **D10/78**
(58) **Field of Classification Search** D10/78, D10/46, 75; 324/754.09, 762.01, 754.23, 324/762.05, 71.5; 356/237.2, 237.6, 432, 356/445, 418, 237.1; 257/E21.53
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

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D600,577 S	*	9/2009	Lloyd et al.	D10/75

* cited by examiner

Primary Examiner — Antoine D Davis

(57) CLAIM

The ornamental design for a junction photovoltage probe face, as shown and described.

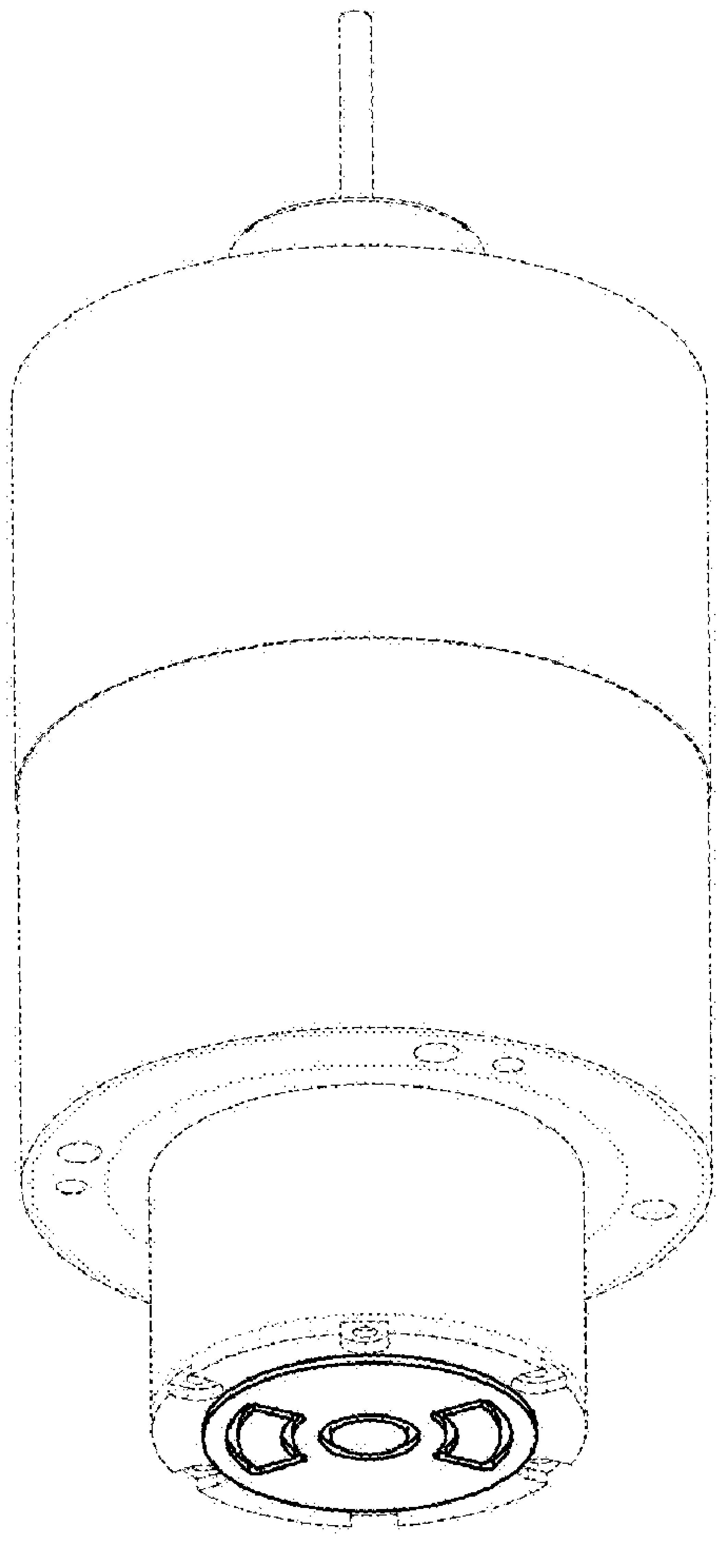
DESCRIPTION

FIG. **1** is a perspective view of the probe showing our design;
FIG. **2** is a rear side view of thereof;
FIG. **3** is a top plan view thereof;
FIG. **4** is a left side view thereof;
FIG. **5** is a front side view thereof;
FIG. **6** is right side view thereof; and,
FIG. **7** is a bottom plan view thereof.

The broken lines shown of the junction photovoltage probe face in the above FIGS. **1-7** are included for the purpose of illustrating environmental structure and form no part of the claimed design.

The present design relates to an ornamental object that can be used as an input device for obtaining accurate junction photovoltage measurements of semiconductor wafers for semiconductor wafer testing equipment.

1 Claim, 7 Drawing Sheets



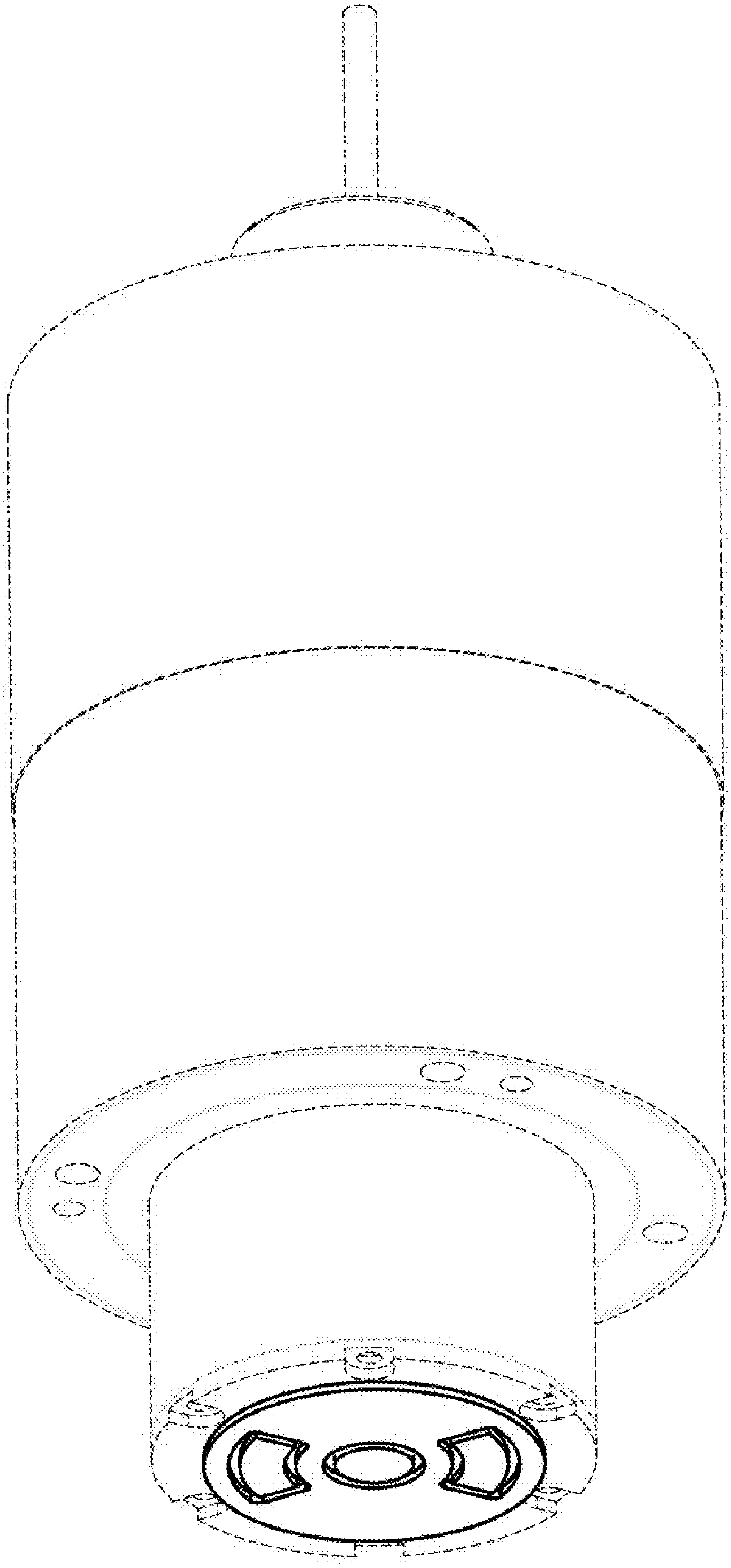


FIG. 1

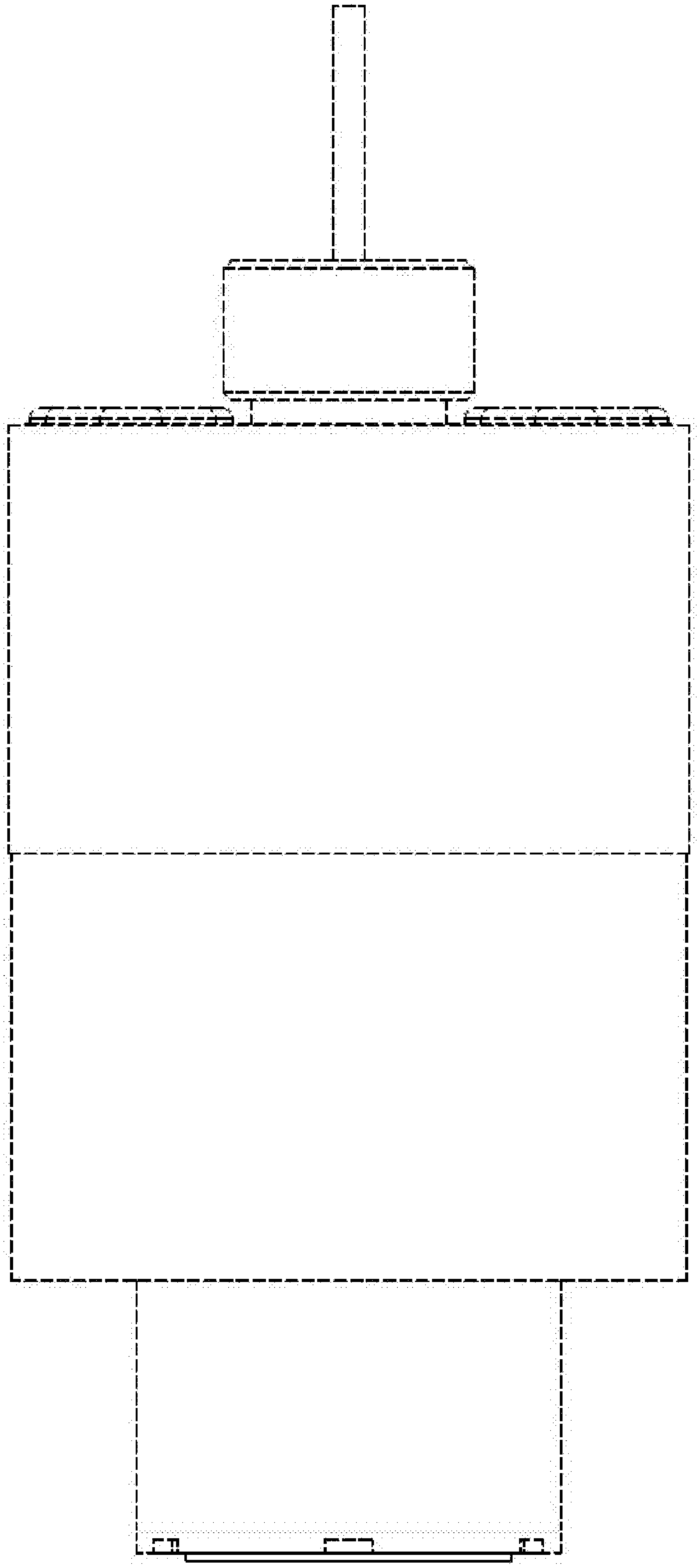


FIG. 2

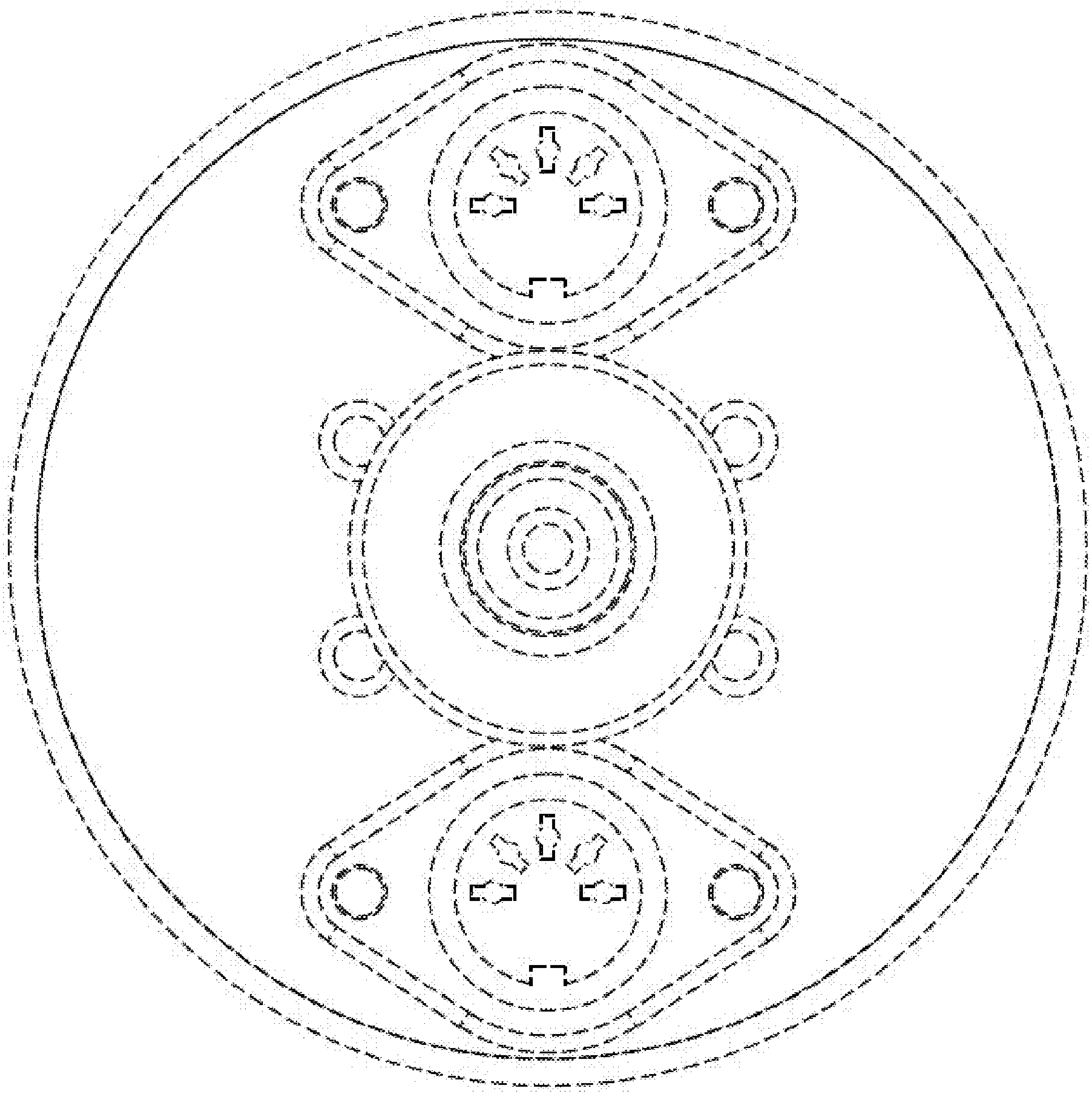


FIG. 3

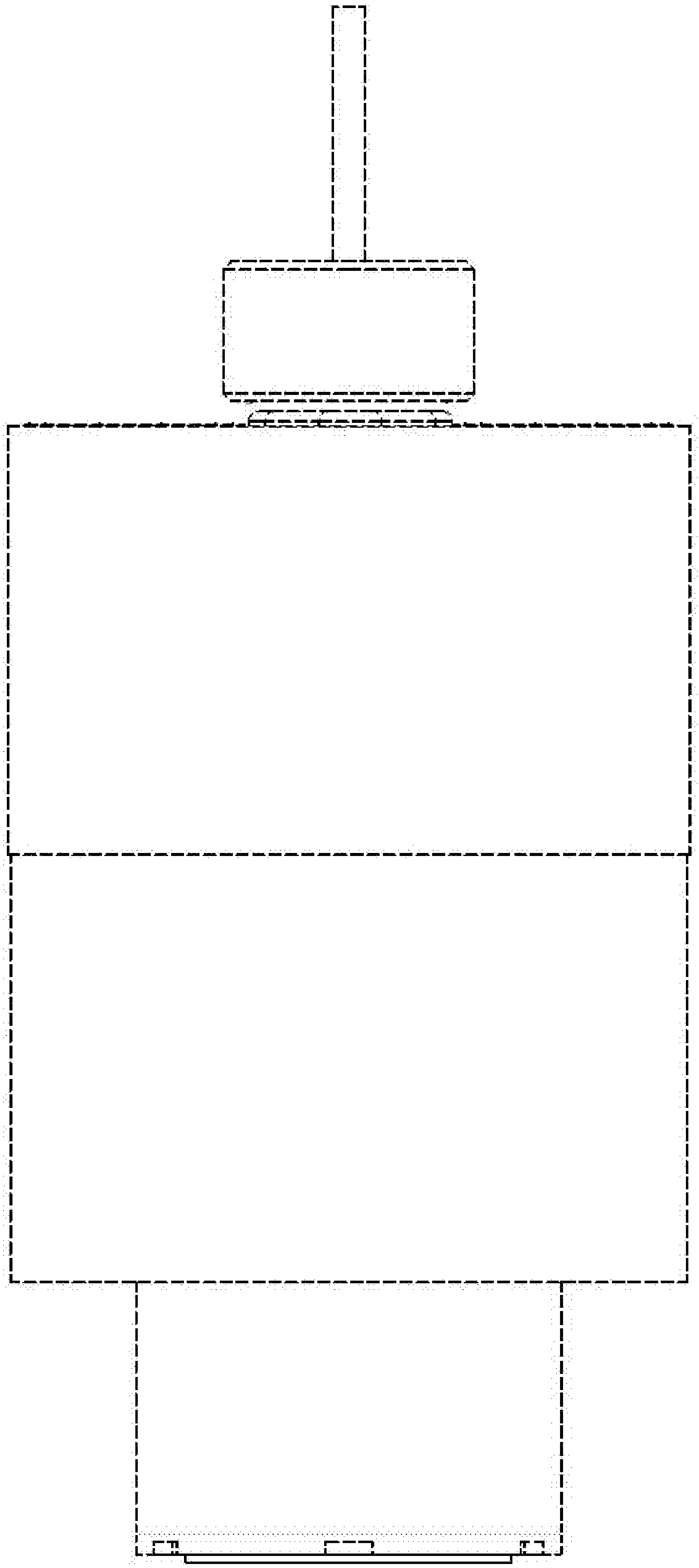


FIG. 4

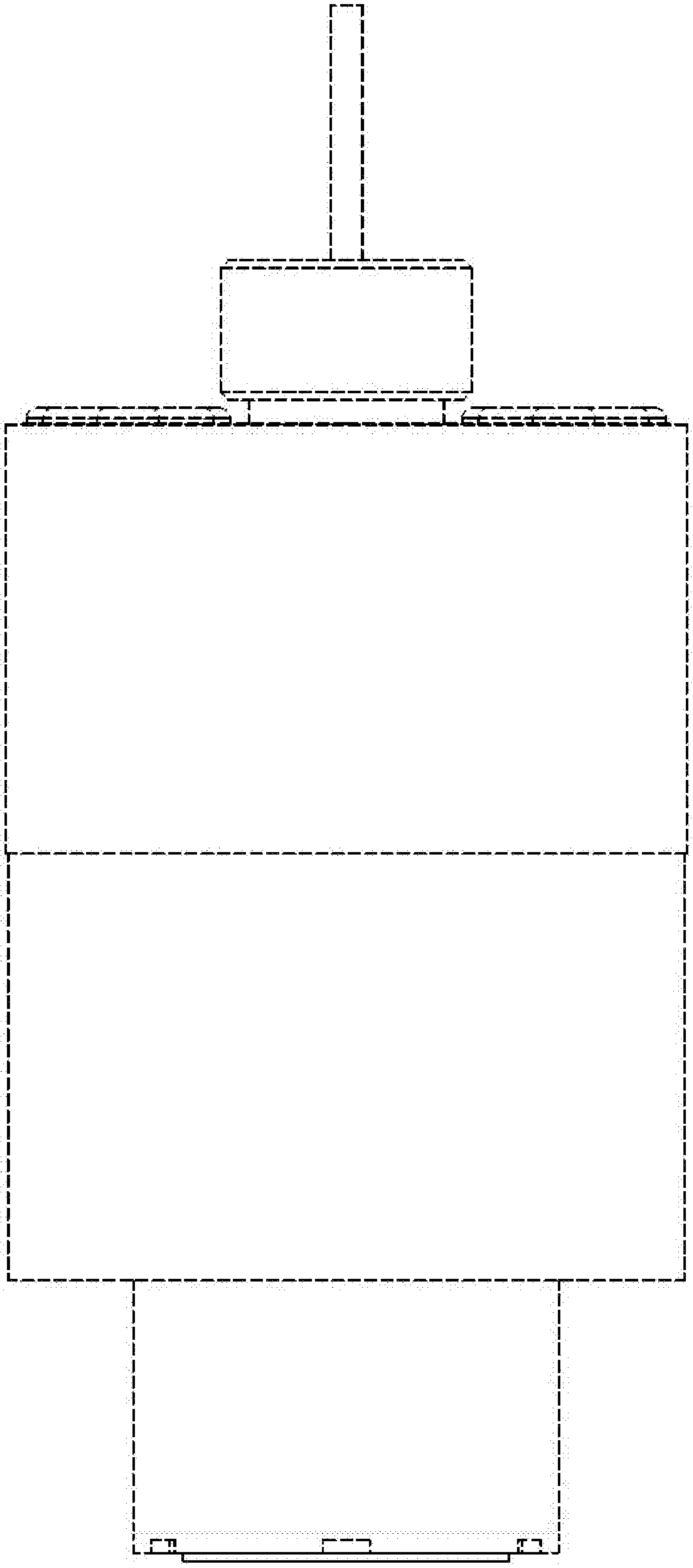


FIG. 5

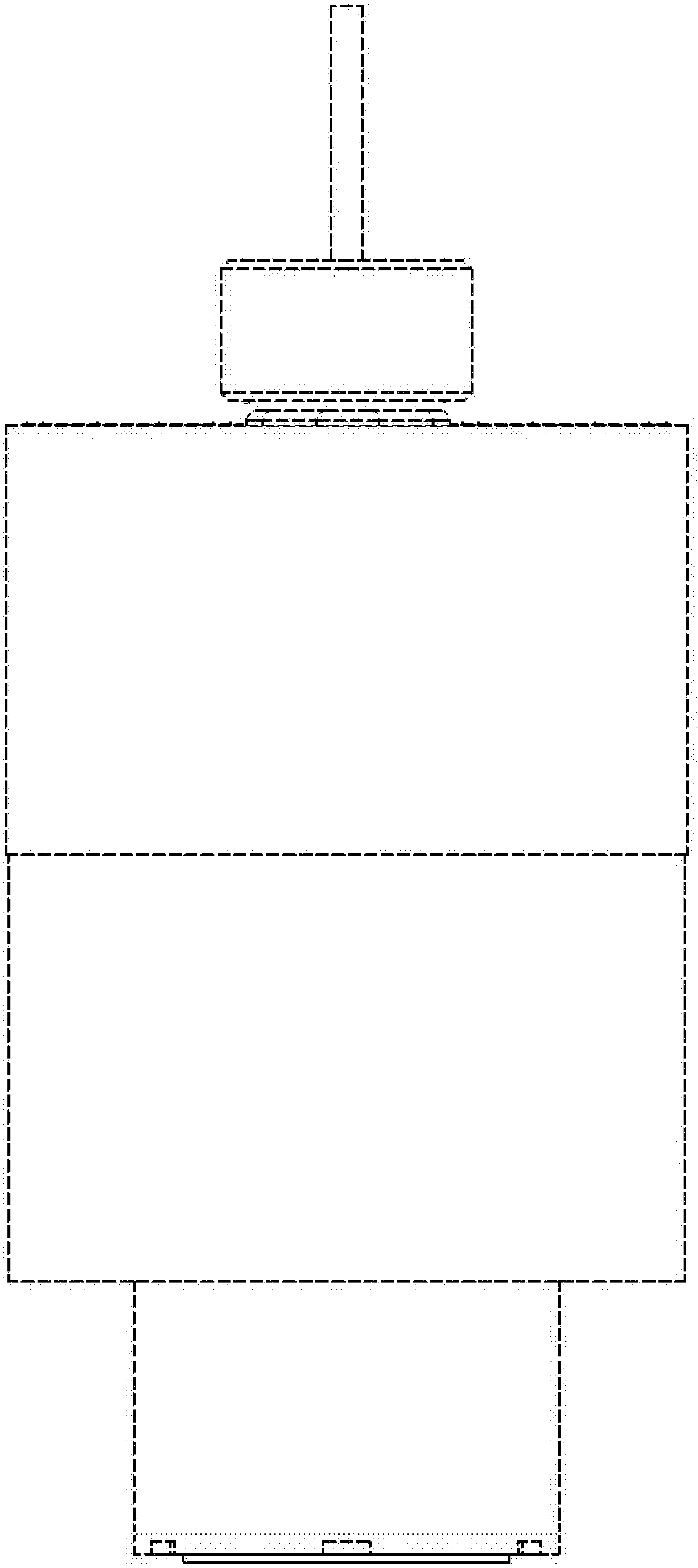


FIG. 6

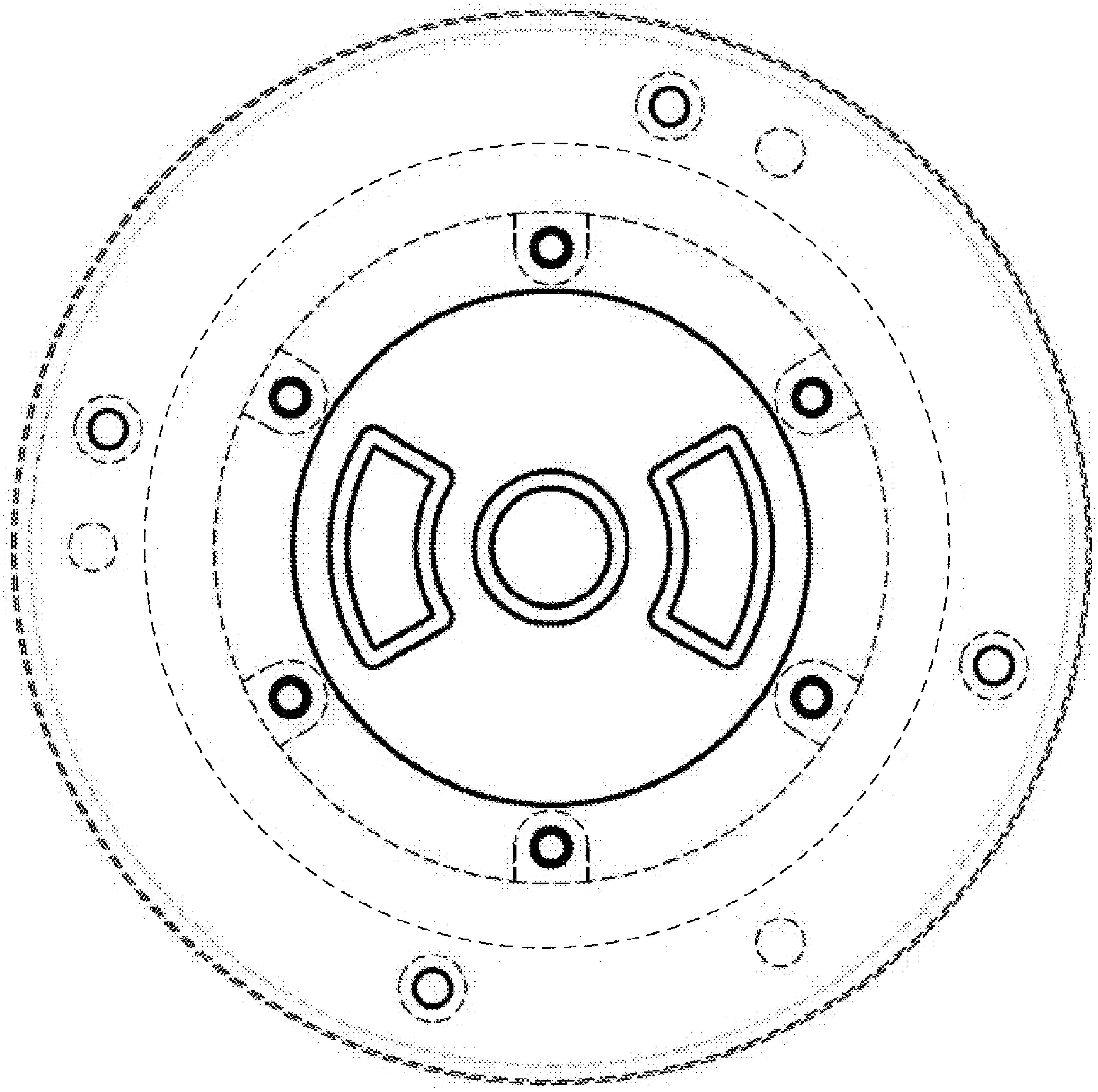


FIG. 7