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(12) **United States Design Patent**
Oonuma et al.

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(45) **Date of Patent:** **** May 3, 2011**

(54) **SEMICONDUCTOR TESTING MACHINE**

(56) **References Cited**

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(**) Term: **14 Years**

(21) Appl. No.: **29/360,394**

(57) **CLAIM**

The ornamental design for a semiconductor testing machine, as shown.

(22) Filed: **Apr. 26, 2010**

(30) **Foreign Application Priority Data**

DESCRIPTION

Oct. 30, 2009 (JP) 2009-025480

(51) **LOC (9) Cl.** **10-04**

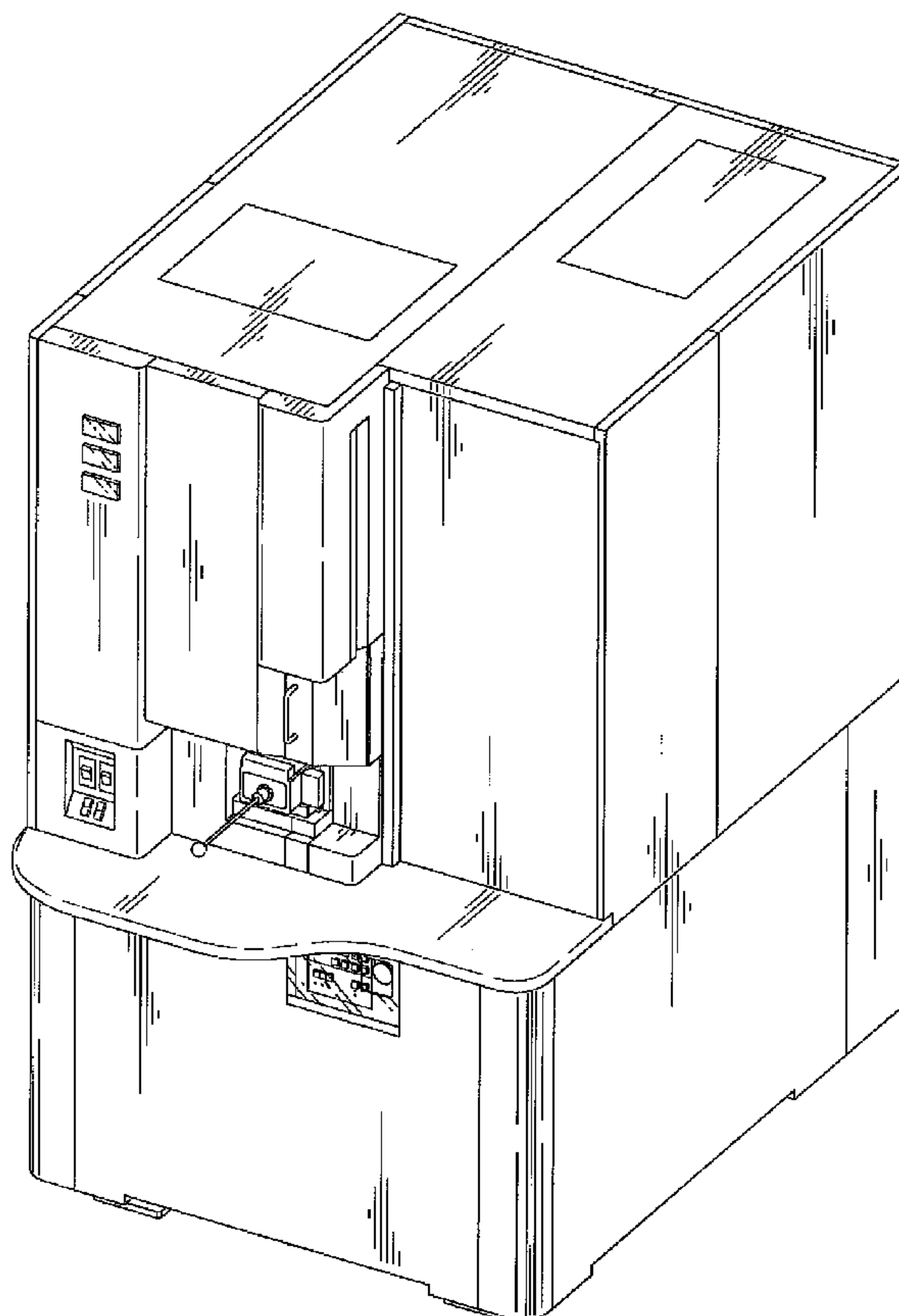
(52) **U.S. Cl.** **D10/75**

(58) **Field of Classification Search** D10/75;
324/72.5, 750.03, 750.07, 750.08, 750.25,
324/756.02, 756.04, 762.01, 762.04, 762.05;
365/201; 439/70, 259, 260, 265; 702/120;
714/E11.001, E11.155, 719, 721, 724, 738

FIG. 1 is a front, top and right side perspective view of a semiconductor testing machine showing our new design; FIG. 2 is a front elevational view thereof; FIG. 3 is a rear elevational view thereof; FIG. 4 is a top plan view thereof; FIG. 5 is a bottom plan view thereof; FIG. 6 is a right side elevational view thereof; and, FIG. 7 is a left side elevational view thereof.

See application file for complete search history.

1 Claim, 7 Drawing Sheets



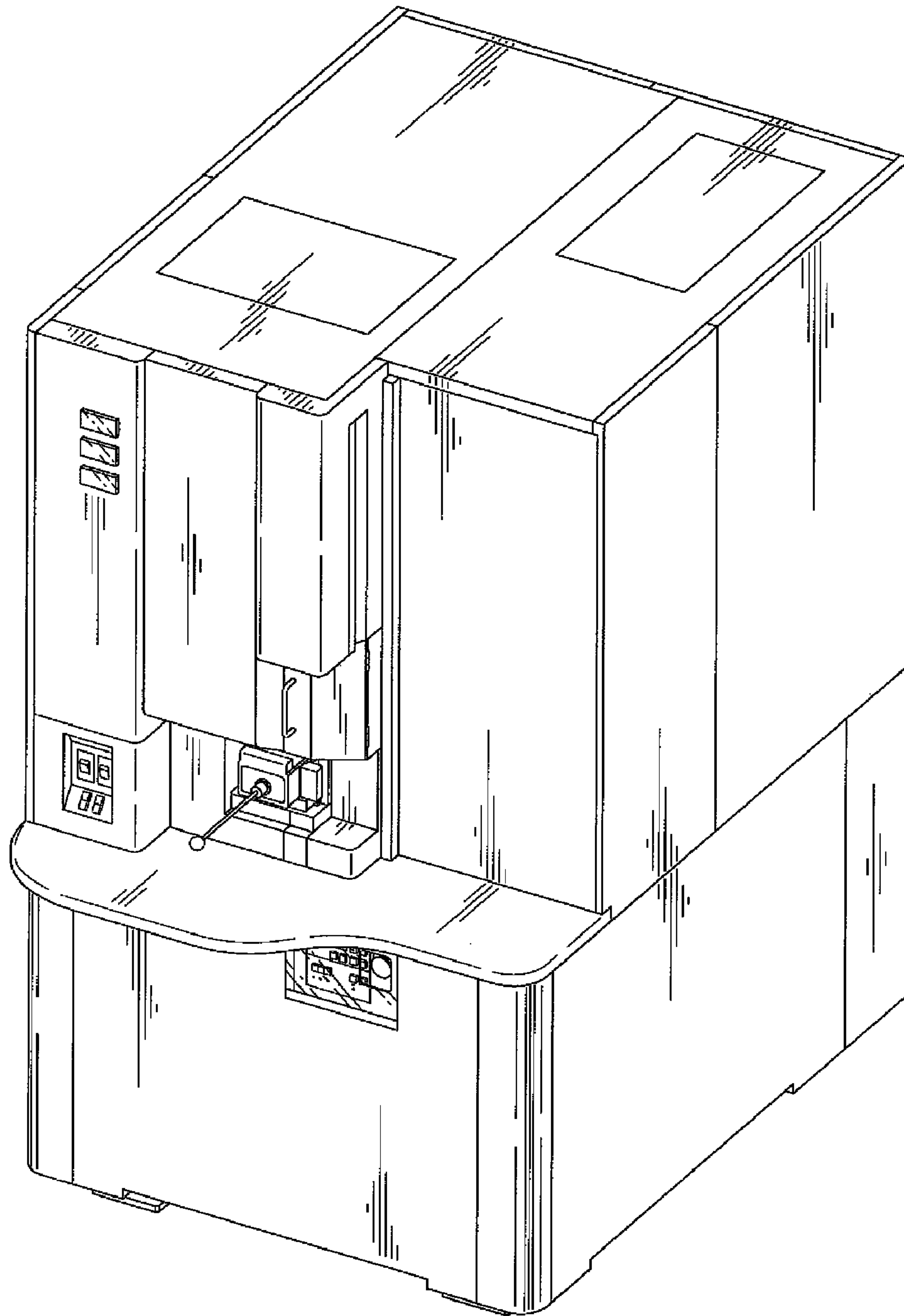


FIG. 1

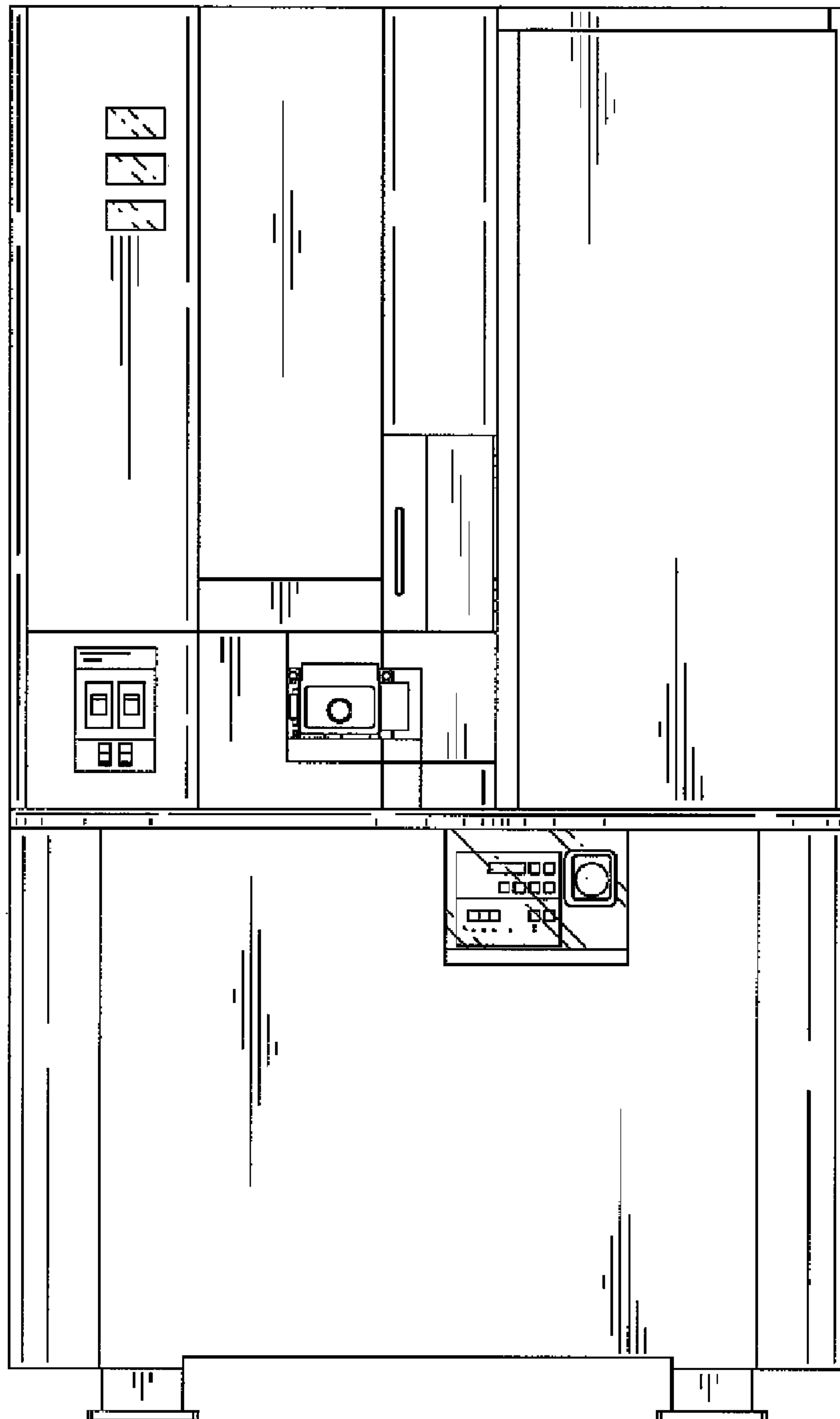


FIG. 2

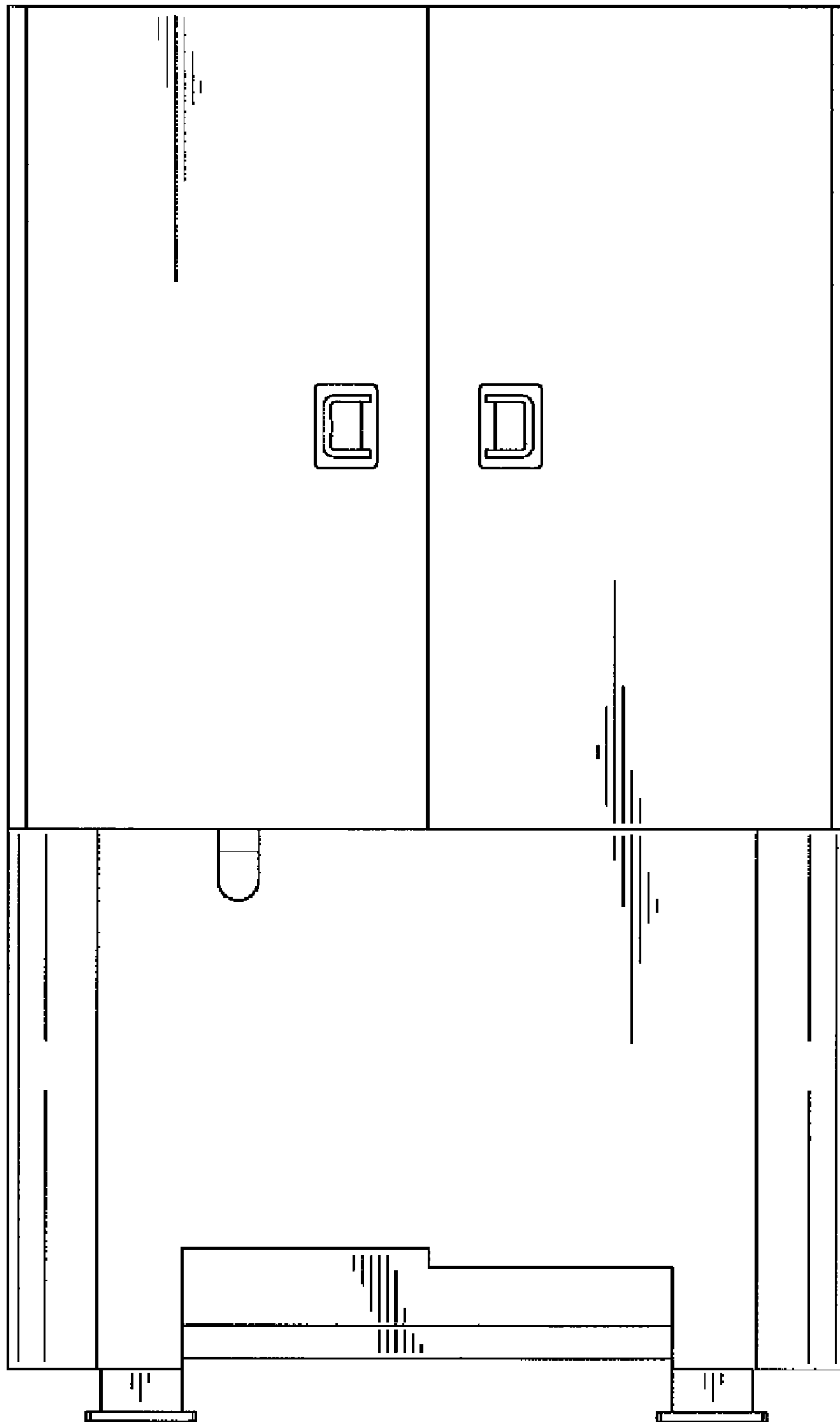


FIG. 3

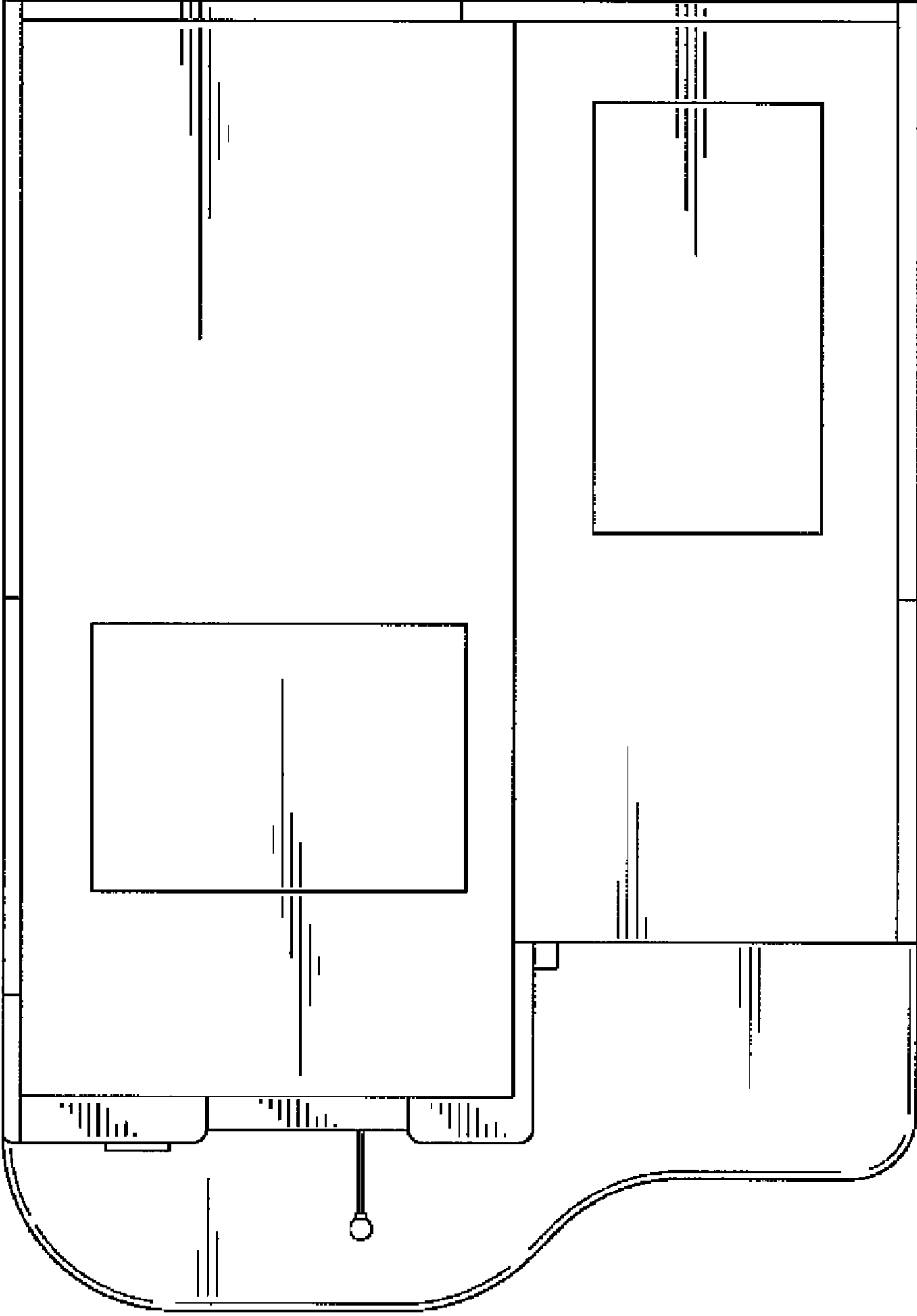


FIG. 4

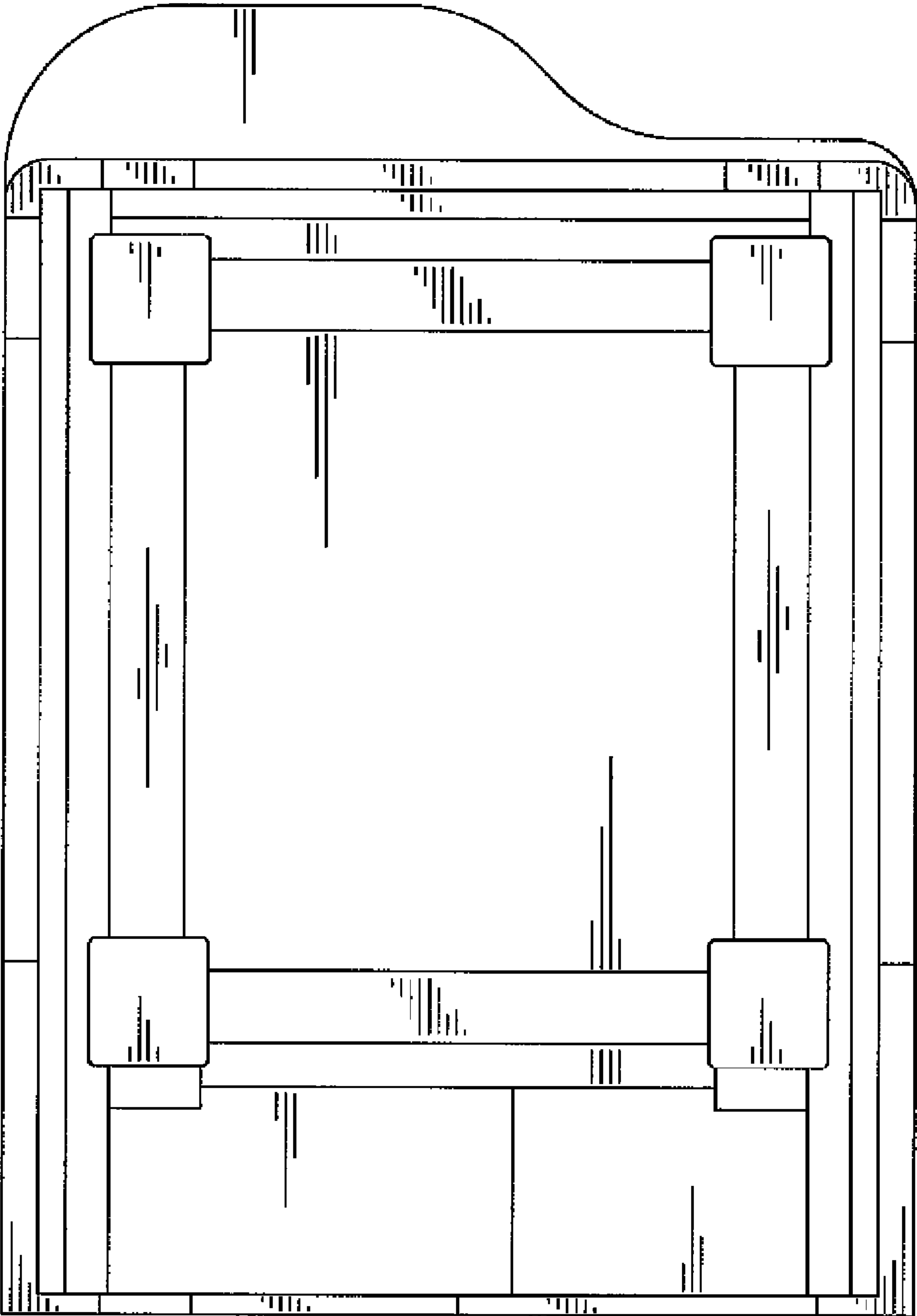


FIG. 5

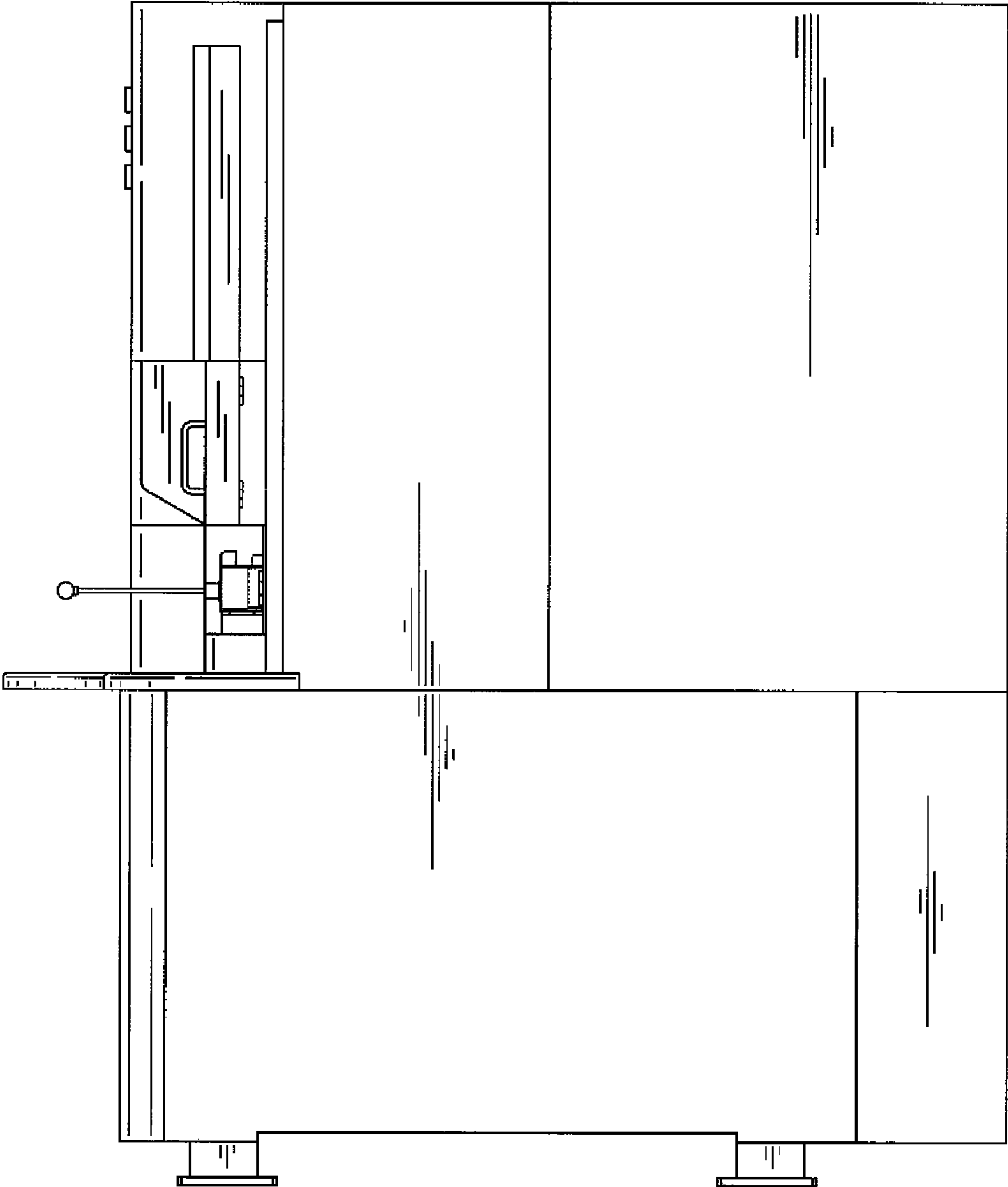


FIG. 6

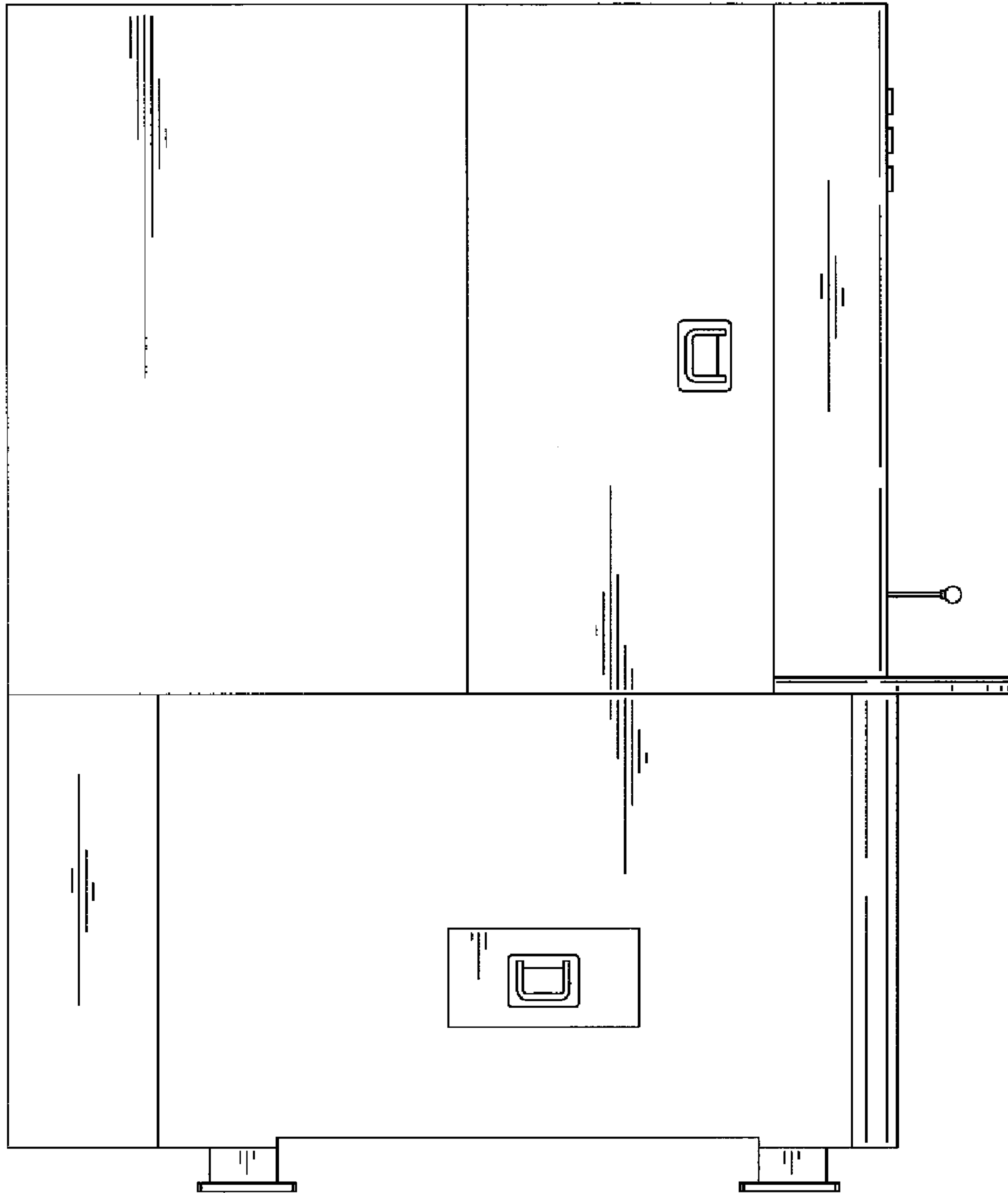


FIG. 7