US00D621803S

(12) United States Design Patent

Maruyama et al.

(10) Patent No.: US D621,803 S
(45) Date of Patent: ** Aug. 17, 2010

(54) **SEMICONDUCTOR WAFER PROCESSING TAPE**

(75) Inventors: **Hiromitsu Maruyama**, Tokyo (JP); **Shuzo Taguchi**, Tokyo (JP); **Yasumasa Morishima**, Tokyo (JP); **Shinichi Ishiwata**, Tokyo (JP)

(73) Assignee: **The Furukawa Electric Co., Ltd.**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/321,418**

(22) Filed: **Jul. 16, 2008**

(51) **LOC (9) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Classification Search** ..... D13/182; 156/235, 248; 428/343, 345, 353, 355 R; 438/114, 455, 460, 463
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,864,295	B2 *	3/2005	Mitarai	521/50.5
D589,473	S *	3/2009	Takamoto et al.	D13/182
D598,380	S *	8/2009	Kuriki	D13/133
2007/0241436	A1 *	10/2007	Ookubo et al.	257/678
2010/0080989	A1 *	4/2010	Asai et al.	428/345

FOREIGN PATENT DOCUMENTS

JP	D1267623	S	4/2006
JP	2007-2173	A	1/2007
JP	D1315406	S	11/2007
JP	D1315621	S	11/2007

* cited by examiner

Primary Examiner—Selina Sikder
(74) *Attorney, Agent, or Firm*—Knoble Yoshida & Dunleavy, LLC

(57) **CLAIM**

The ornamental design for a "semiconductor wafer processing tape," as shown and described.

DESCRIPTION

FIG. **1** is a perspective view showing our new design;

FIG. **2** is a top plan view;

FIG. **3** is a bottom plan view;

FIG. **4** is a left side view;

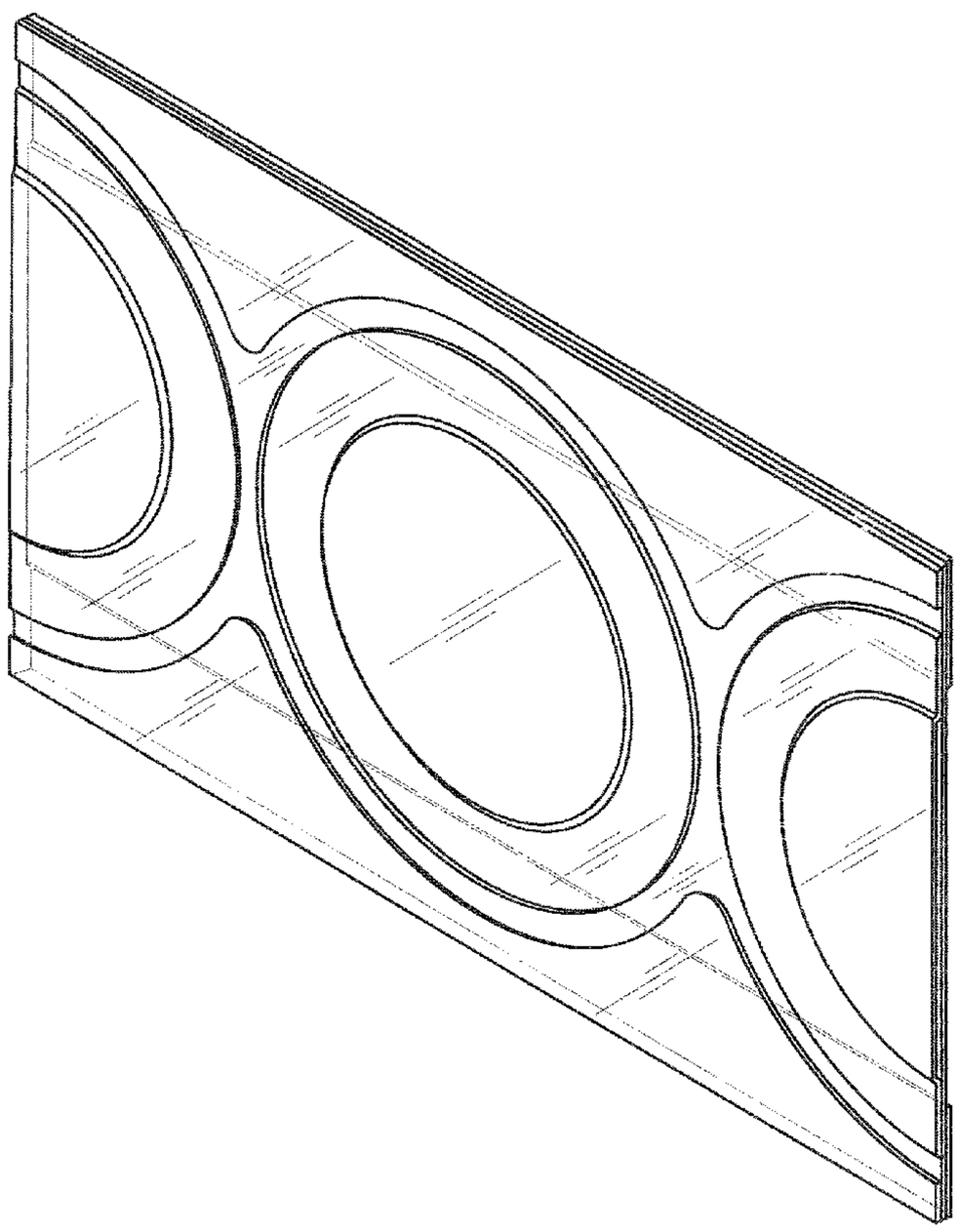
FIG. **5** is a front side view;

FIG. **6** is a right side view;

FIG. **7** is a cross sectional view at **7**—**7** of FIG. **1**; and,

FIG. **8** is a cross sectional view at **8**—**8** of FIG. **1**.

1 Claim, 5 Drawing Sheets



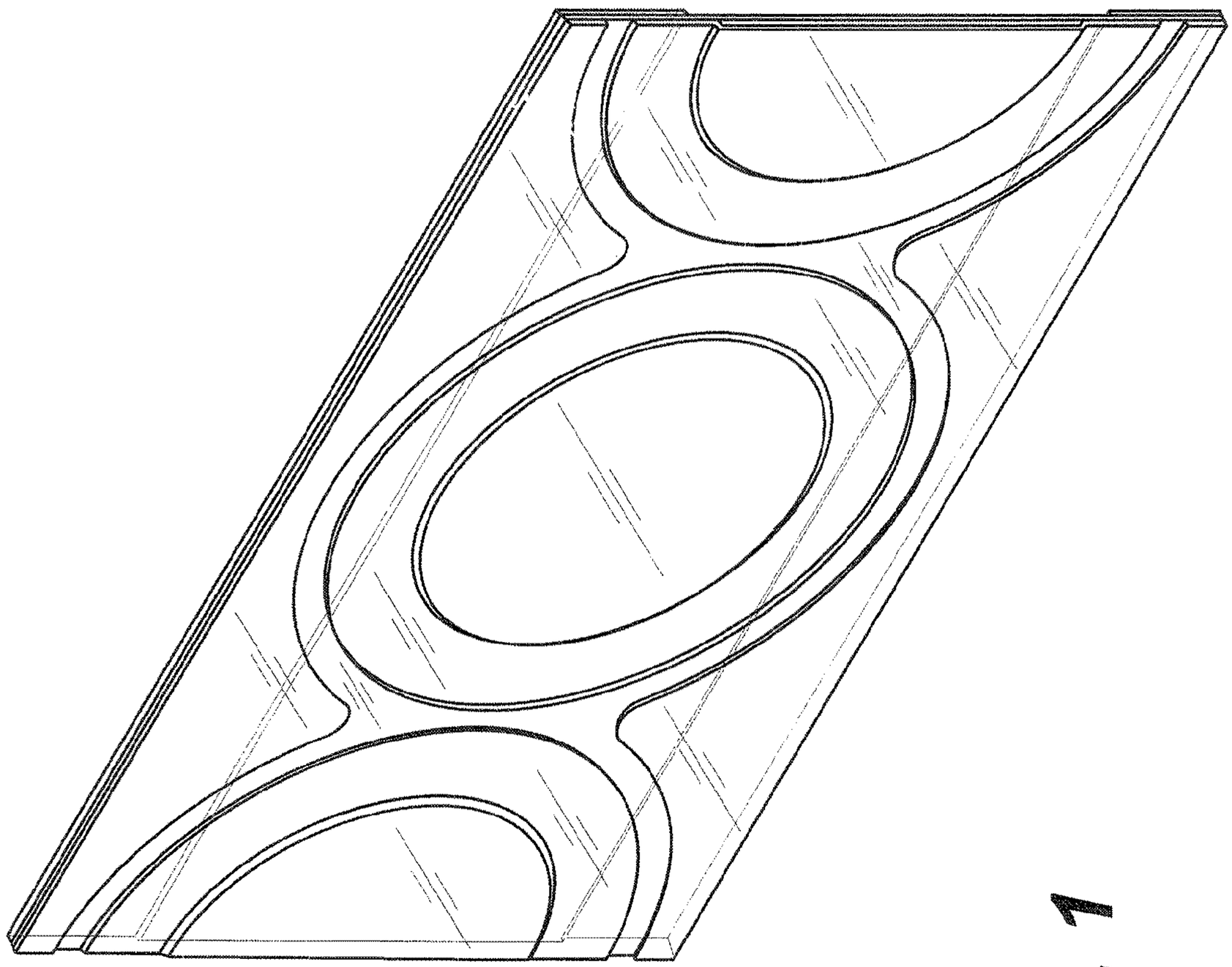


FIG. 1

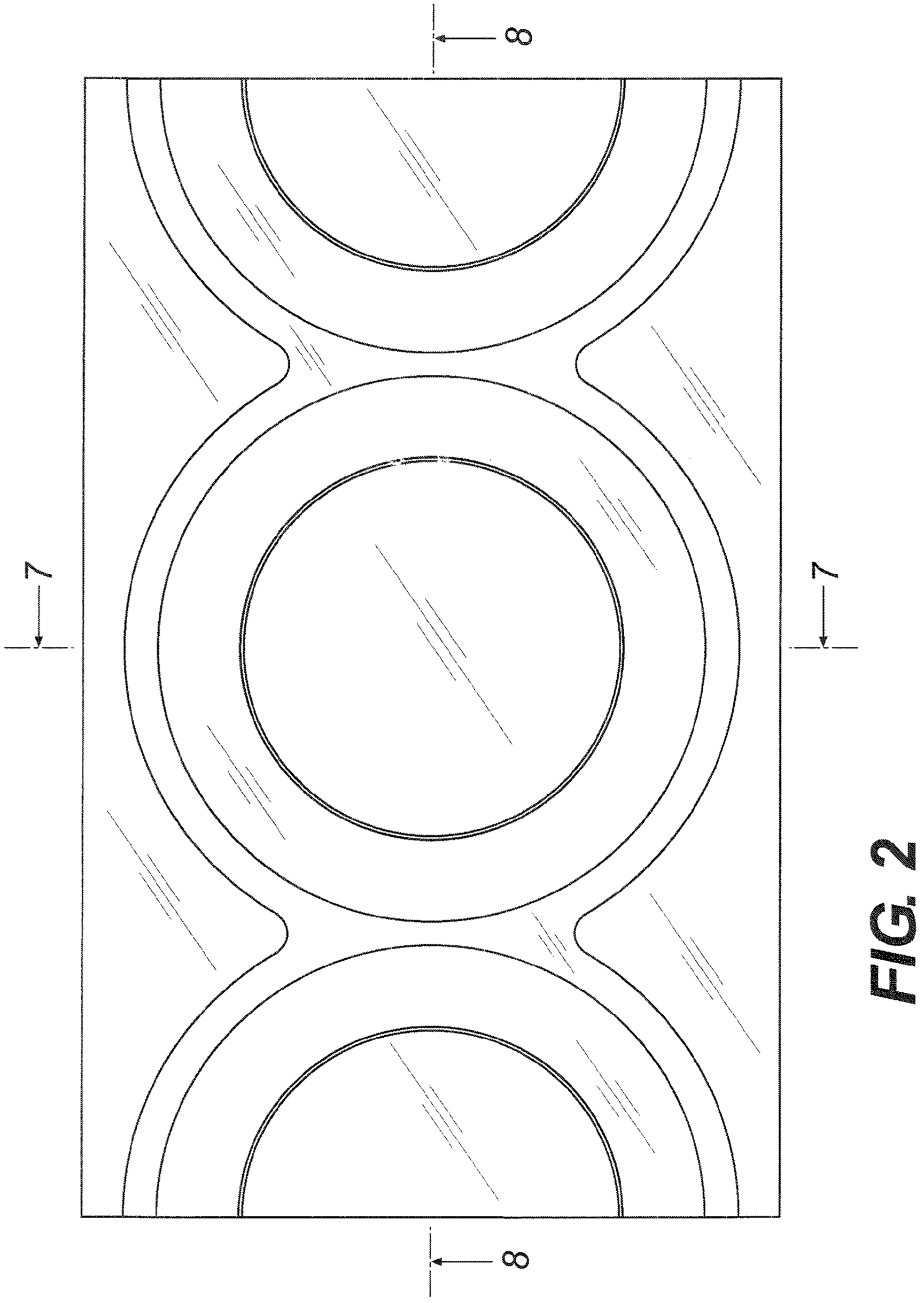


FIG. 2

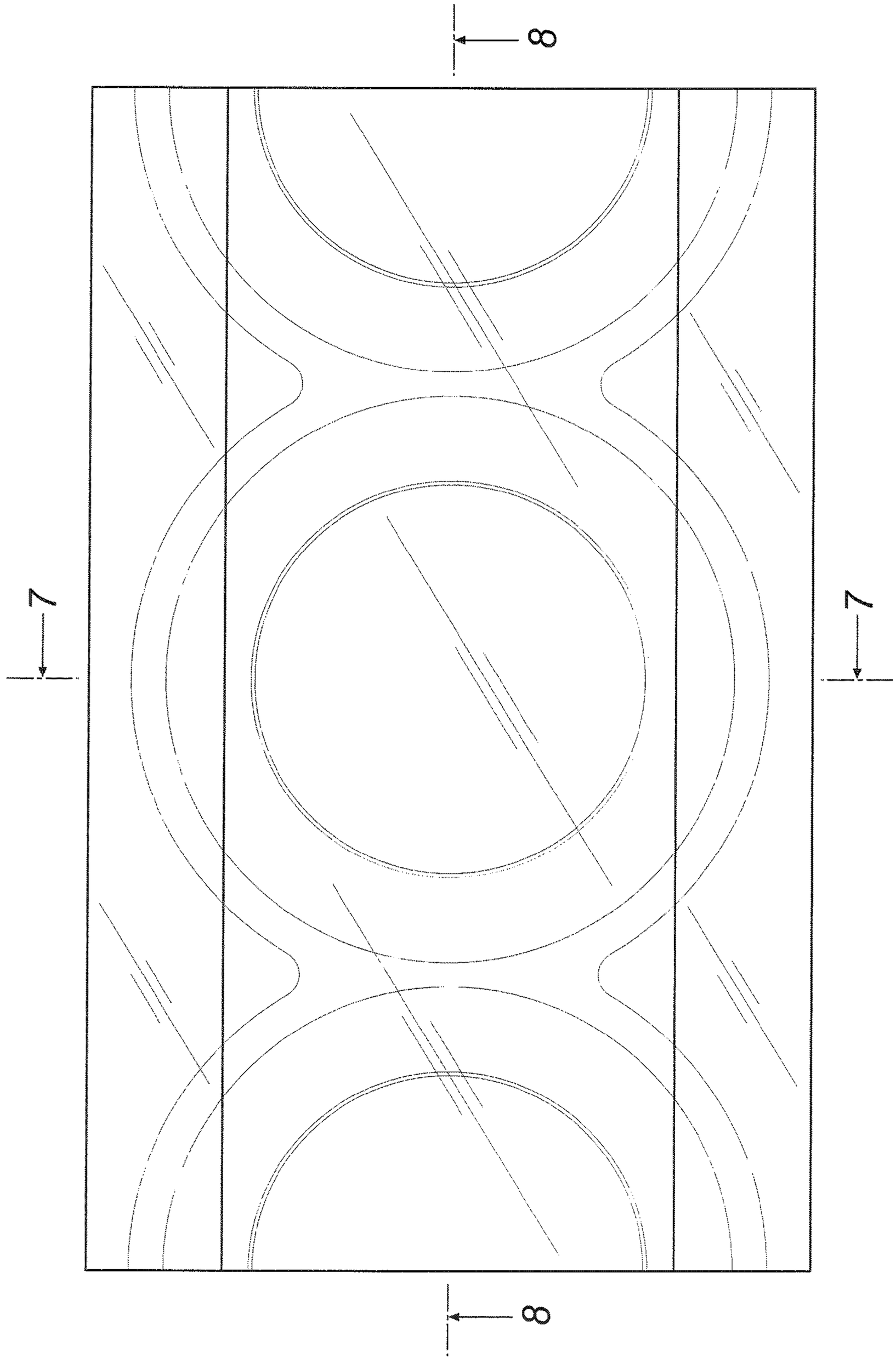


FIG. 3

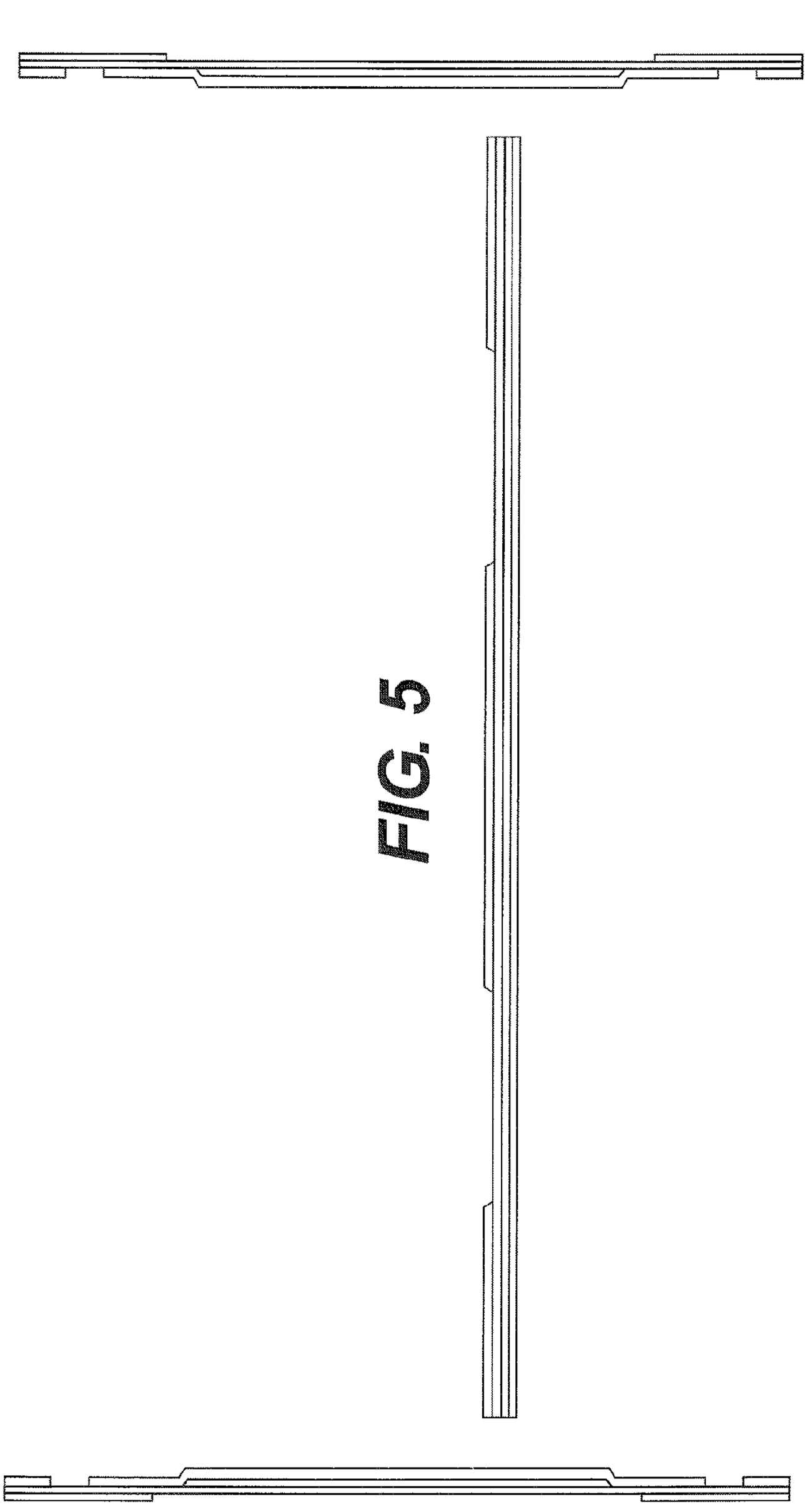


FIG. 6

FIG. 5

FIG. 4

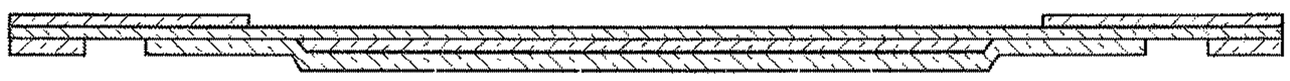


FIG. 7

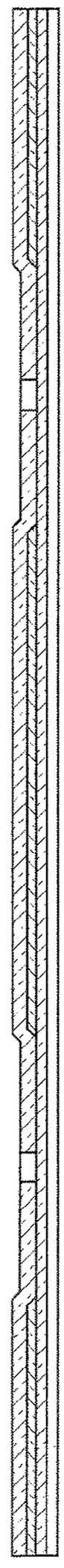


FIG. 8