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(12) **United States Design Patent**
Maruyama et al.

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(54) **SEMICONDUCTOR WAFER PROCESSING TAPE**

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FOREIGN PATENT DOCUMENTS

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(**) Term: **14 Years**

(21) Appl. No.: **29/321,418**

(57) **CLAIM**

(22) Filed: **Jul. 16, 2008**

The ornamental design for a “semiconductor wafer processing tape,” as shown and described.

(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
156/235, 248; 428/343, 345, 353, 355 R;
438/114, 455, 460, 463

See application file for complete search history.

DESCRIPTION

FIG. 1 is a perspective view showing our new design;

FIG. 2 is a top plan view;

FIG. 3 is a bottom plan view;

FIG. 4 is a left side view;

FIG. 5 is a front side view;

FIG. 6 is a right side view;

FIG. 7 is a cross sectional view at 7—7 of FIG. 1; and,

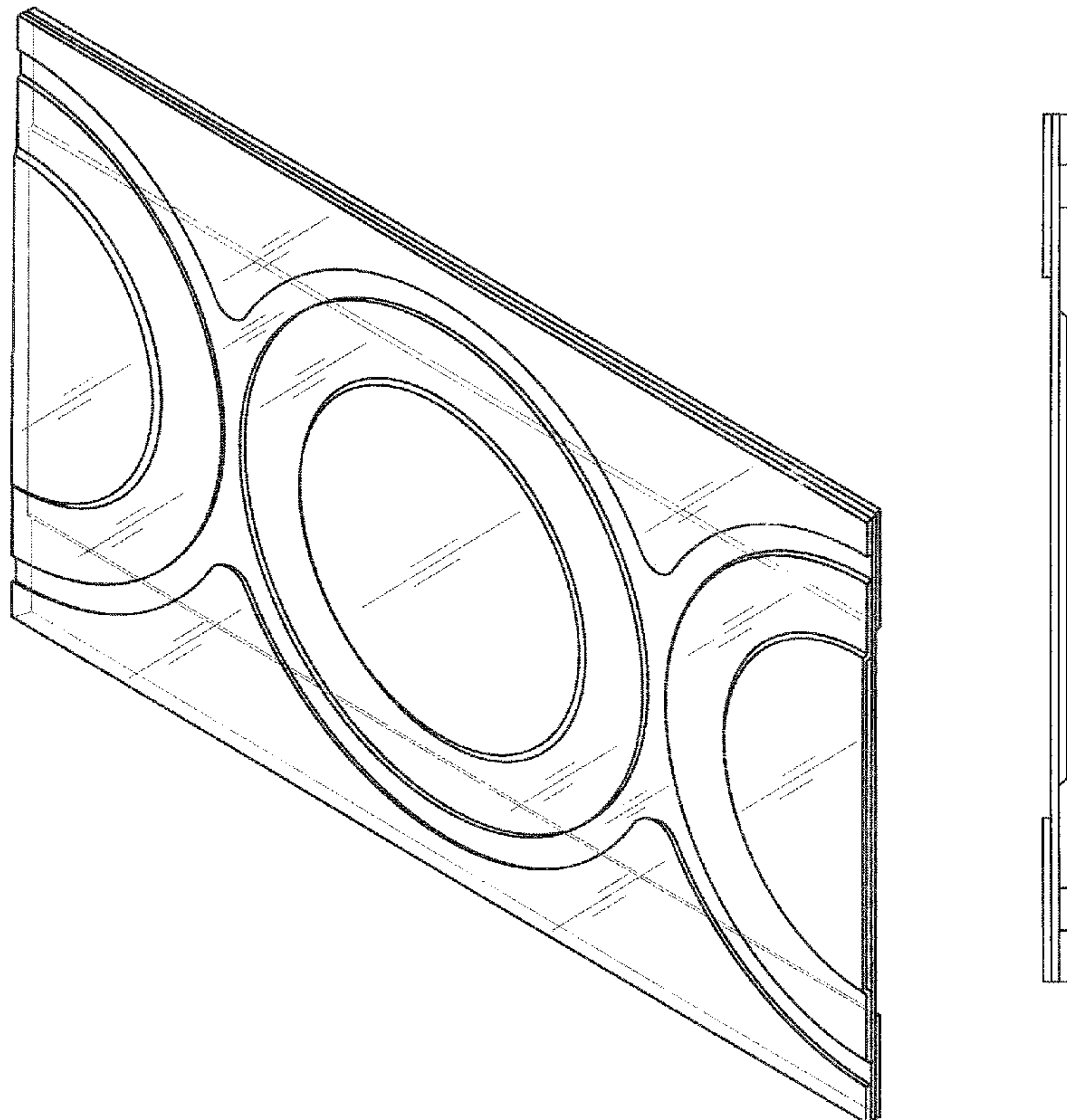
FIG. 8 is a cross sectional view at 8—8 of FIG. 1.

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1 Claim, 5 Drawing Sheets



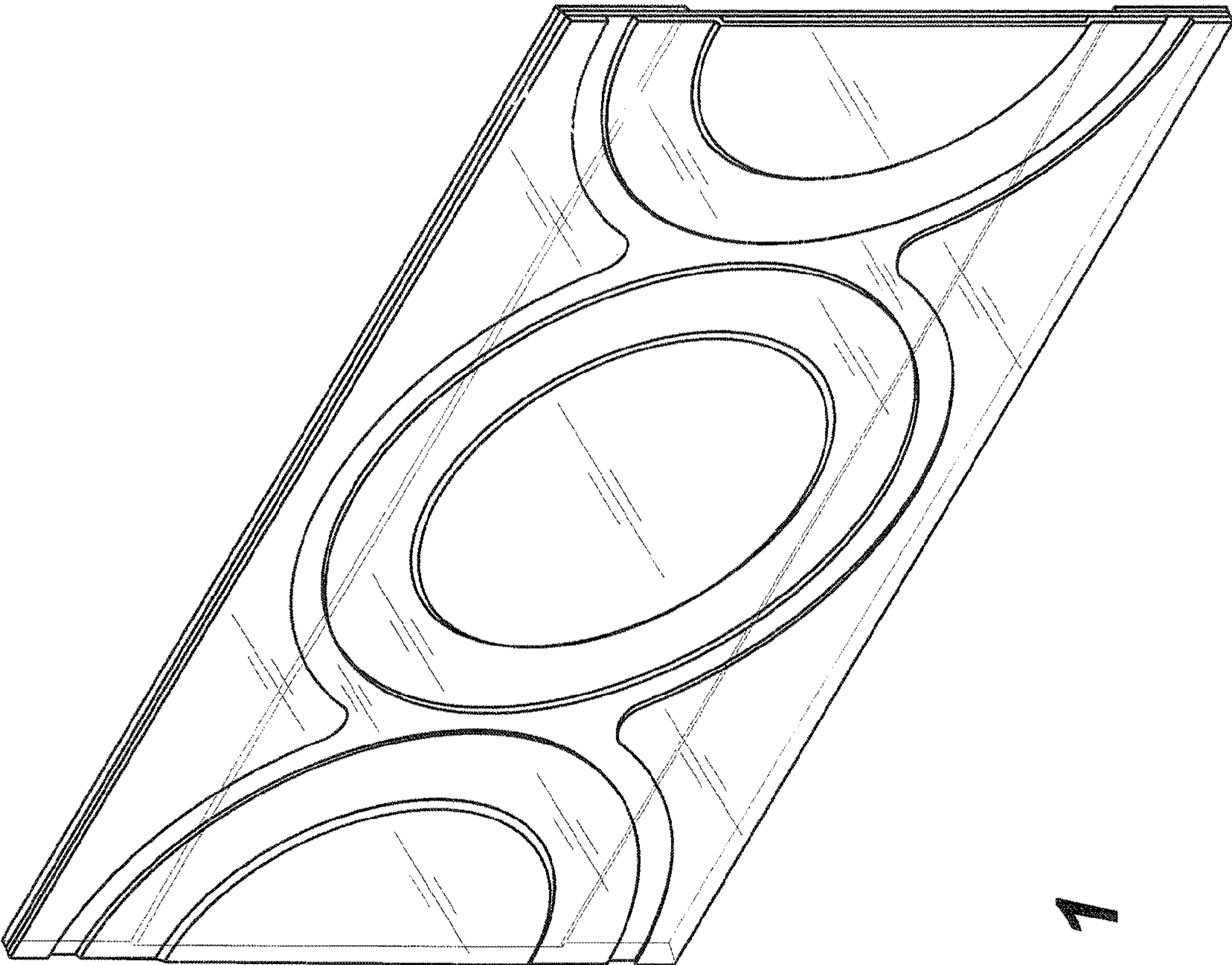


FIG. 1

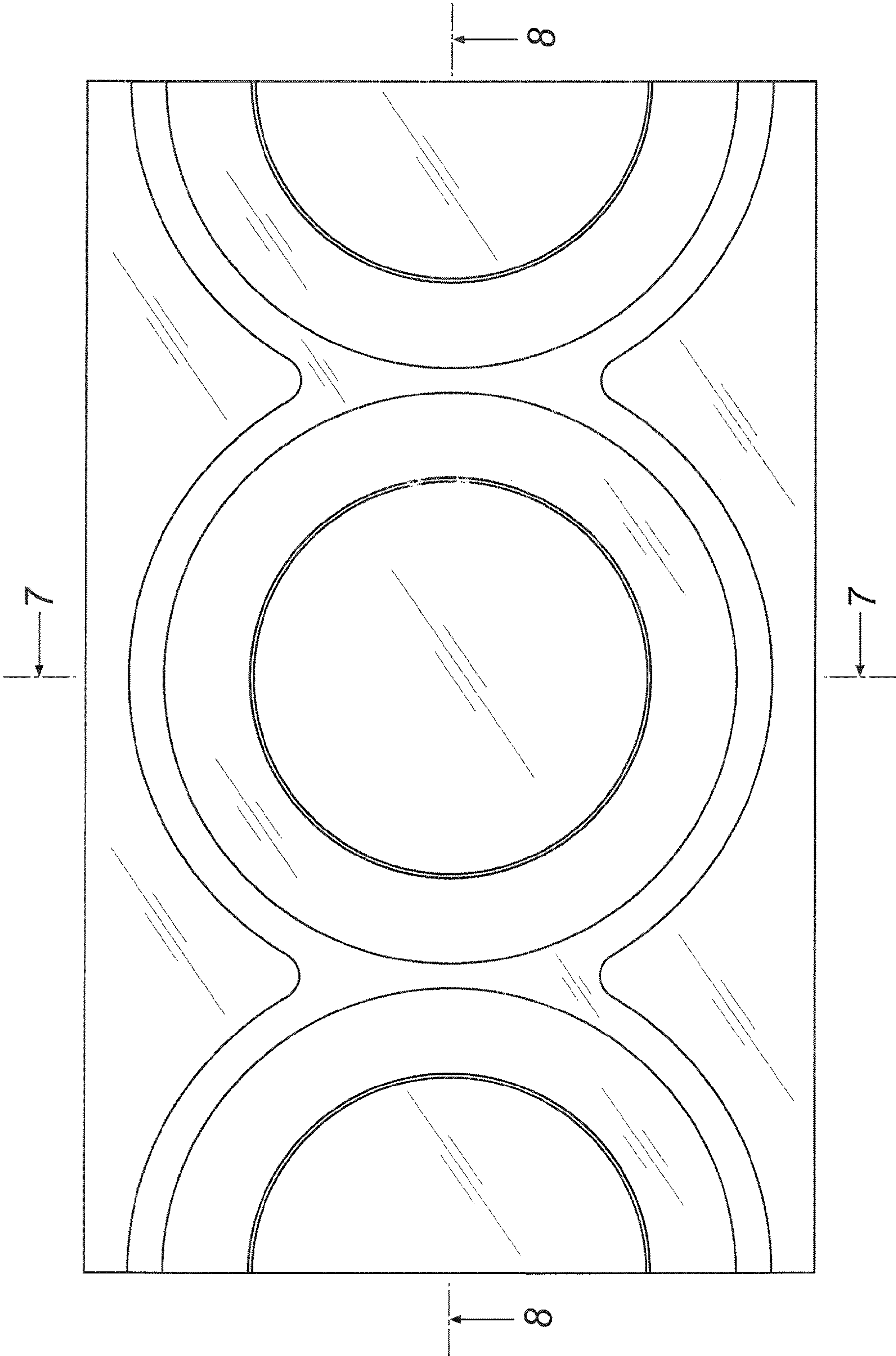


FIG. 2

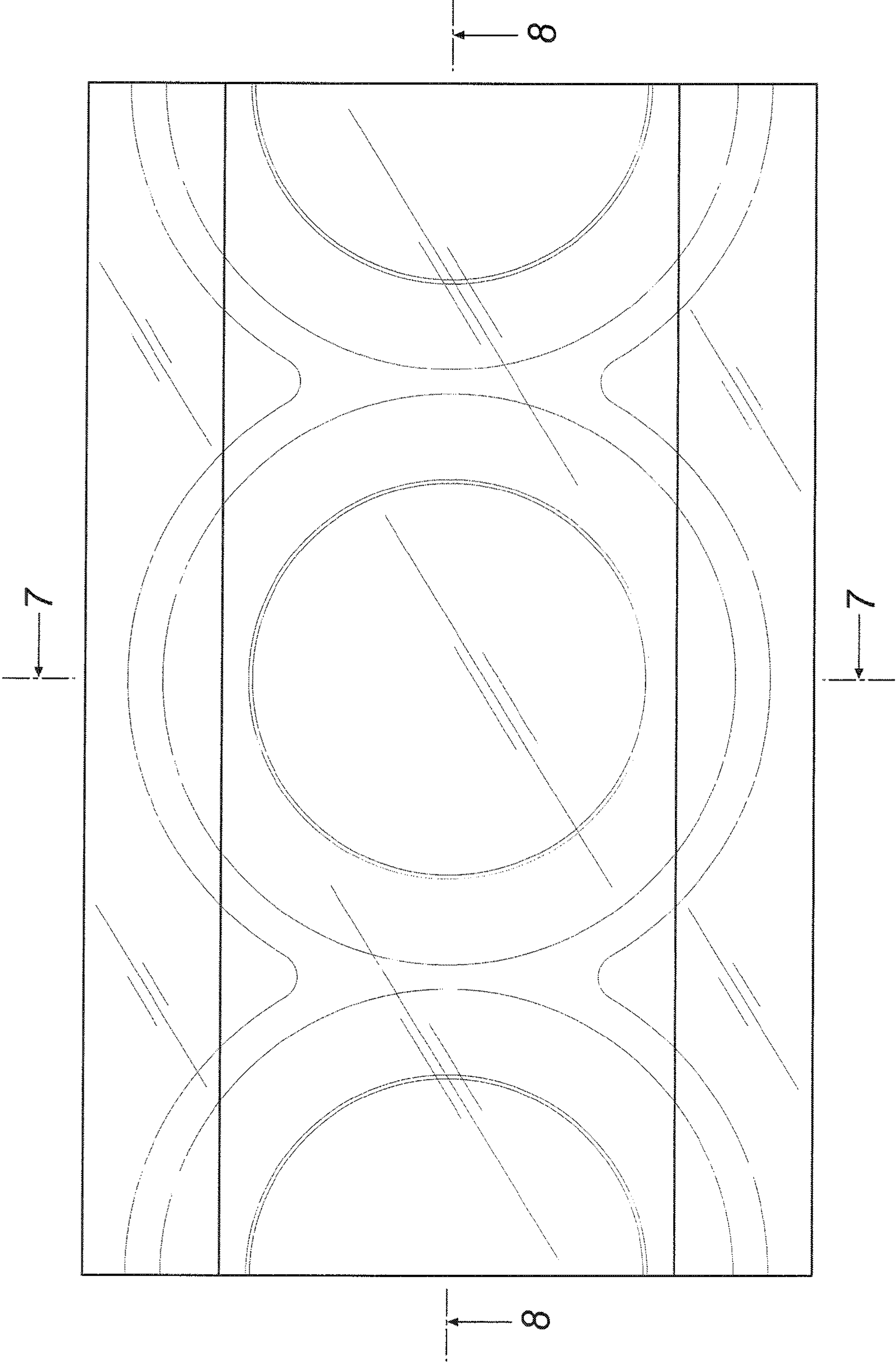


FIG. 3

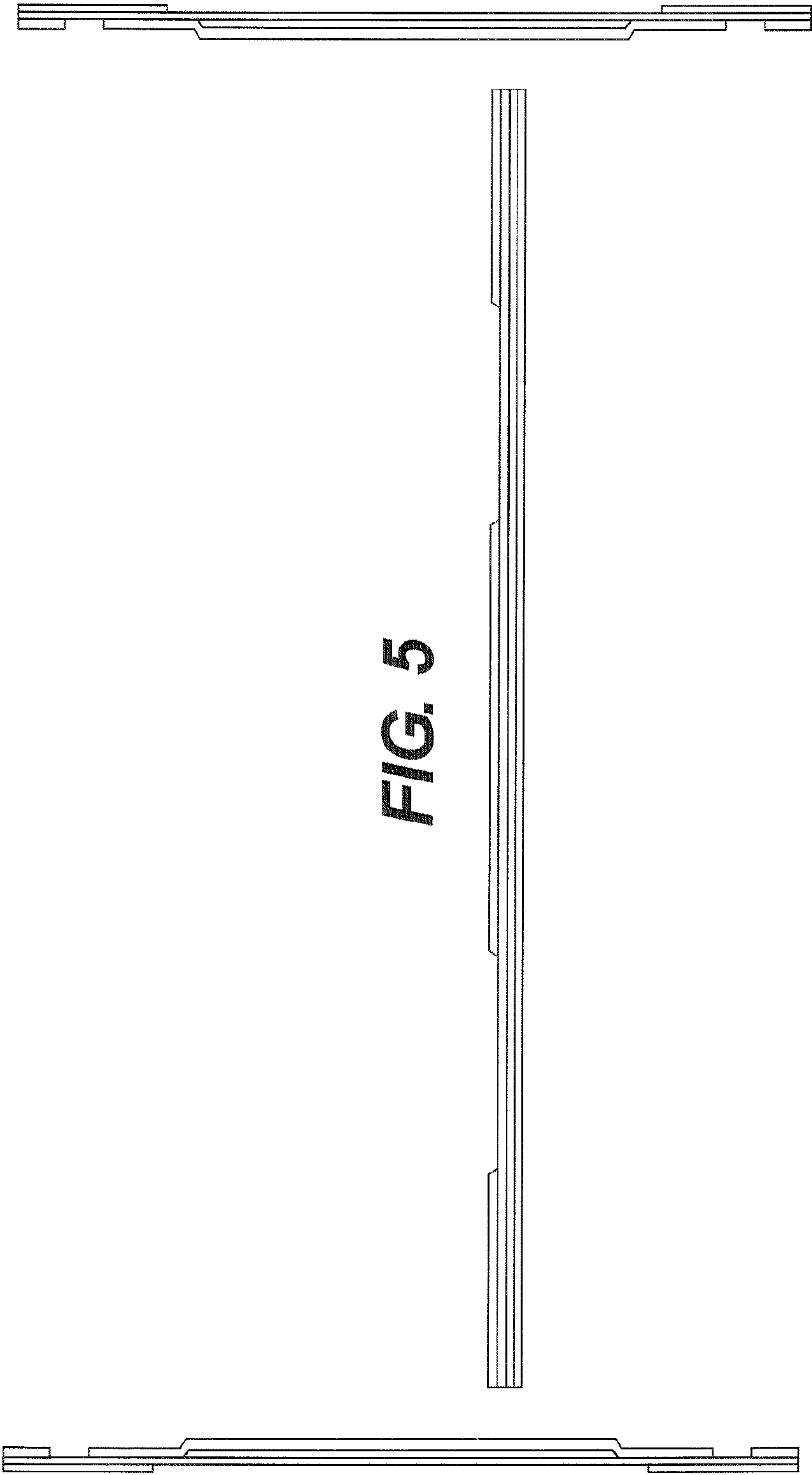


FIG. 5

FIG. 6

FIG. 4

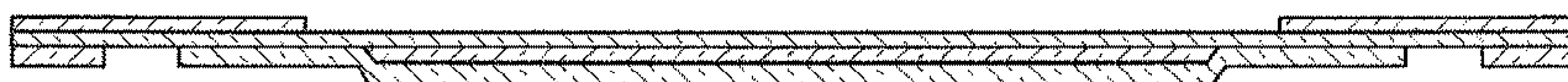


FIG. 7



FIG. 8