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(12) **United States Design Patent**
Sato

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(54) **HEAT RADIATION FIN OF HEAT INSULATING CYLINDER FOR MANUFACTURING SEMICONDUCTOR WAFERS**

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(**) Term: **14 Years**

(21) Appl. No.: **29/342,852**

(22) Filed: **Sep. 2, 2009**

(30) **Foreign Application Priority Data**

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(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
206/454, 711; 118/728, 729; 211/41.18;
432/241, 253, 258

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,421,595	A *	6/1995	Cripe et al.	279/3
D404,372	S *	1/1999	Ishii	D13/182
6,056,123	A *	5/2000	Niemirowski et al.	206/711
6,062,853	A *	5/2000	Shimazu et al.	432/258
6,110,285	A *	8/2000	Kitazawa et al.	118/715
7,033,168	B1 *	4/2006	Gupta et al.	432/253
7,484,958	B2 *	2/2009	Kobayashi	432/258
D600,220	S *	9/2009	Sato	D13/182

2002/0113027 A1* 8/2002 Minami et al. 211/41.18

* cited by examiner

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(57) **CLAIM**

The ornamental design for a heat radiation fin of heat insulating cylinder for manufacturing semiconductor wafers, as shown and described.

DESCRIPTION

FIG. 1 is front perspective view of a heat radiation fin of heat insulating cylinder for manufacturing semiconductor wafers illustrating my new design;

FIG. 2 is a front view thereof;

FIG. 3 is a rear view thereof;

FIG. 4 is a right side view thereof;

FIG. 5 is a left side view thereof;

FIG. 6 is a top plan view thereof;

FIG. 7 is a bottom plan view thereof;

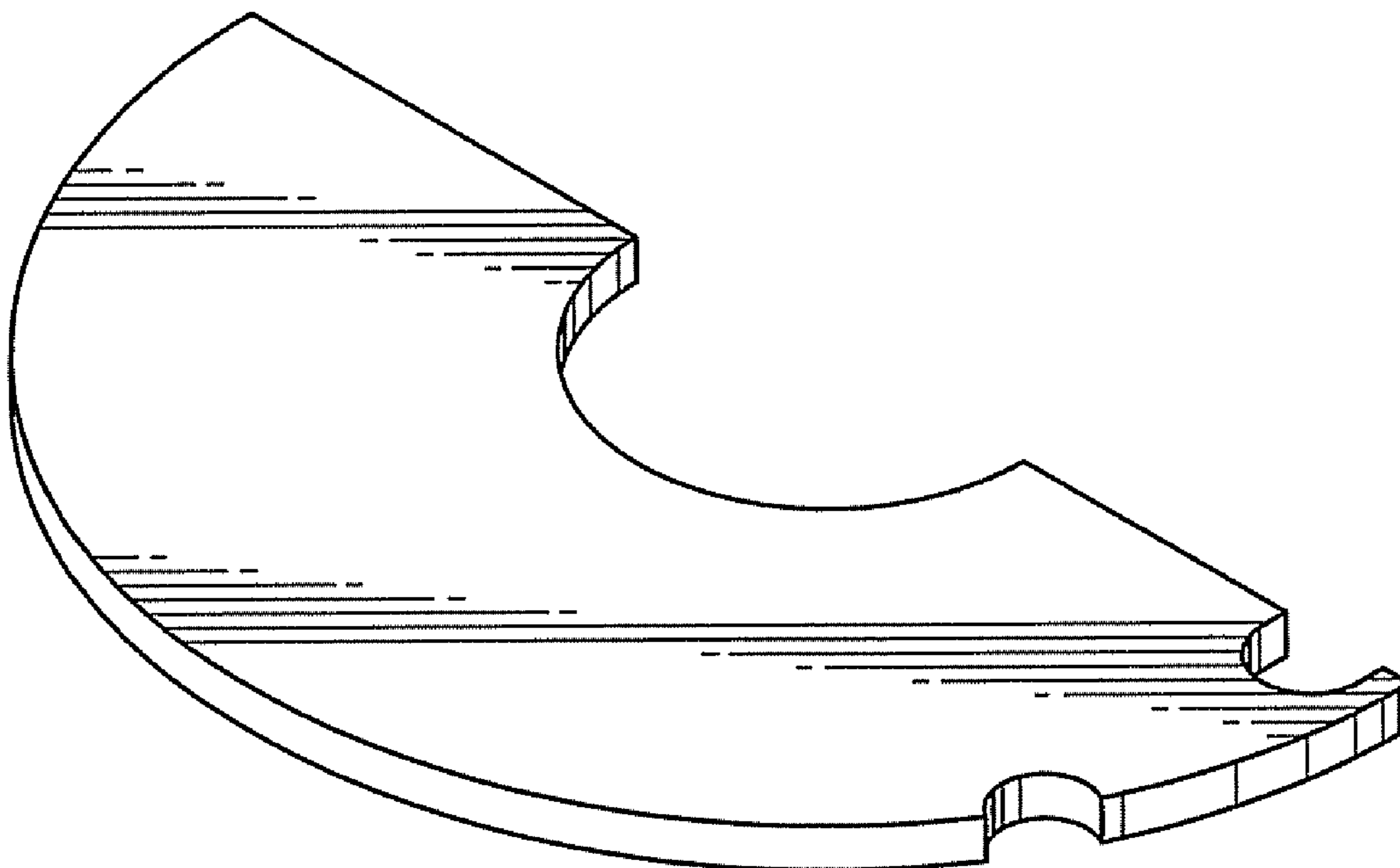
FIG. 8 is a cross-sectional view thereof taken through line 8—8 of FIG. 6;

FIG. 9 is a cross-sectional view thereof taken through line 9—9 of FIG. 6; and,

FIG. 10 is a front perspective view of a heat radiation fin of heat insulating cylinder for manufacturing semiconductor wafers in use.

The broken lines are shown for illustrative purposes only and form no part of the claimed design.

1 Claim, 3 Drawing Sheets



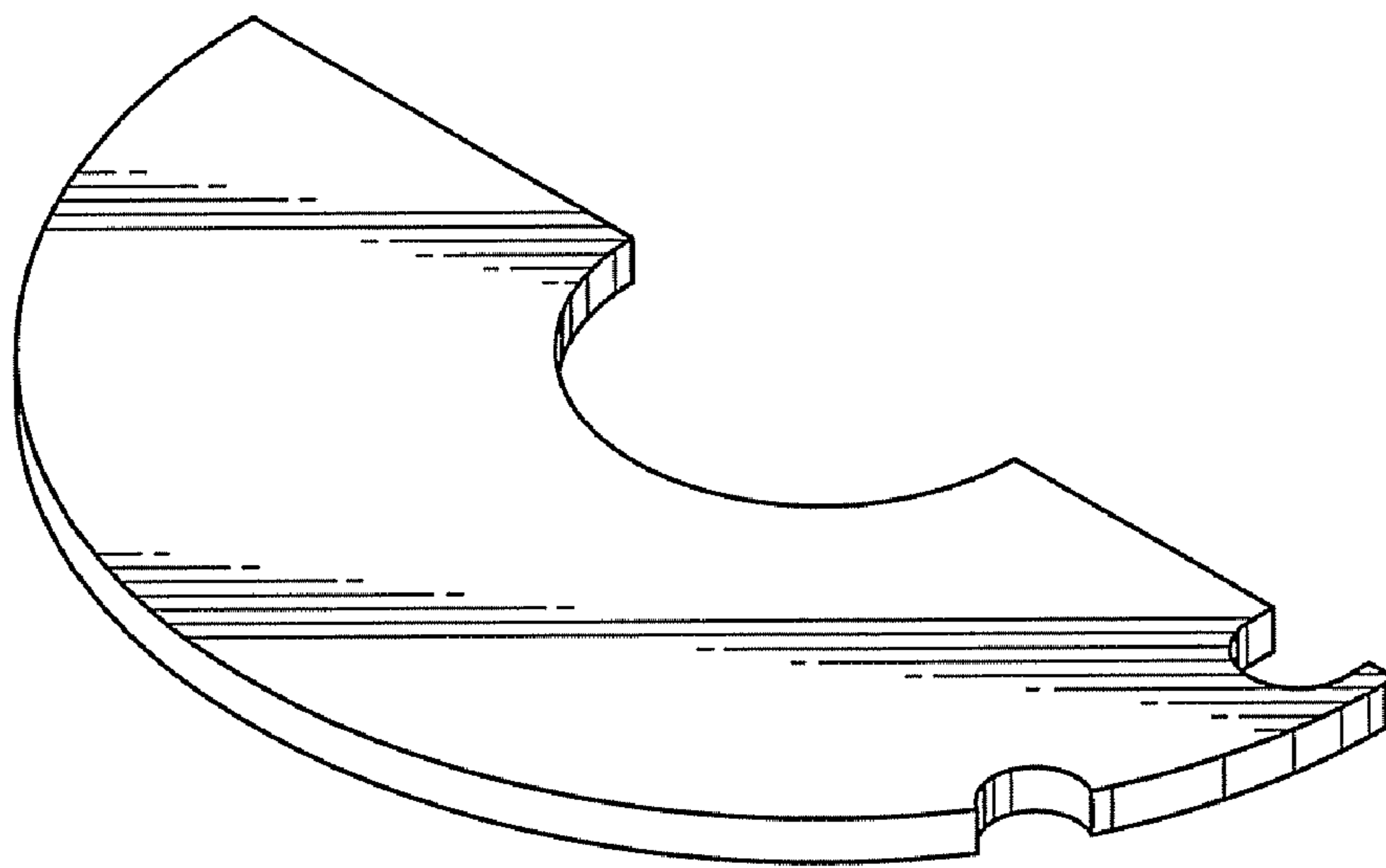


FIG. 1



FIG. 2



FIG. 3



FIG. 4



FIG. 5

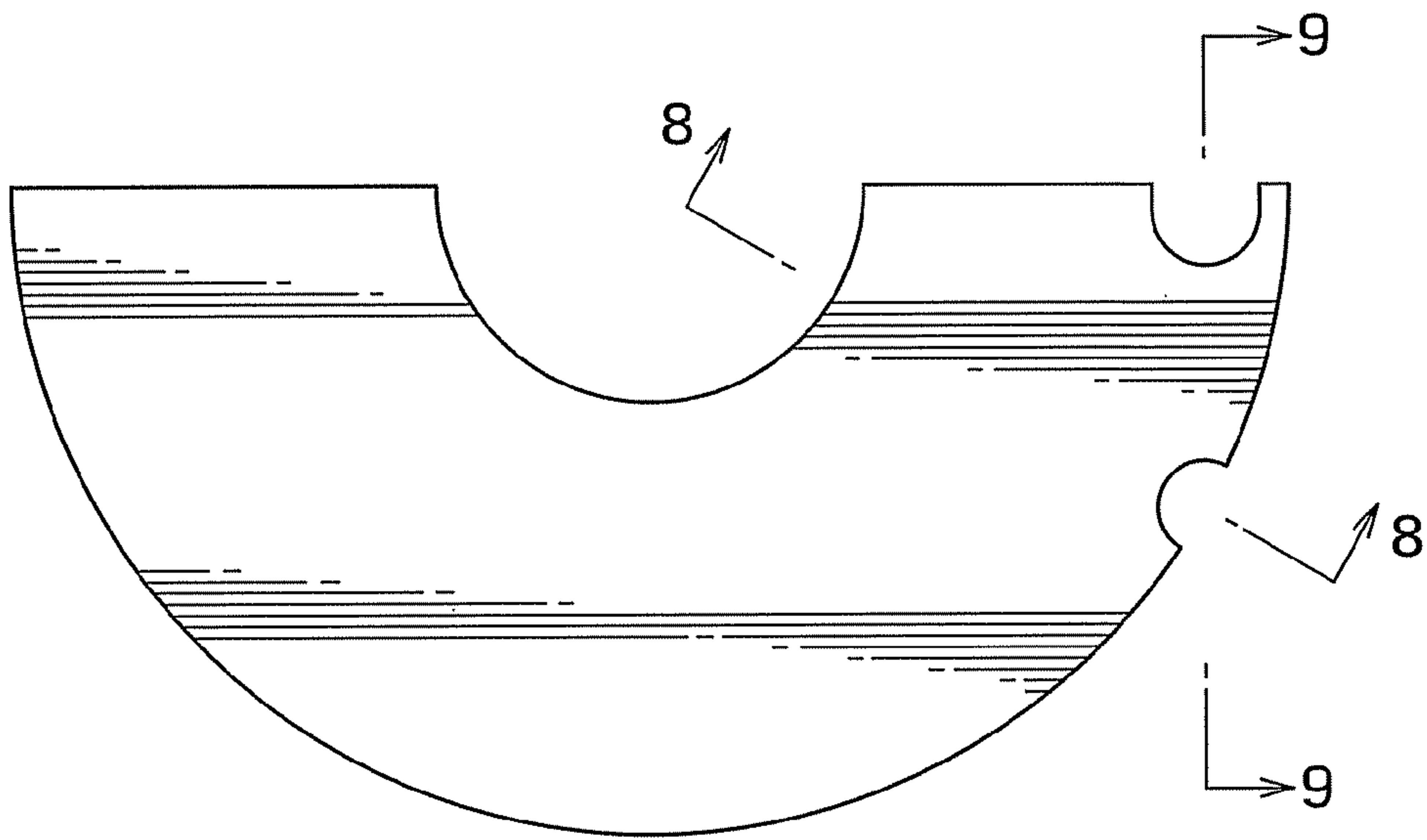


FIG. 6

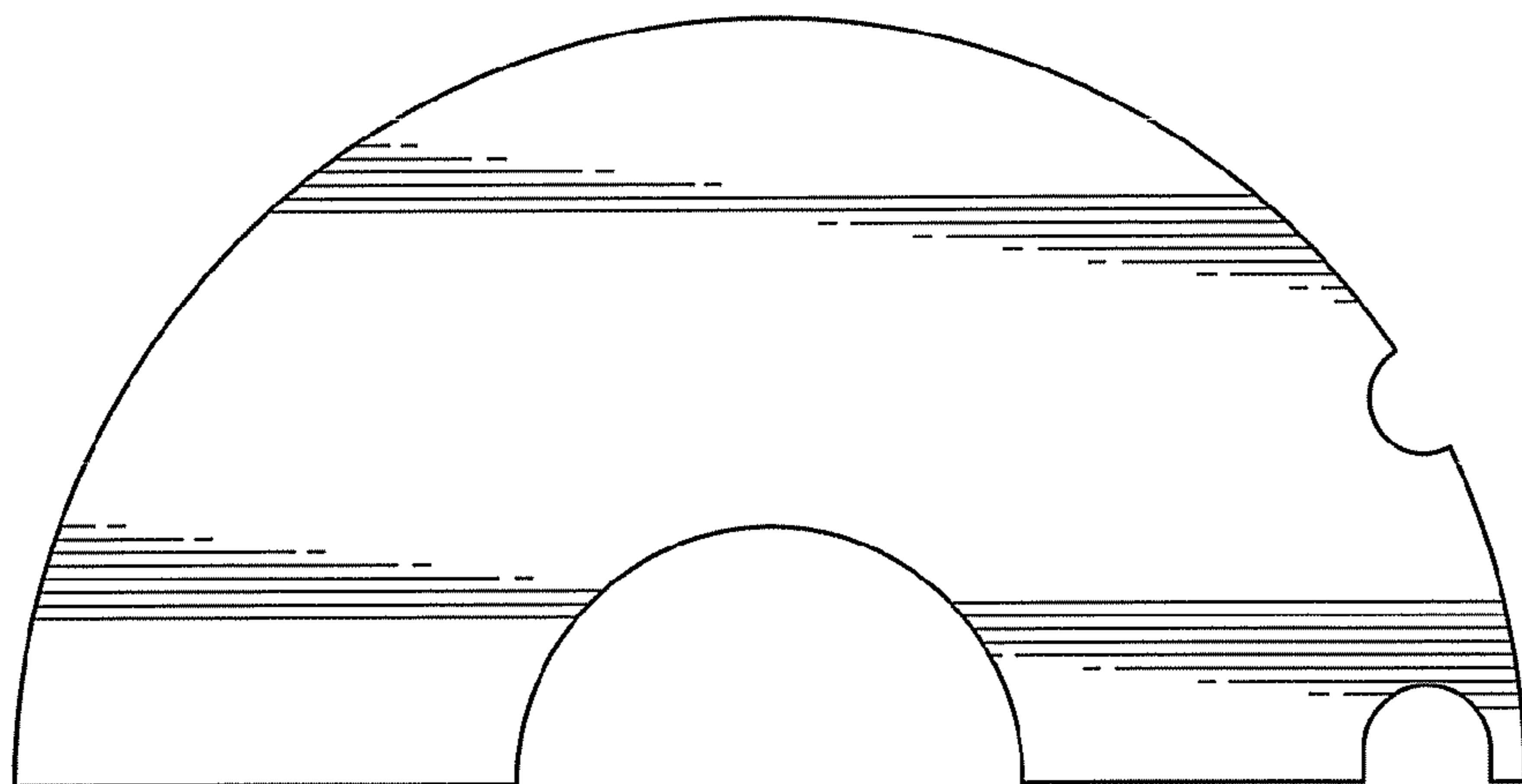


FIG. 7



FIG. 8



FIG. 9

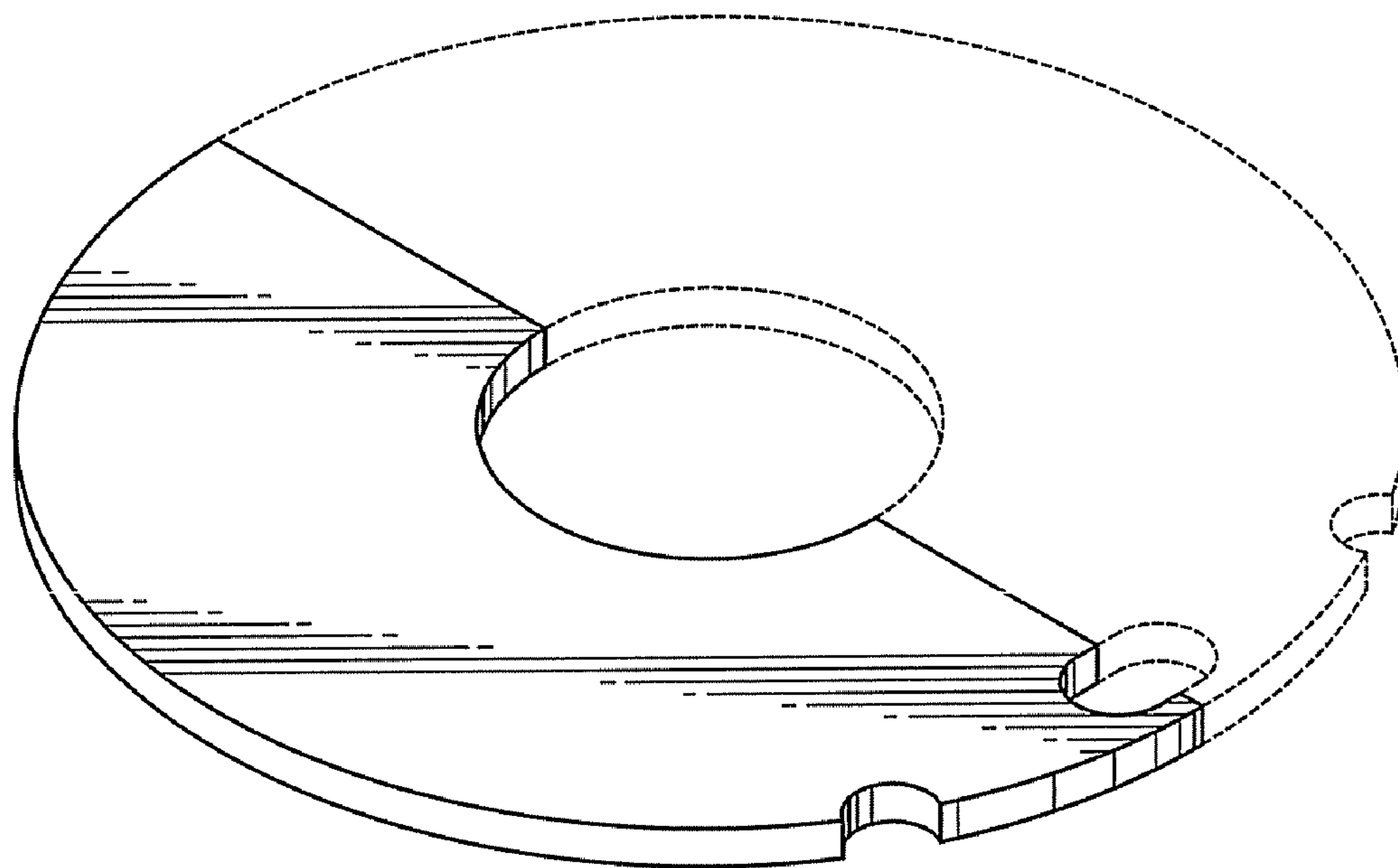


FIG. 10