



US00D611013S

(12) **United States Design Patent**  
**Takahashi**

(10) **Patent No.:** **US D611,013 S**  
(45) **Date of Patent:** **\*\* Mar. 2, 2010**

(54) **PROCESS TUBE FOR MANUFACTURING SEMICONDUCTOR WAFERS**

(75) Inventor: **Kiyohiko Takahashi**, Oshu (JP)

(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)

(\*\*) Term: **14 Years**

(21) Appl. No.: **29/309,700**

(22) Filed: **Sep. 26, 2008**

(30) **Foreign Application Priority Data**

Mar. 28, 2008 (JP) ..... 2008-007851

(51) **LOC (9) Cl.** ..... **13-03**

(52) **U.S. Cl.** ..... **D13/182**

(58) **Field of Classification Search** ..... D13/182;  
D7/600.2; D23/266; 83/35, 39; 118/715;  
138/92, 118, 118.1, 121, 178; 206/454, 711;  
211/41.18; 414/935; 432/253

See application file for complete search history.

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

- 4,950,870 A \* 8/1990 Mitsuhashi et al. .... 219/390
- D324,645 S \* 3/1992 Magro et al. .... D8/380
- D404,368 S \* 1/1999 Shimazu ..... D13/182
- D405,429 S \* 2/1999 Hanagata et al. .... D13/182
- D405,430 S \* 2/1999 Matsushima ..... D13/182
- D407,696 S \* 4/1999 Shimazu ..... D13/182
- 5,948,300 A \* 9/1999 Gero et al. .... 219/390
- 5,968,593 A \* 10/1999 Sakamoto et al. .... 427/248.1
- D417,438 S \* 12/1999 Matsushima ..... D13/182

- D424,024 S \* 5/2000 Hanagata et al. .... D13/182
- D552,047 S \* 10/2007 Sugawara ..... D13/182
- D586,768 S \* 2/2009 Inoue et al. .... D13/182
- 2007/0181062 A1 \* 8/2007 Kim et al. .... 118/715

\* cited by examiner

*Primary Examiner*—Selina Sikder

(74) *Attorney, Agent, or Firm*—Smith, Gambrell & Russell, LLP

(57) **CLAIM**

The ornamental design for a process tube for manufacturing semiconductor wafers, as shown and described.

**DESCRIPTION**

FIG. 1 is a perspective view;

FIG. 2 is a front view;

FIG. 3 is a rear view;

FIG. 4 is a left side view and the right side being a mirror image thereof;

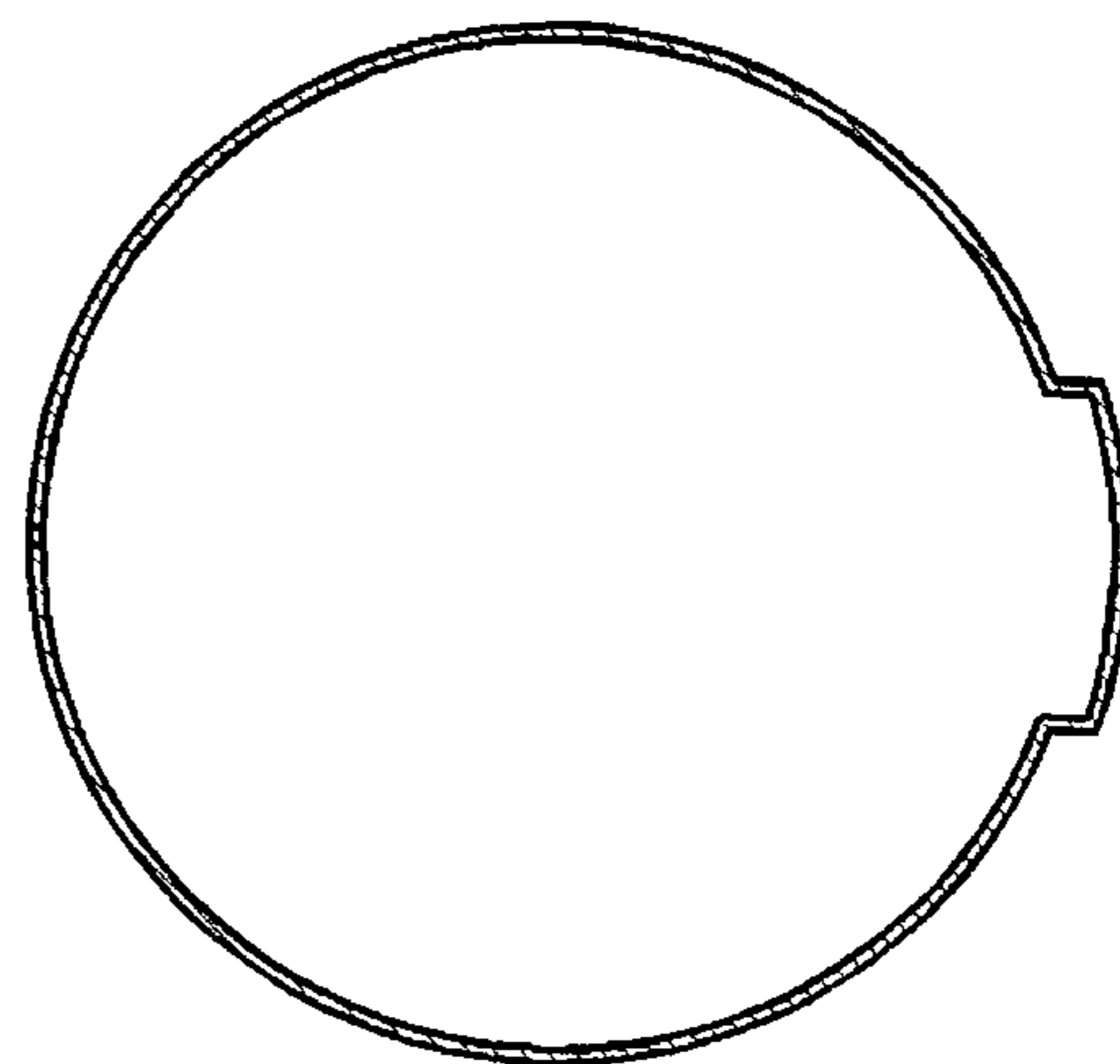
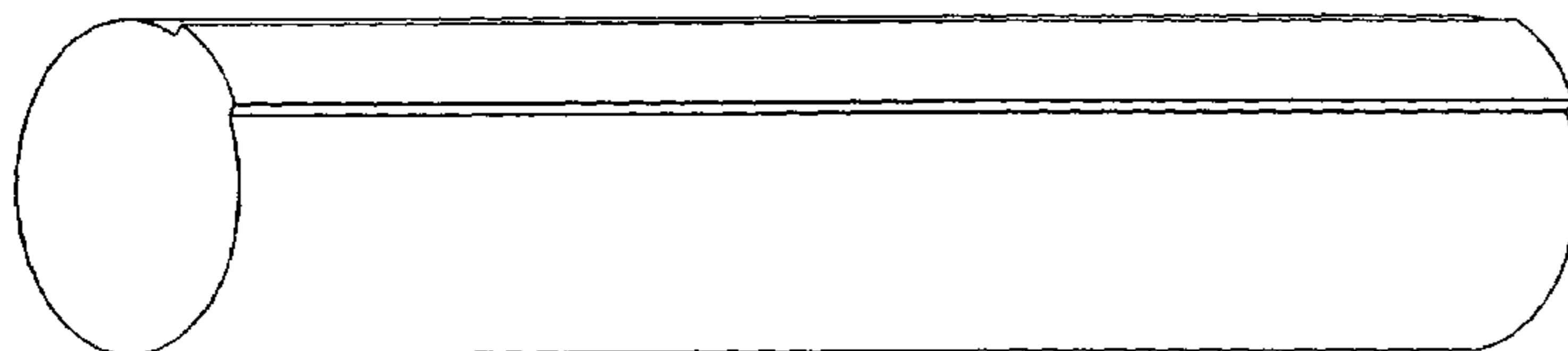
FIG. 5 is a plan view and the bottom plan being a mirror image thereof;

FIG. 6 is a sectional view thereof along 6—6 of the plan view shown in FIG. 5;

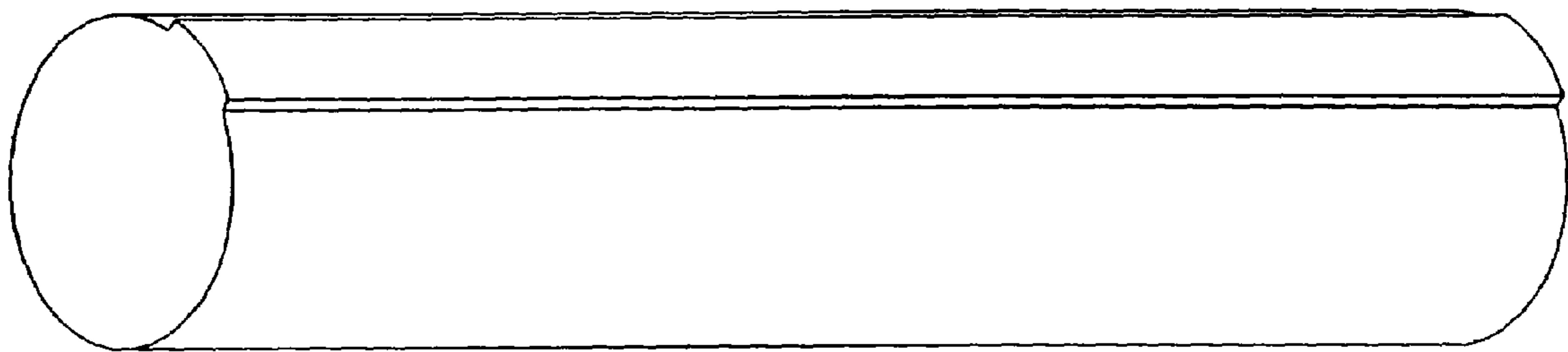
FIG. 7 is an enlarged sectional view along 7—7 of the rear view shown in FIG. 3; and,

FIG. 8 is a view of process tube for manufacturing semiconductor wafers in use wherein the broken line showing of the environment is for illustrative purposes only and forms no part of the claimed design.

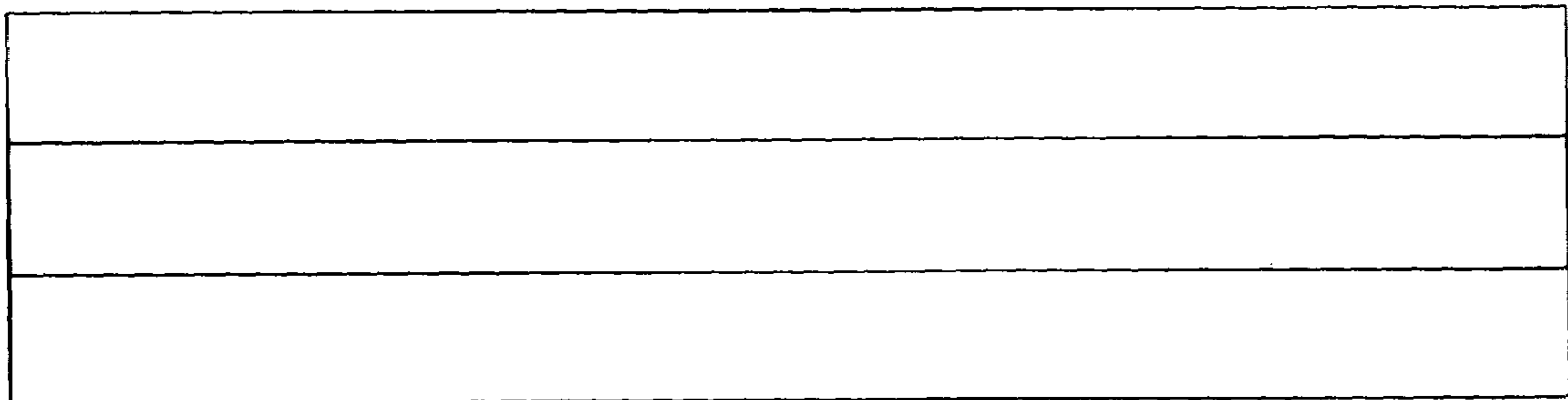
**1 Claim, 8 Drawing Sheets**



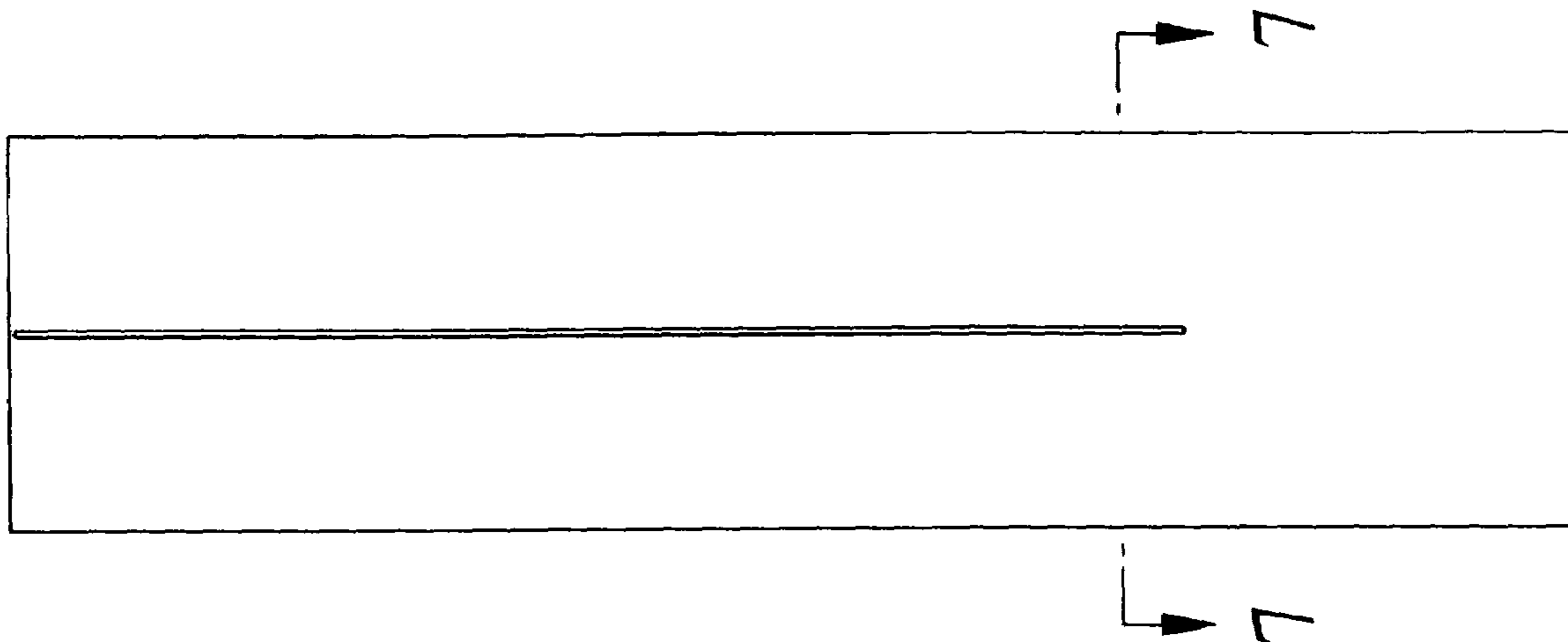
**FIGURE 1**



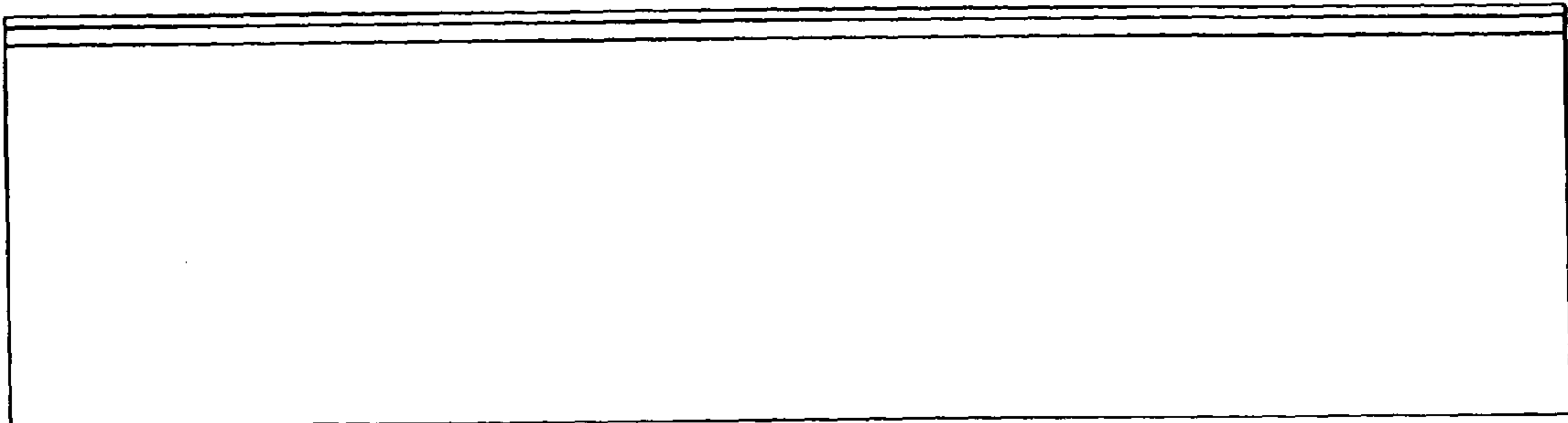
**FIGURE 2**



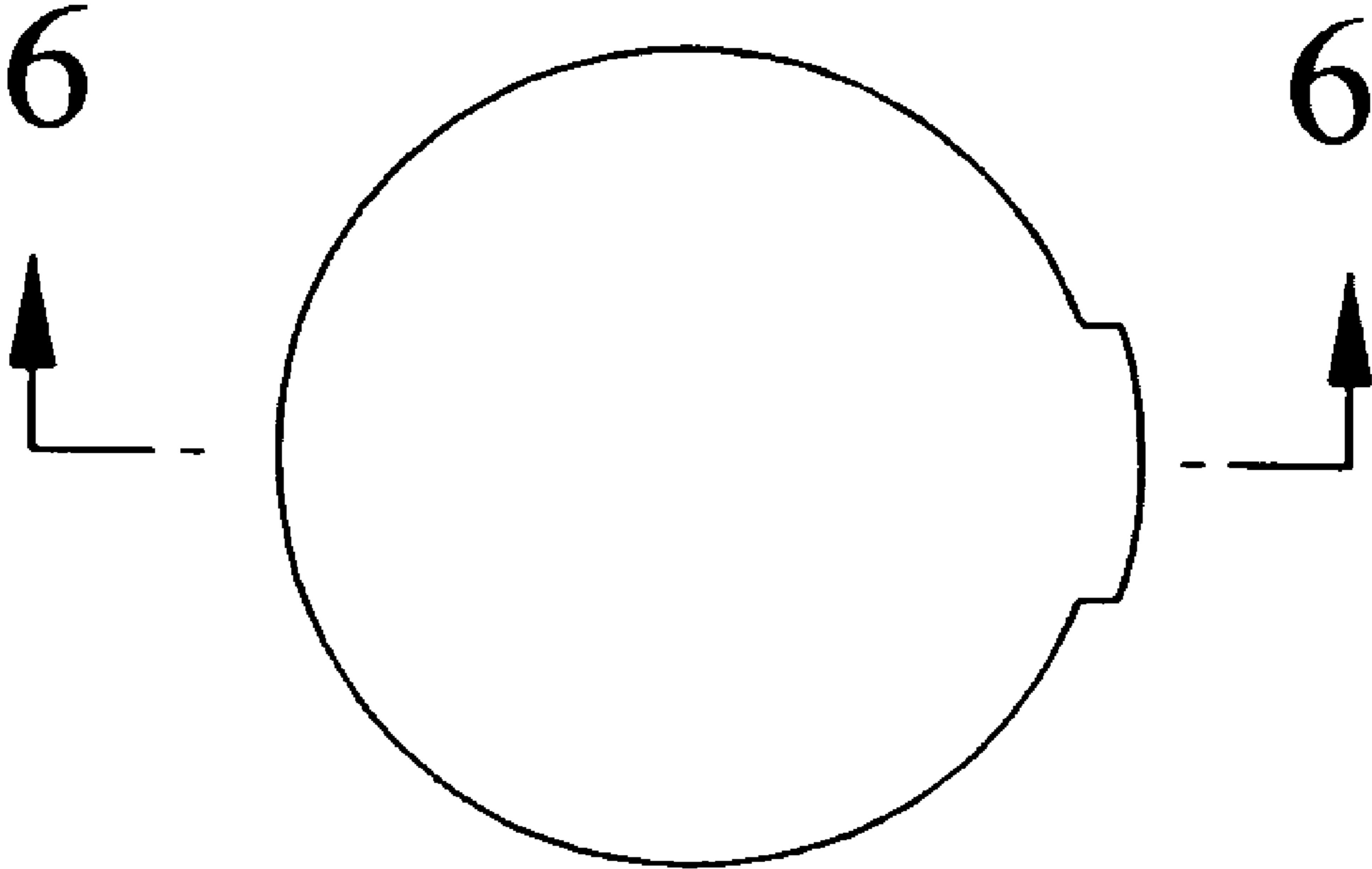
**FIGURE 3**



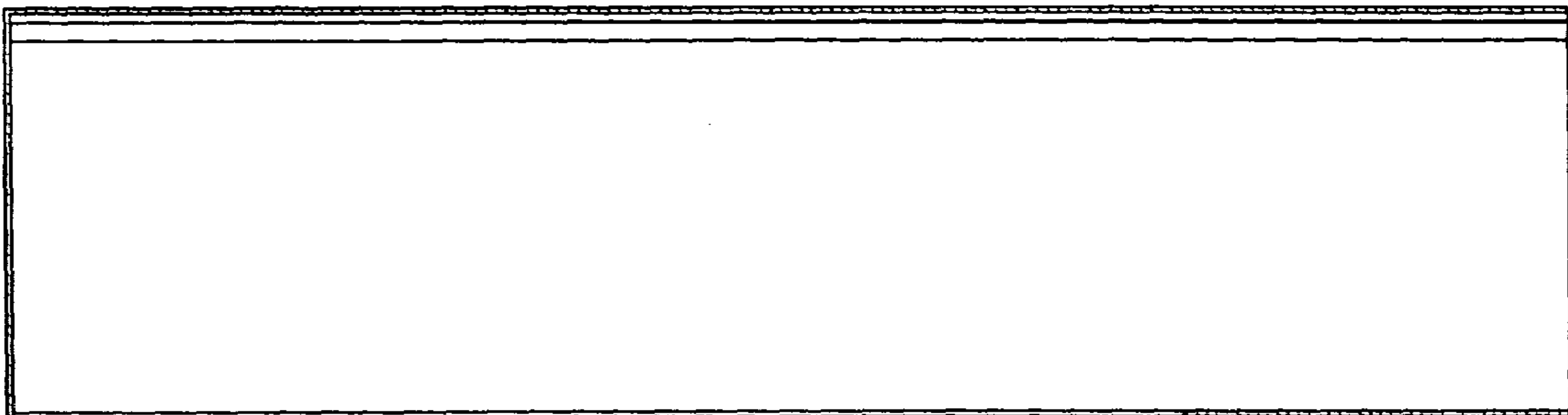
**FIGURE 4**



# FIGURE 5



**FIGURE 6**



# FIGURE 7

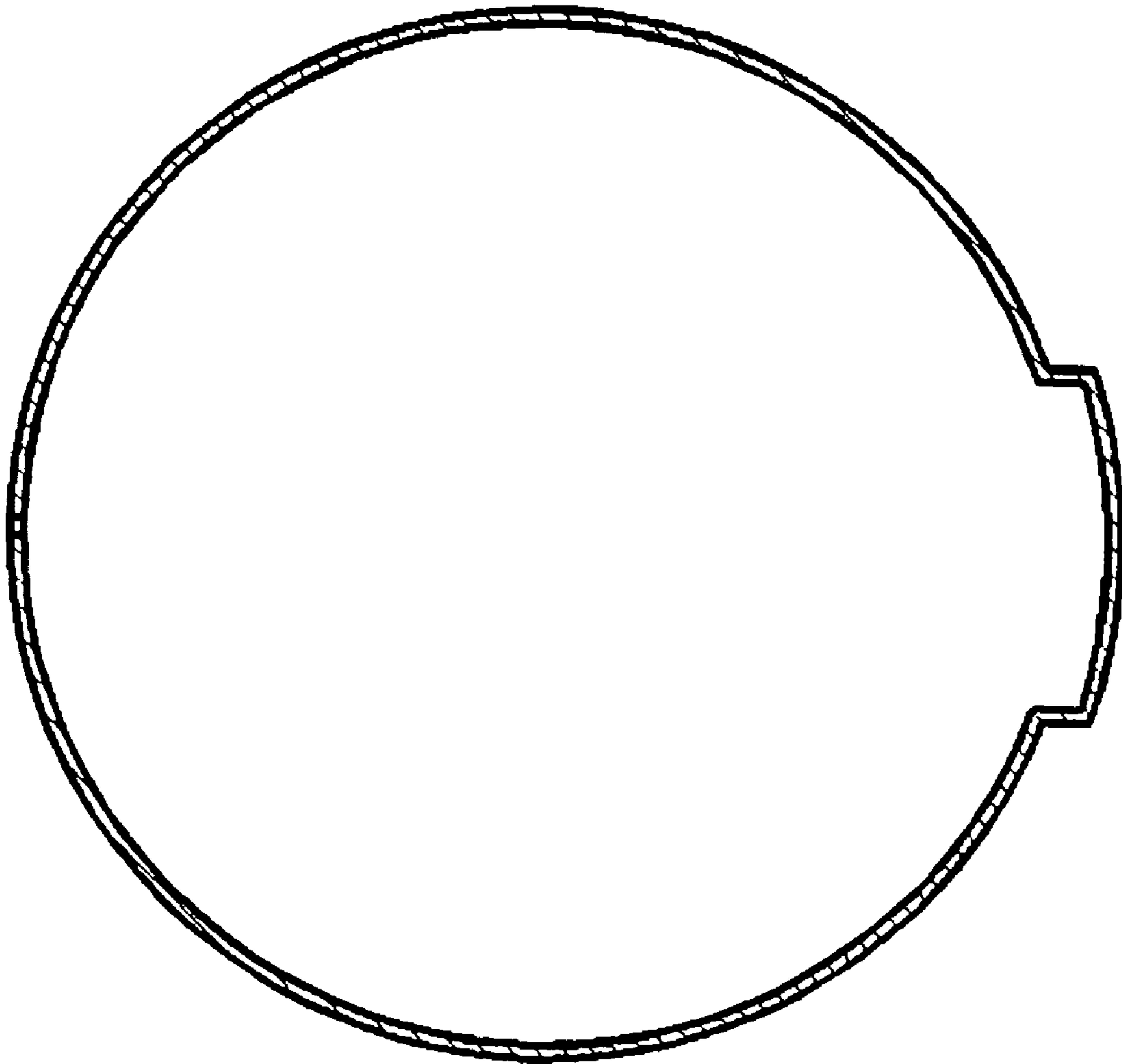




FIG. 8

