US00D608741S

(12) United States Design Patent

Miyashita

(10) Patent No.: US D608,741 S
(45) Date of Patent: ** Jan. 26, 2010

(54) **SUBSTRATE FOR ELECTRIC CIRCUIT**

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(73) Assignee: **Panasonic Corporation**, Osaka (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/320,624**

(22) Filed: **Jun. 30, 2008**

(30) **Foreign Application Priority Data**

Mar. 13, 2008 (JP) 2008-006279

(51) **LOC (9) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Classification Search** D13/182; D7/393, 394; D8/303, 315, 316, 317; 174/250; 257/718; 361/748, 760, 777; 439/67; D6/446
See application file for complete search history.

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(57) **CLAIM**

I claim the ornamental design for a substrate for electric circuit, as shown and described.

DESCRIPTION

FIG. **1** is a front perspective view of a first embodiment of a substrate for electric circuit of the present invention;

FIG. **2** is a front view thereof;

FIG. **3** is a rear view thereof;

FIG. **4** is a top view thereof;

FIG. **5** is a bottom view thereof;

FIG. **6** is a first side view thereof;

FIG. **7** is a second side view thereof;

FIG. **8** is a front perspective view of a second embodiment of a substrate for electric circuit of the present invention;

FIG. **9** is a front view thereof;

FIG. **10** is a rear view thereof;

FIG. **11** is a top view thereof;

FIG. **12** is a bottom view thereof;

FIG. **13** is a first side view thereof; and,

FIG. **14** is a second side view thereof.

The broken line showing of substrate for electric circuit is included for the purpose of illustrating environment and forms no part of the claimed design. Additionally, the unevenly broken lines in the drawings define the limits of the claimed design.

1 Claim, 14 Drawing Sheets

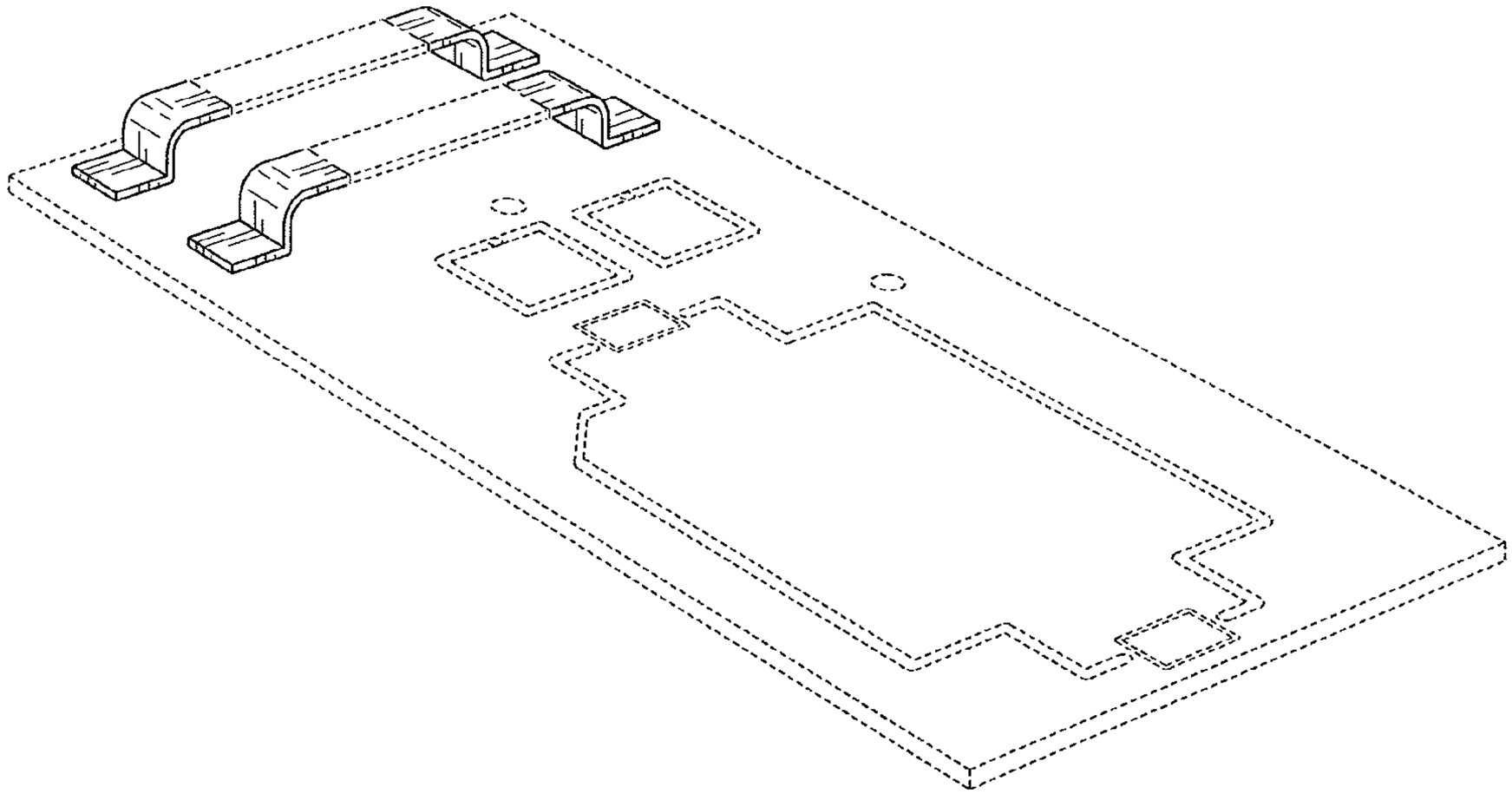

FIG.1

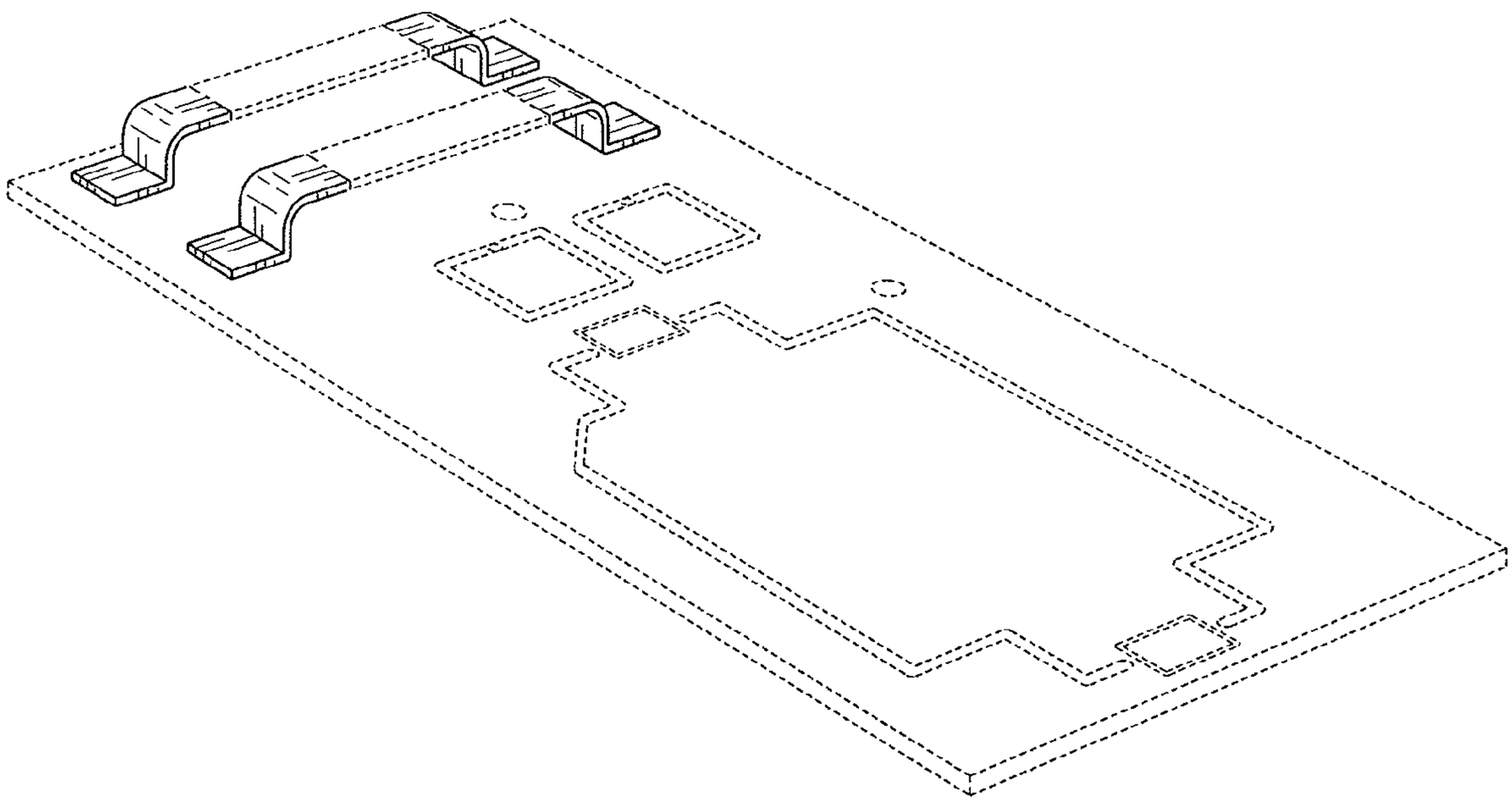

FIG.2

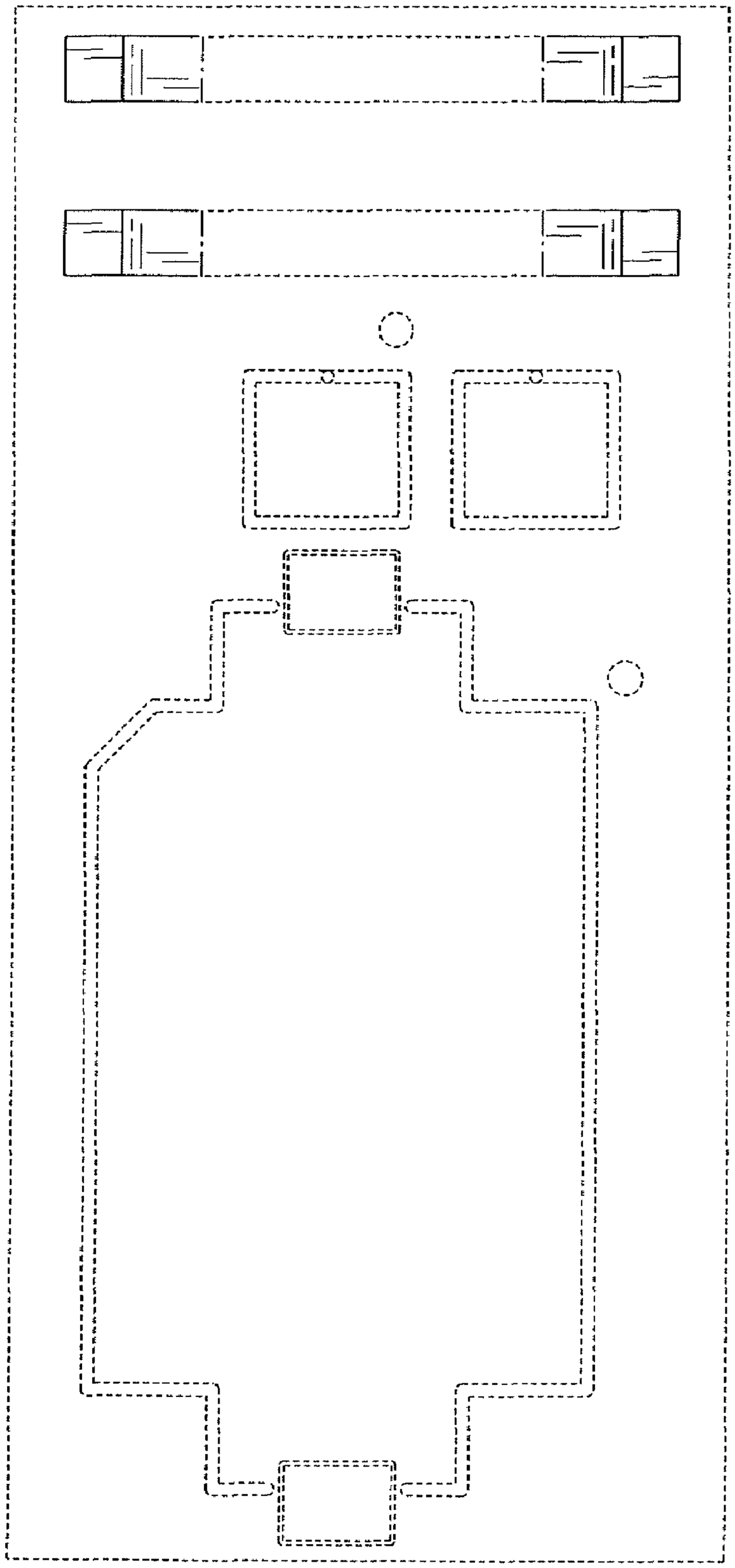

FIG.3

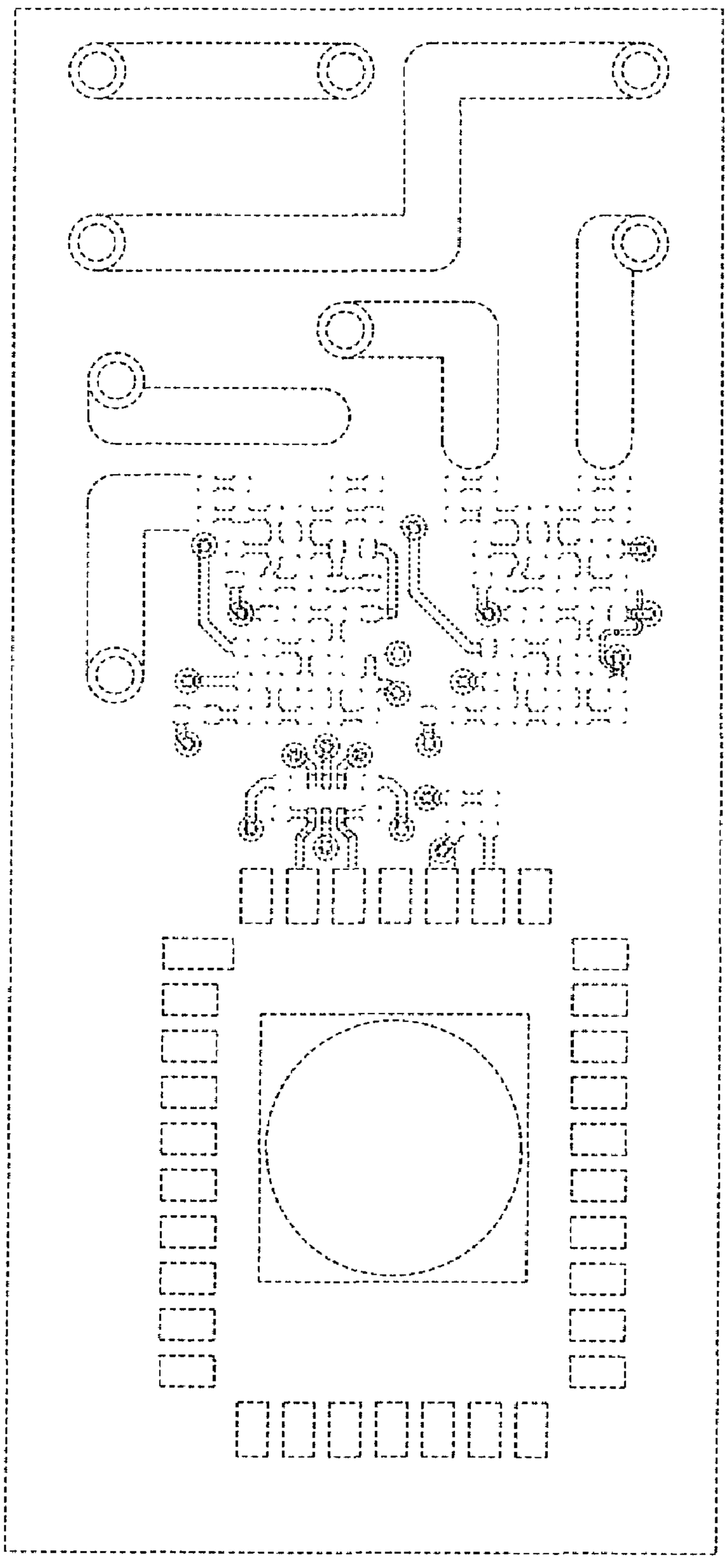

FIG.4

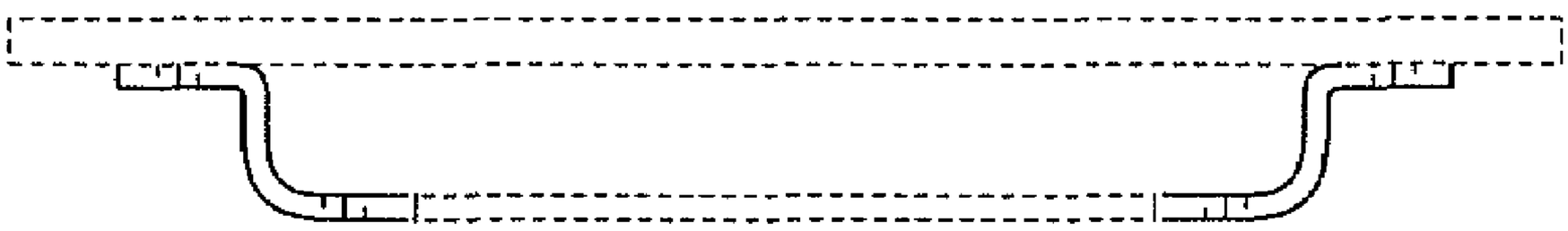

FIG.5

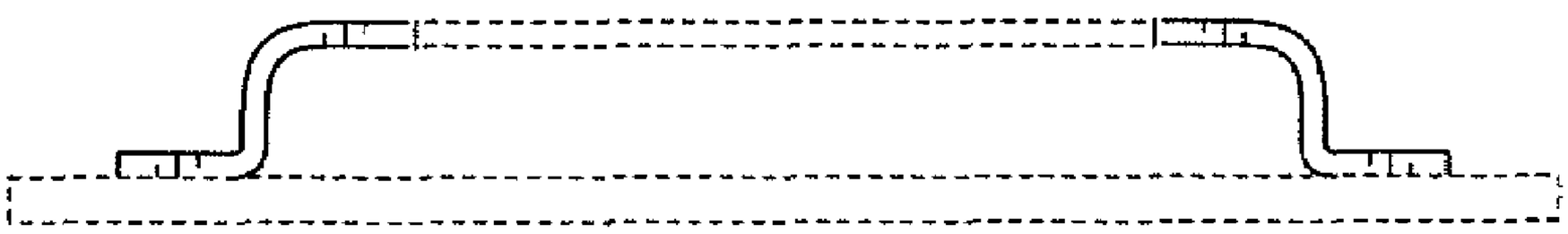

FIG.6

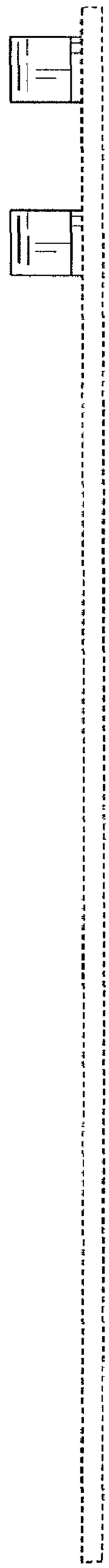

FIG.7

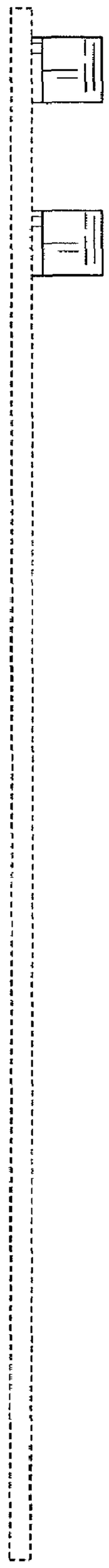

FIG.8

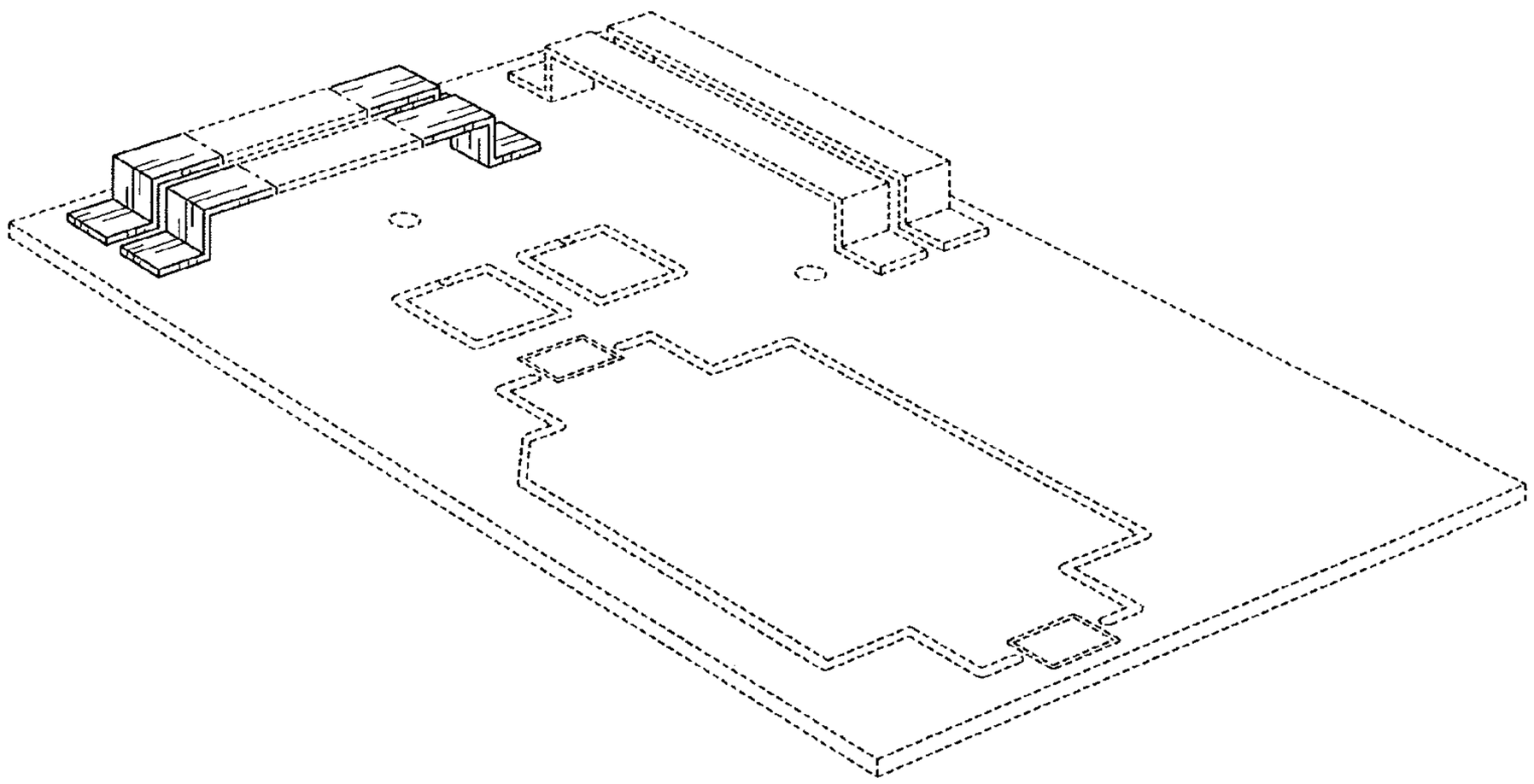

FIG.9

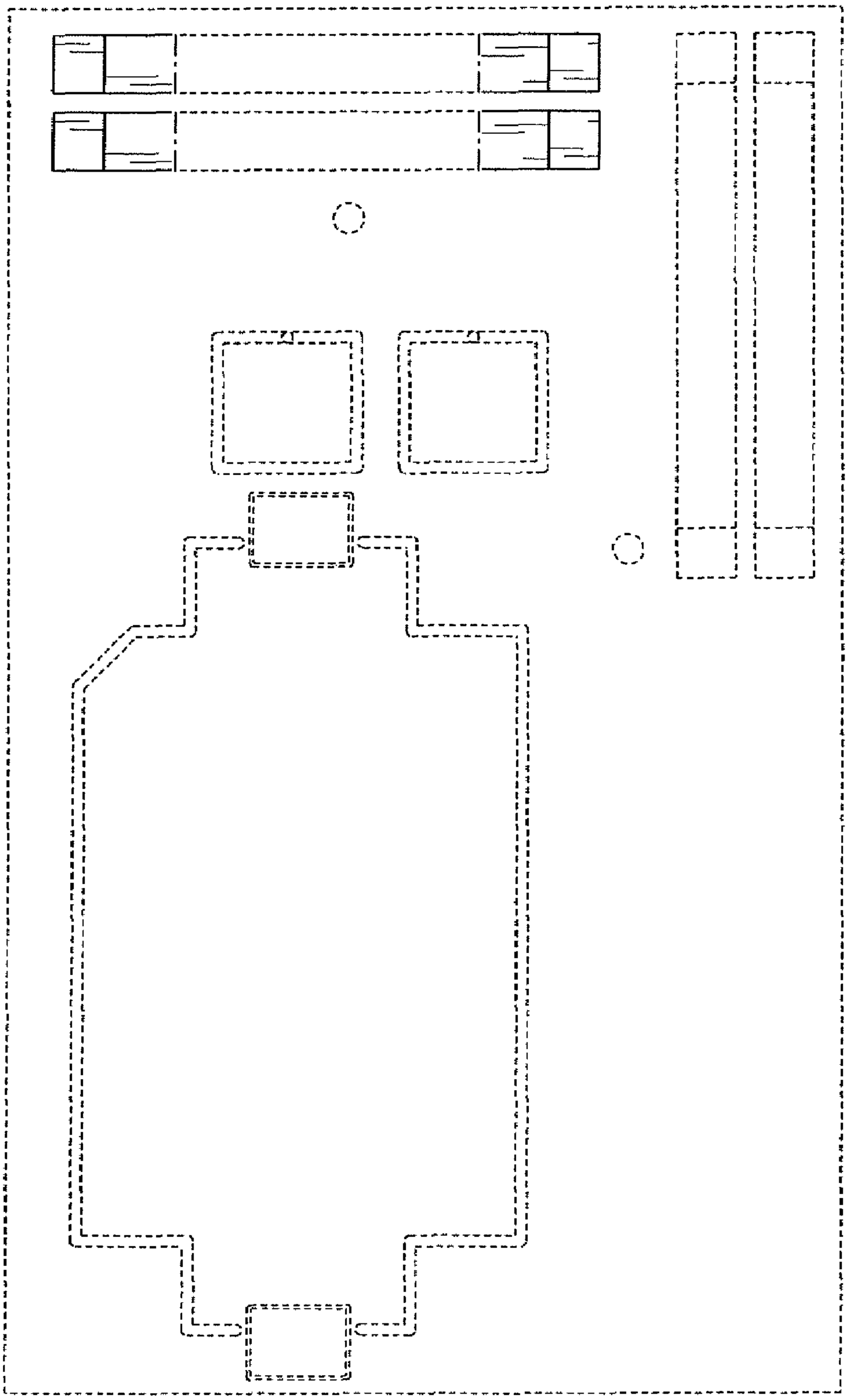

FIG.10

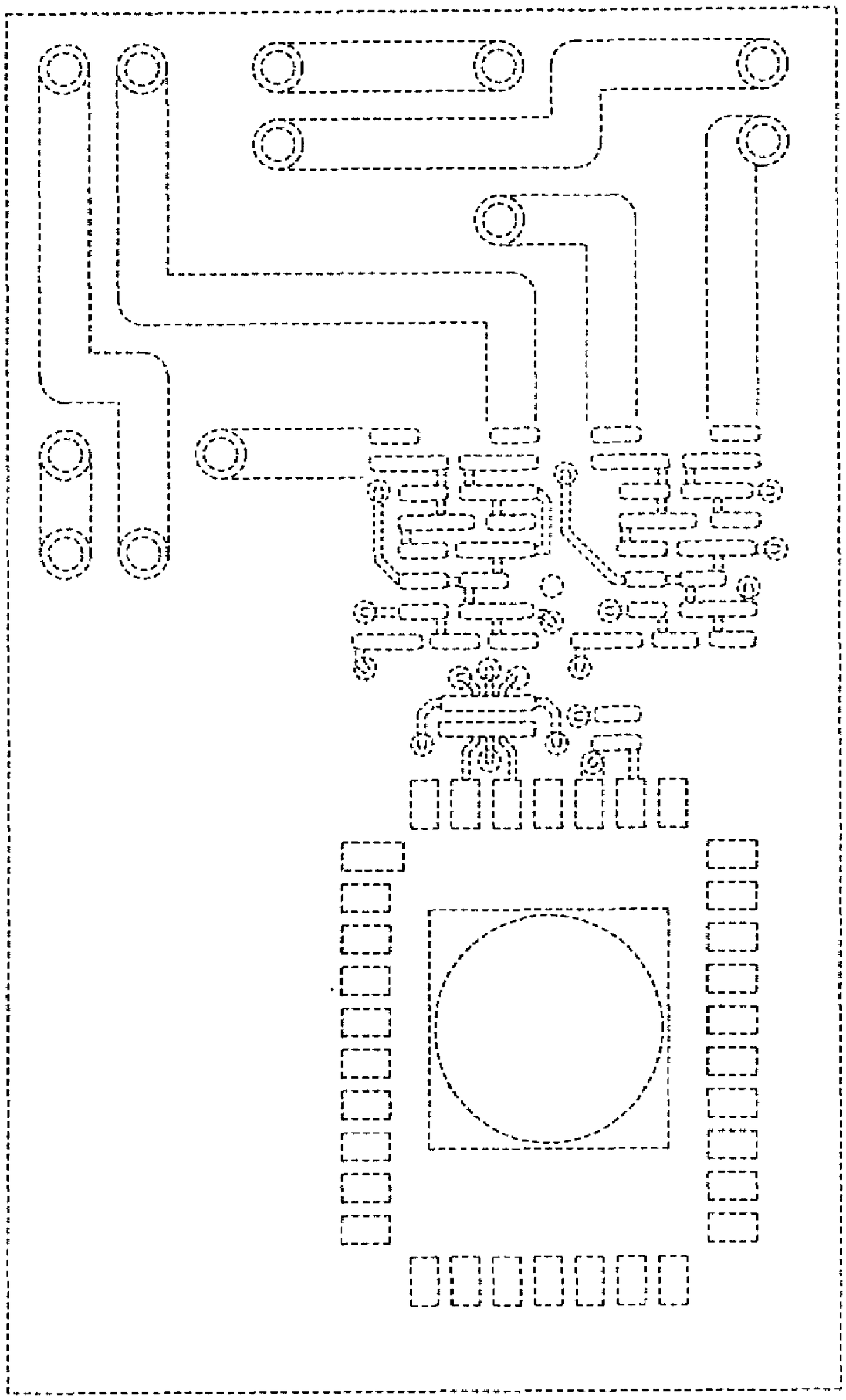

FIG.11

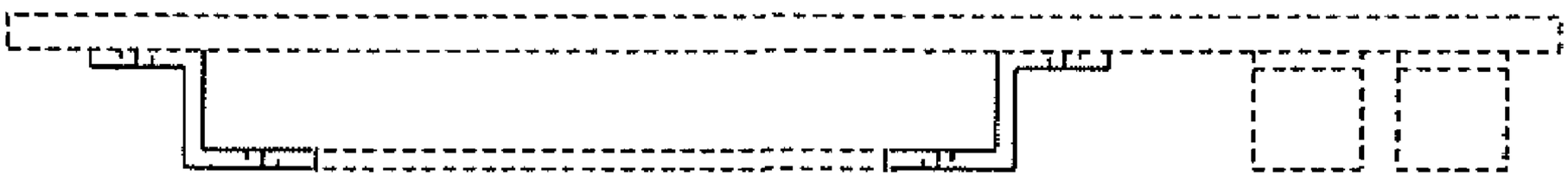

FIG.12

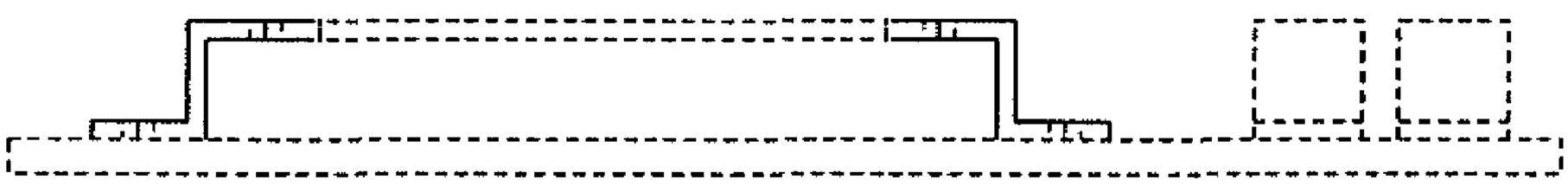

FIG.13

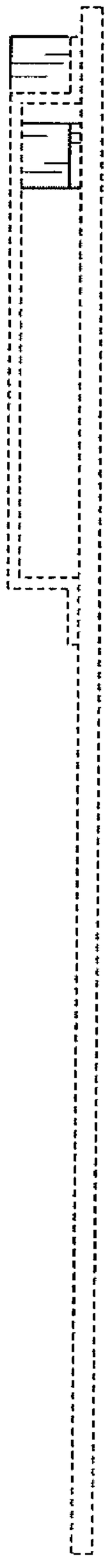

FIG.14