



US00D600659S

(12) **United States Design Patent**
Matsuura et al.

(10) **Patent No.:** **US D600,659 S**

(45) **Date of Patent:** **** Sep. 22, 2009**

(54) **PROCESS TUBE FOR MANUFACTURING SEMICONDUCTOR WAFERS**

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(57) **CLAIM**

(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)

The ornamental design for a process tub for manufacturing semiconductor wafers, as shown and described.

(**) Term: **14 Years**

(21) Appl. No.: **29/273,613**

DESCRIPTION

(22) Filed: **Mar. 9, 2007**

(30) **Foreign Application Priority Data**

Sep. 12, 2006 (JP) 2006-024315

(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
118/715, 724, 725; 219/390, 486, 523; 432/247
See application file for complete search history.

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FIG. 1 is a perspective view of the design for a process tube for manufacturing semiconductor wafers in accordance with the invention;

FIG. 2 is a front view thereof;

FIG. 3 is a rear view thereof;

FIG. 4 is a top view thereof;

FIG. 5 is a bottom view thereof;

FIG. 6 is a right side view thereof;

FIG. 7 is a left side view thereof;

FIG. 8 is a sectional view thereof along line 8—8 of FIG. 4;

FIG. 9 is a sectional view thereof along line 9—9 of FIG. 4;

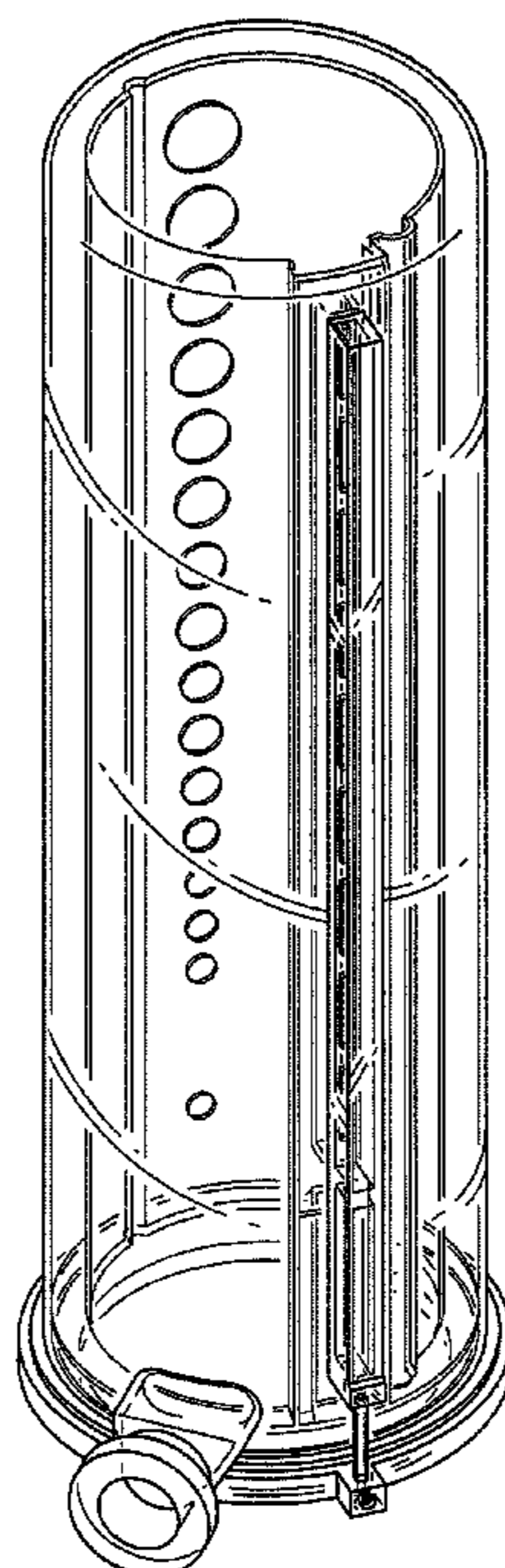
FIG. 10 is a sectional view thereof along line 10—10 of FIG. 4; and,

FIG. 11 is a sectional view thereof along line 11—11 of FIG. 2.

The broken lines are shown for illustrative purpose only and form no part of the claimed design.

* cited by examiner

1 Claim, 11 Drawing Sheets



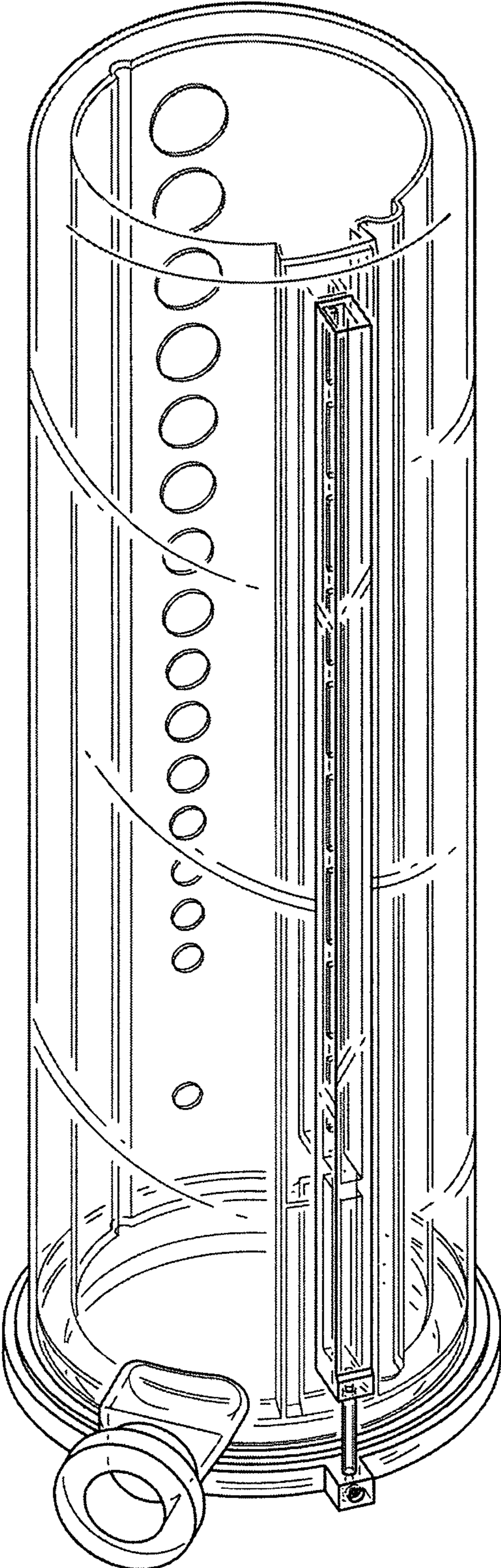


FIG. 1

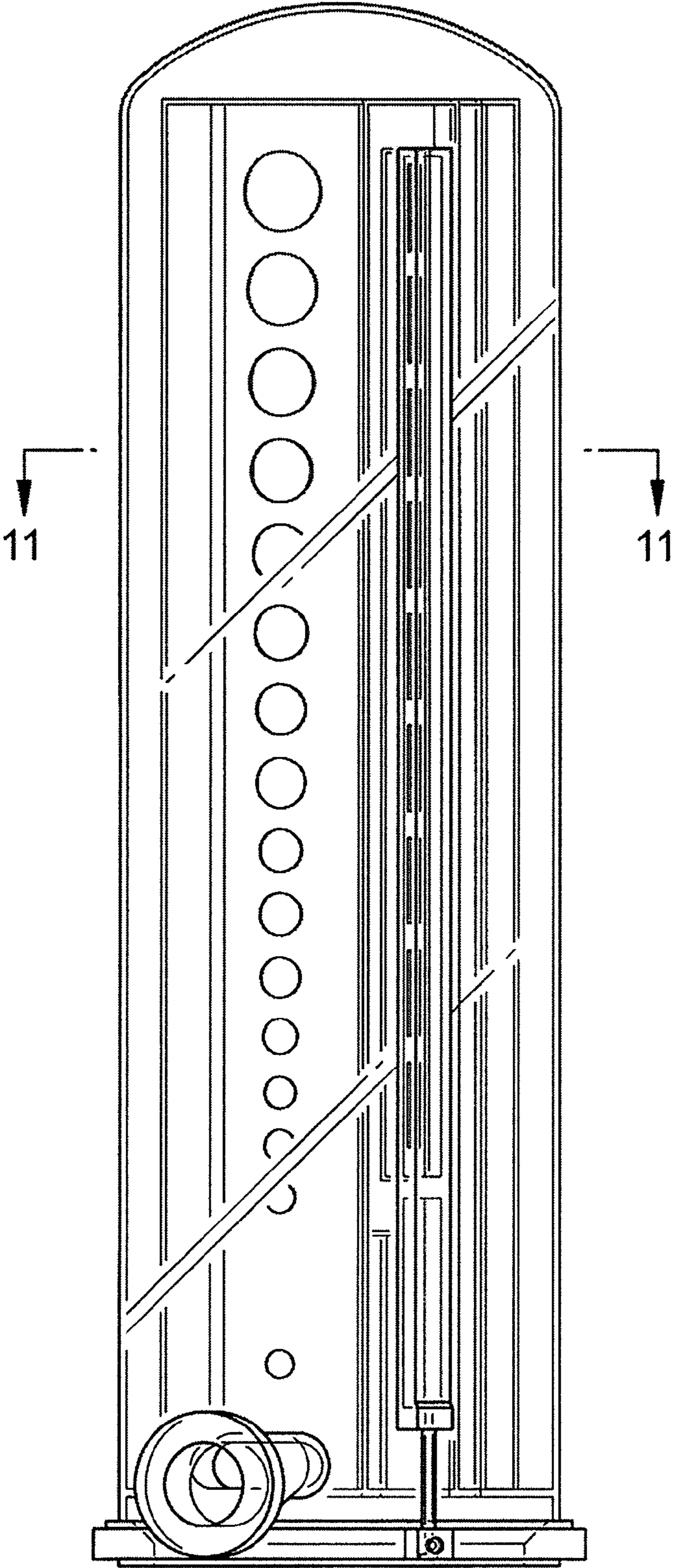


FIG. 2

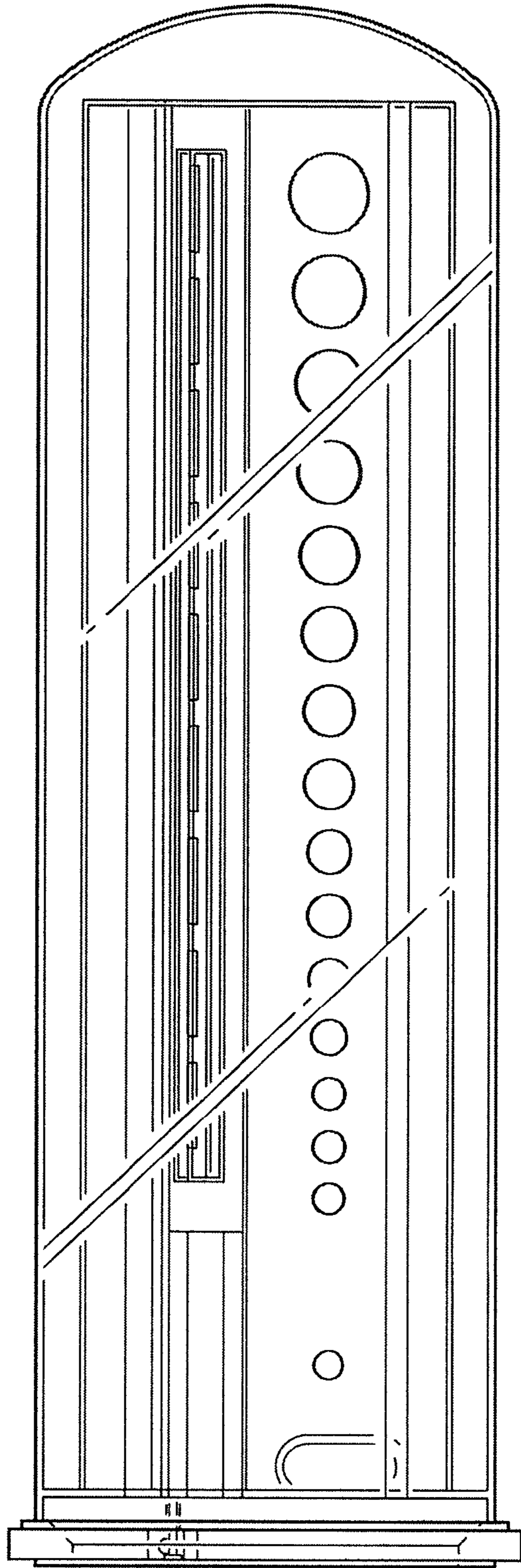


FIG. 3

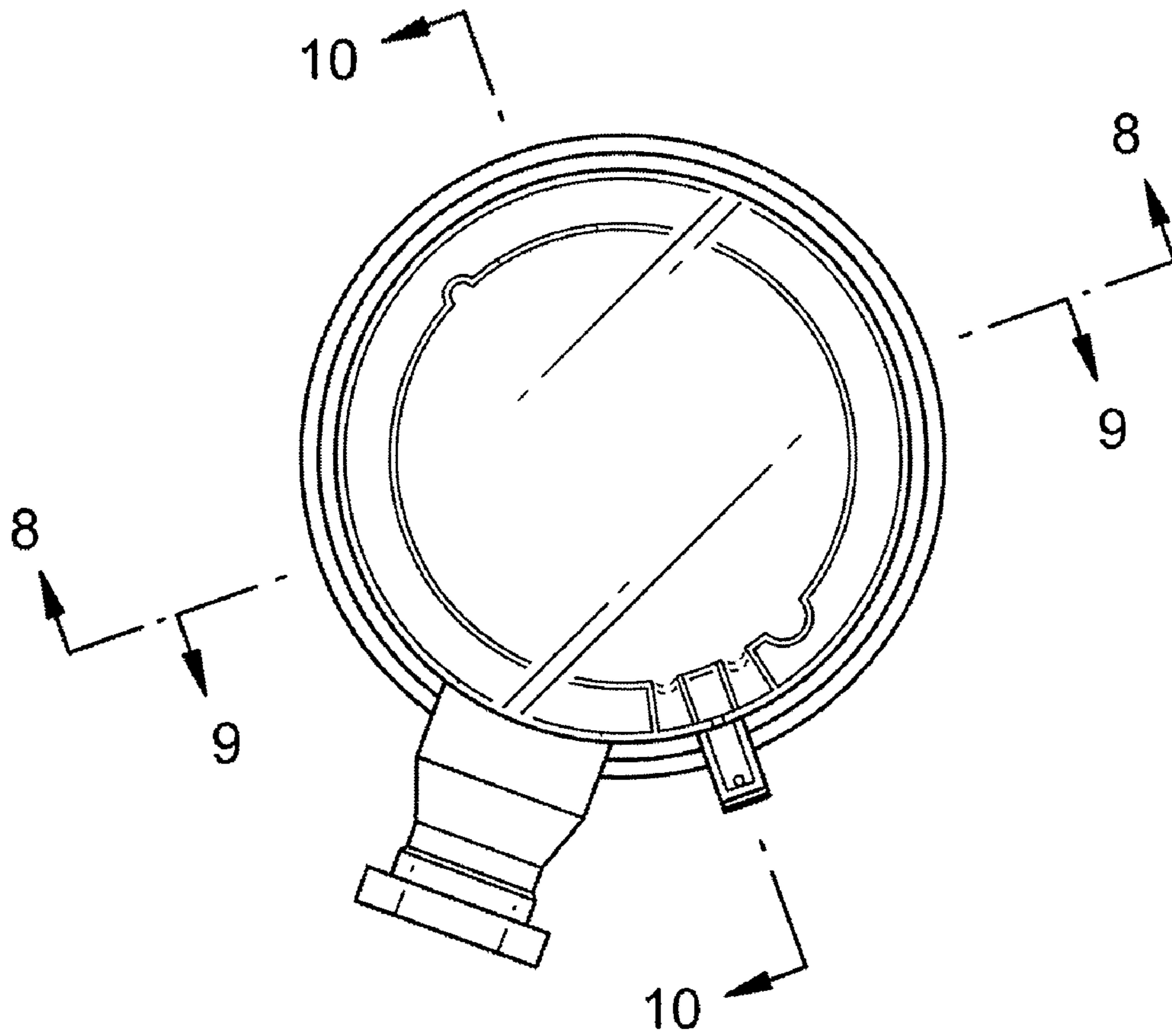


FIG. 4

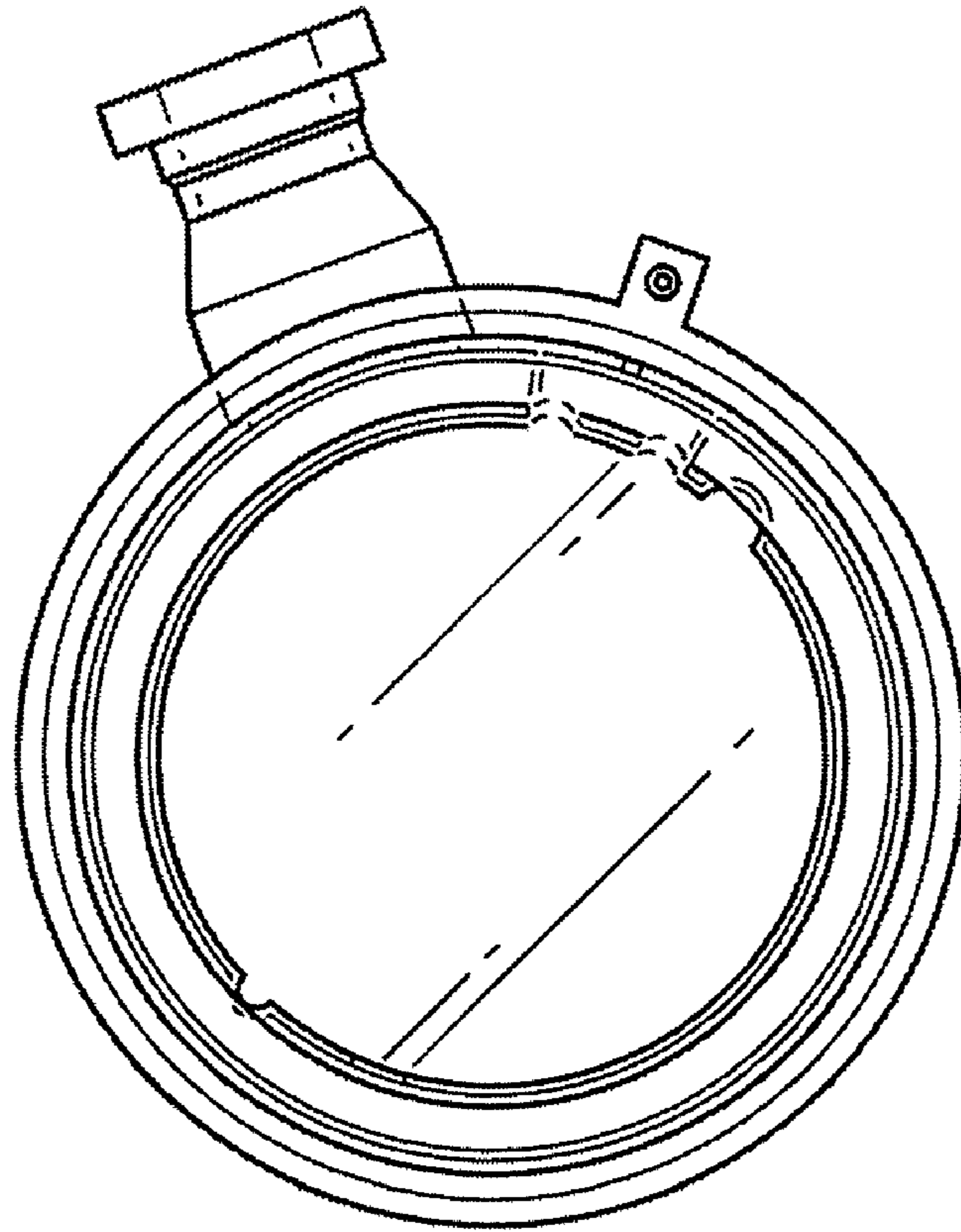


FIG. 5

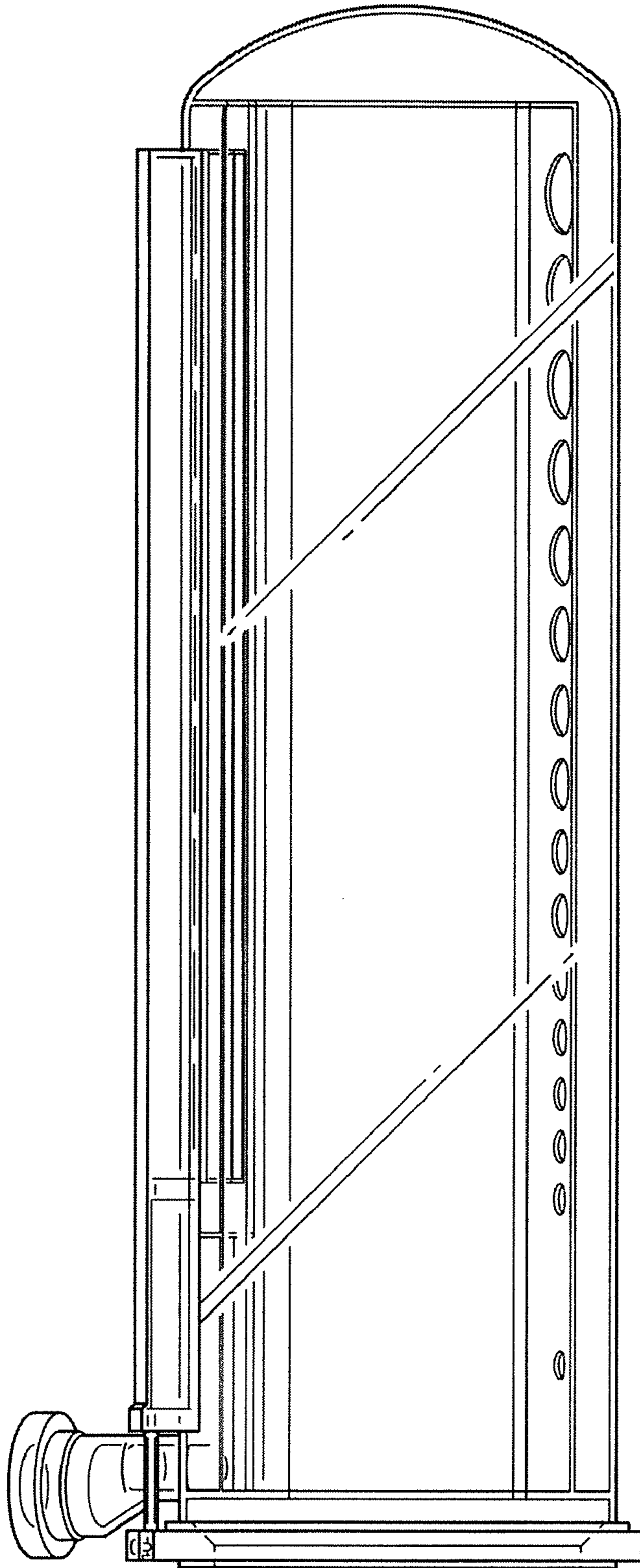


FIG. 6

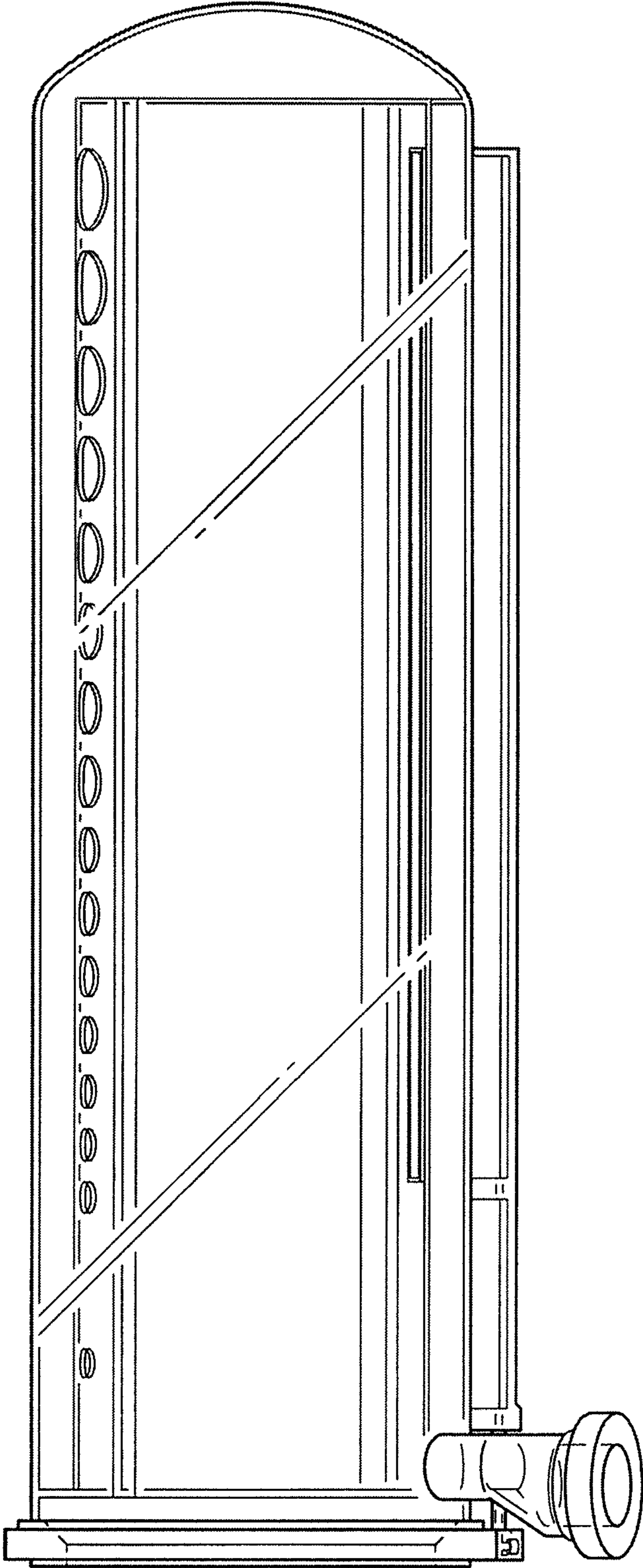


FIG. 7

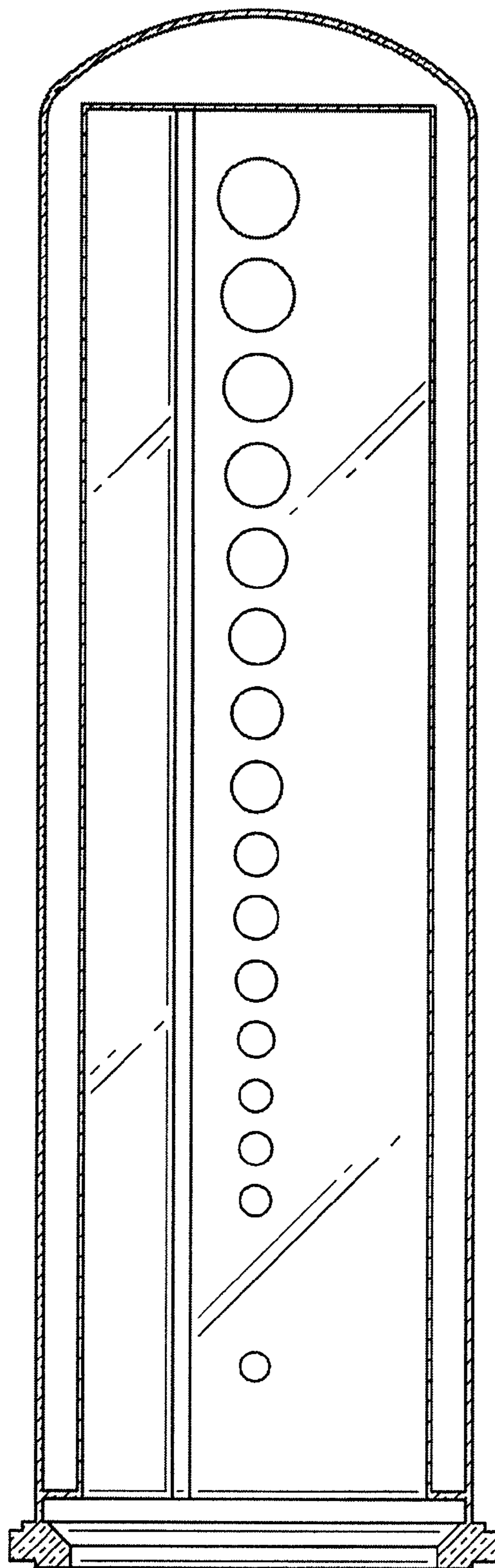


FIG. 8

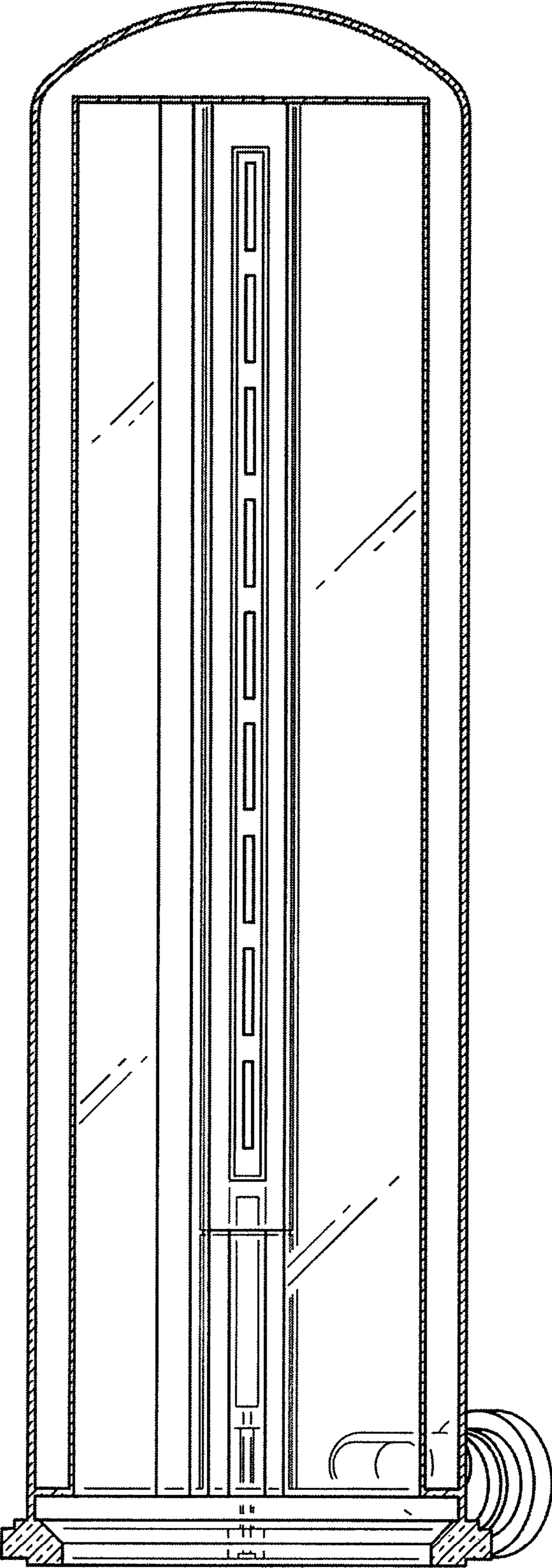


FIG. 9

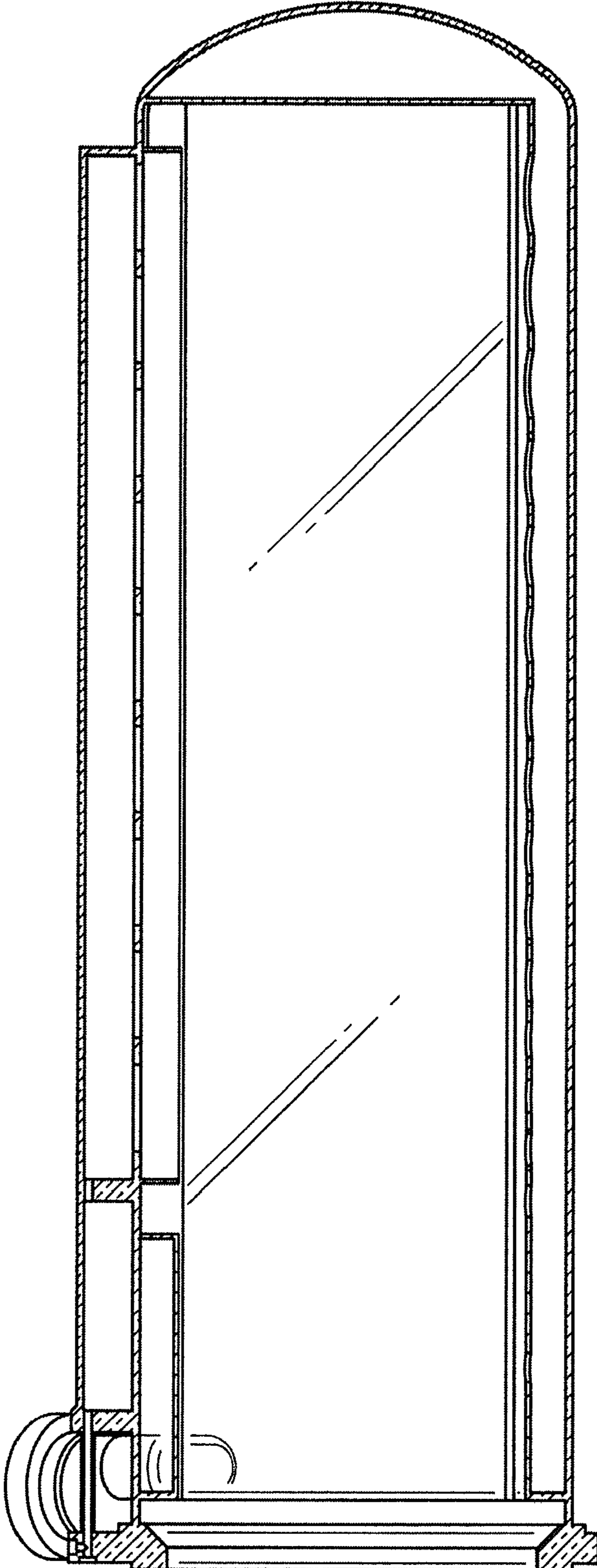


FIG. 10

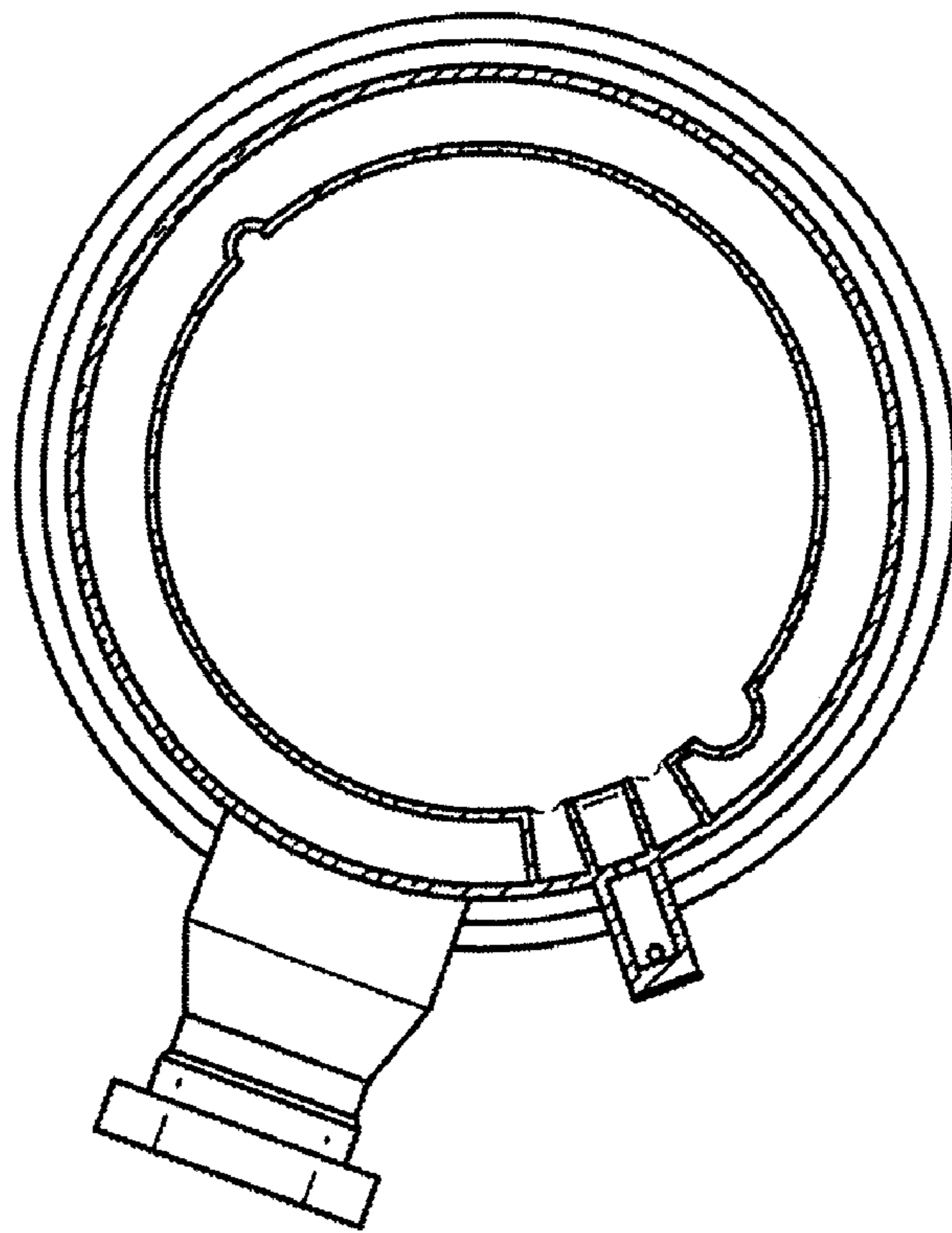


FIG. 11