



US00D600222S

(12) **United States Design Patent**
Sato

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(45) **Date of Patent:** **** Sep. 15, 2009**

(54) **WAFER BOAT**

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(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/309,701**

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(30) **Foreign Application Priority Data**

Mar. 28, 2008 (JP) 2008-007857

(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
D25/113, 118, 136; D21/484, 500, 505;
52/610; 118/728, 729; 211/41.18; 432/241,
432/253, 258

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a wafer boat, as shown and described.

DESCRIPTION

FIG. 1 is a front view;

FIG. 2 is a partial enlarged perspective view of a bottom along 2—2 of the frontal view shown in FIG. 1;

FIG. 3 is an enlarged bottom view;

FIG. 4 is a rear view;

FIG. 5 is a left side view the right side being a mirror image thereof;

FIG. 6 is a plan view;

FIG. 7 is a bottom view; and,

FIG. 8 is a partial, enlarged view, along 2—2 of a front view shown in FIG. 1 of the wafer boat in use.

Salients are formed on a bottom board of a wafer boat to get into reentrants of a heat insulating cylinder for manufacturing a semiconductor wafer, and stabilize it in a setting condition. The portion shown in solid lines is my claimed design. The broken line showing in the figures is for illustrative purposes only and forms no part of the claimed design.

1 Claim, 8 Drawing Sheets

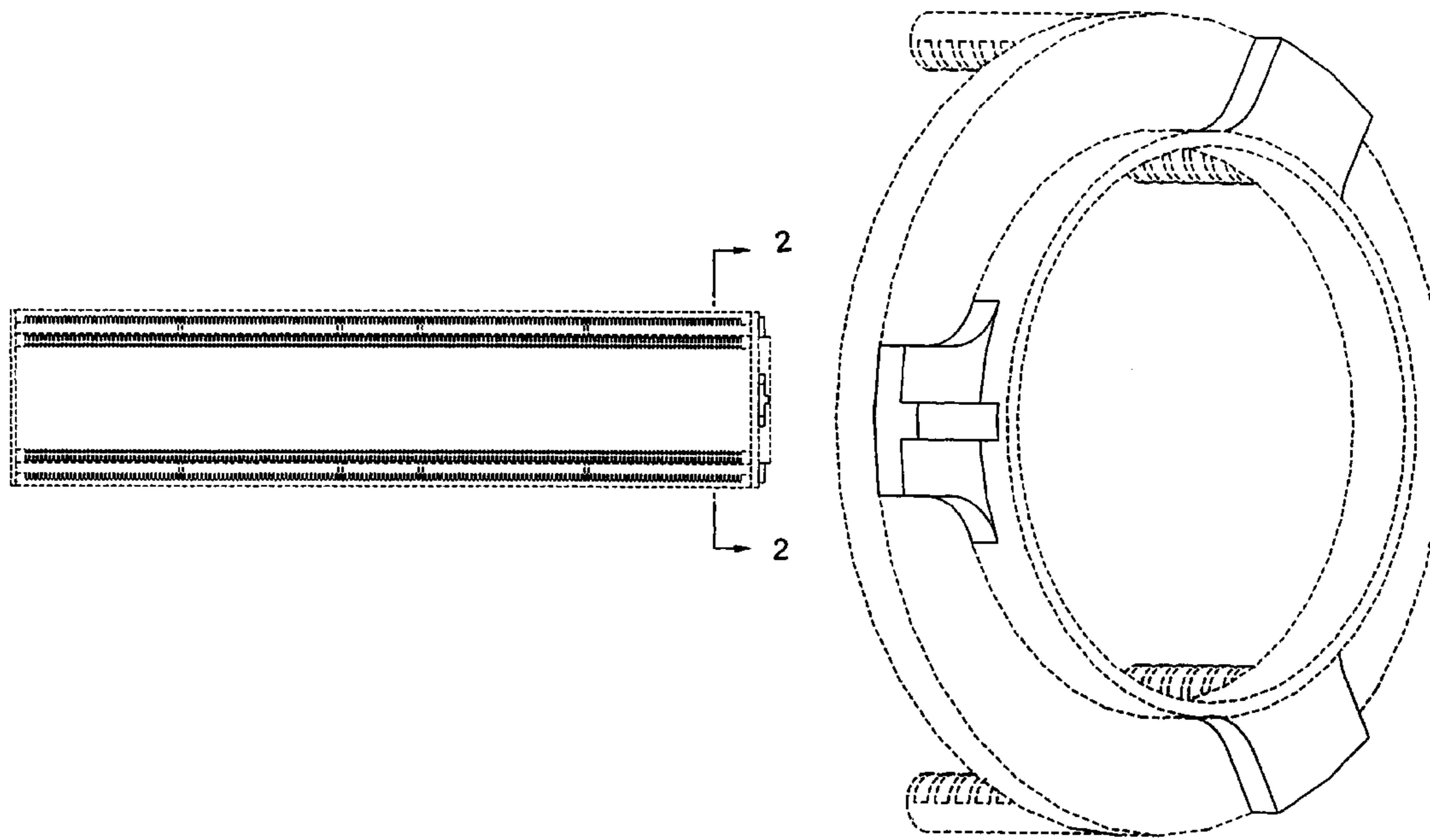


FIGURE 1

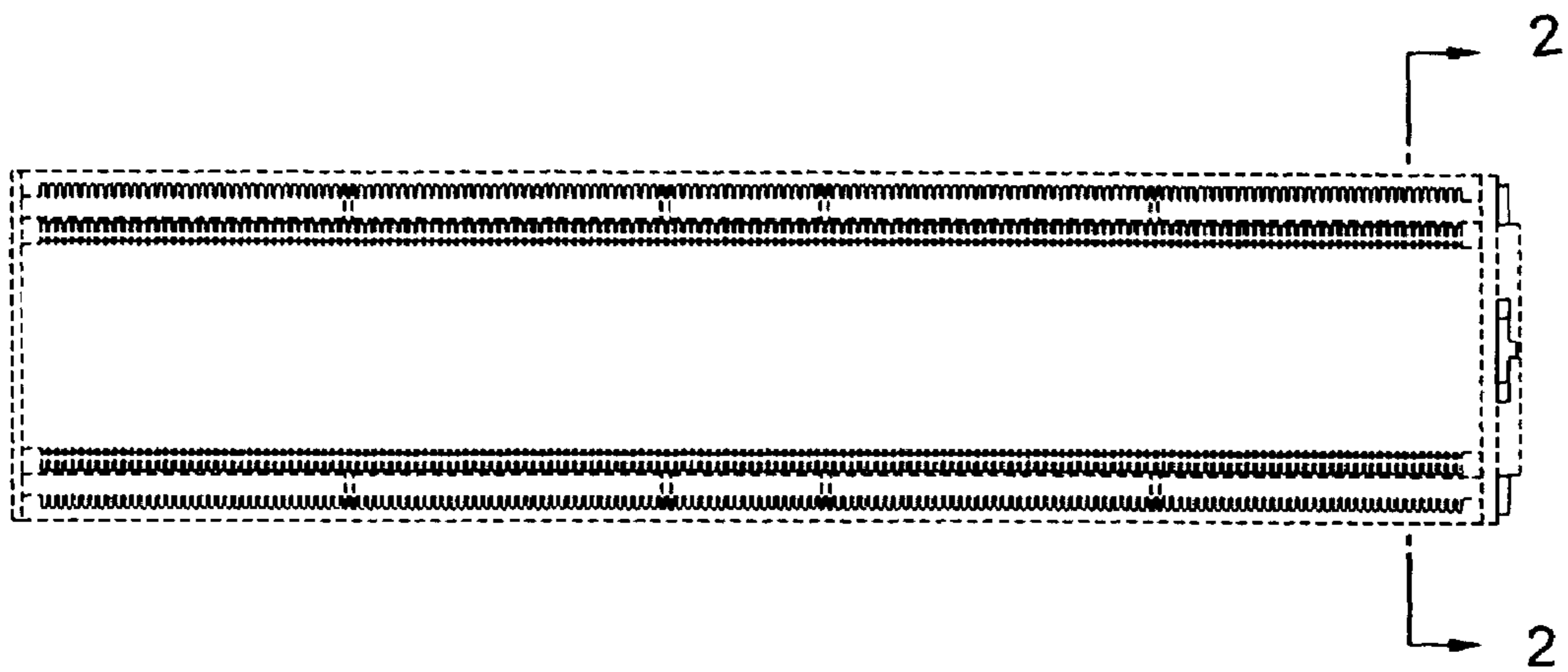


FIGURE 2

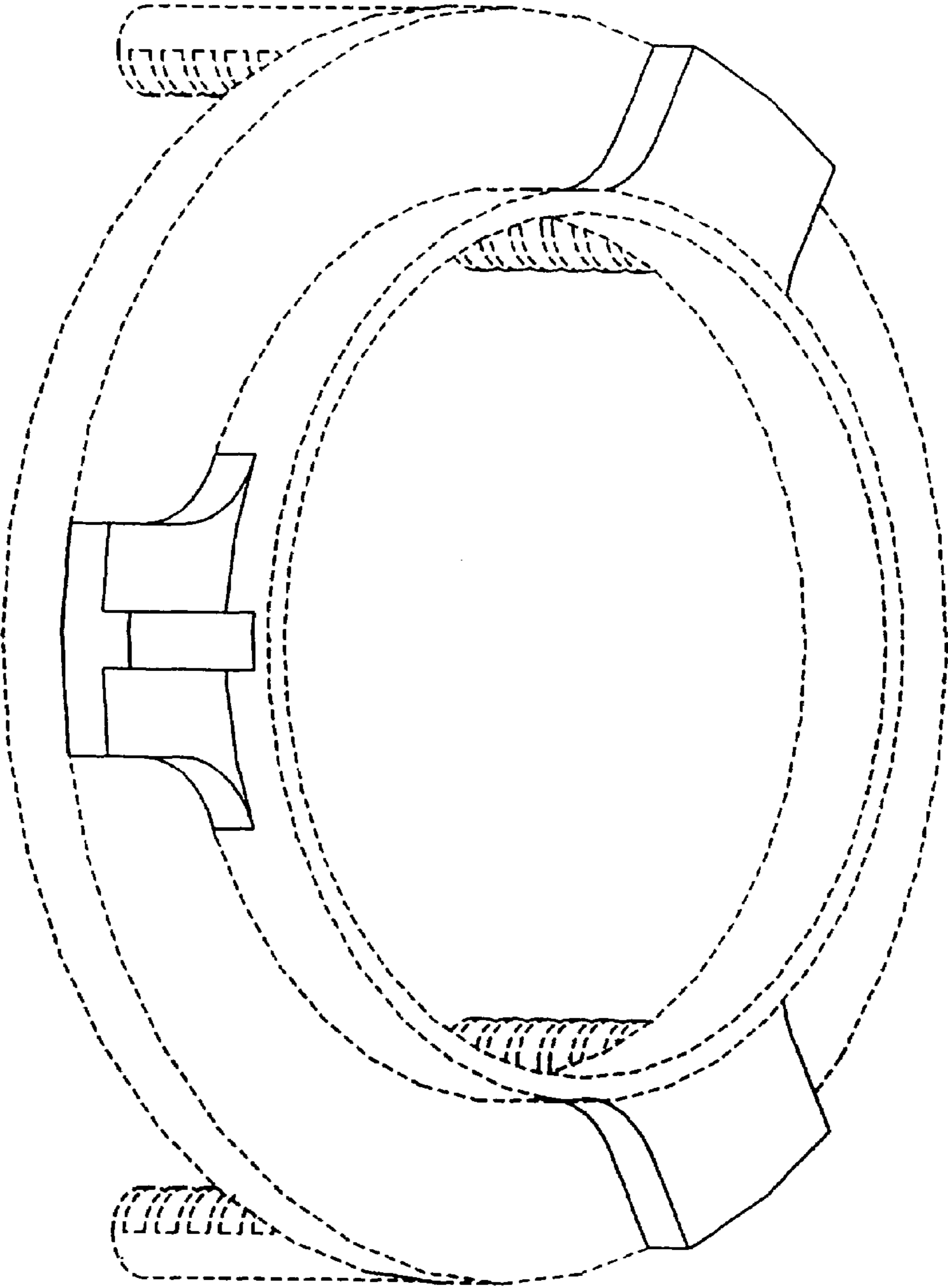


FIGURE 3

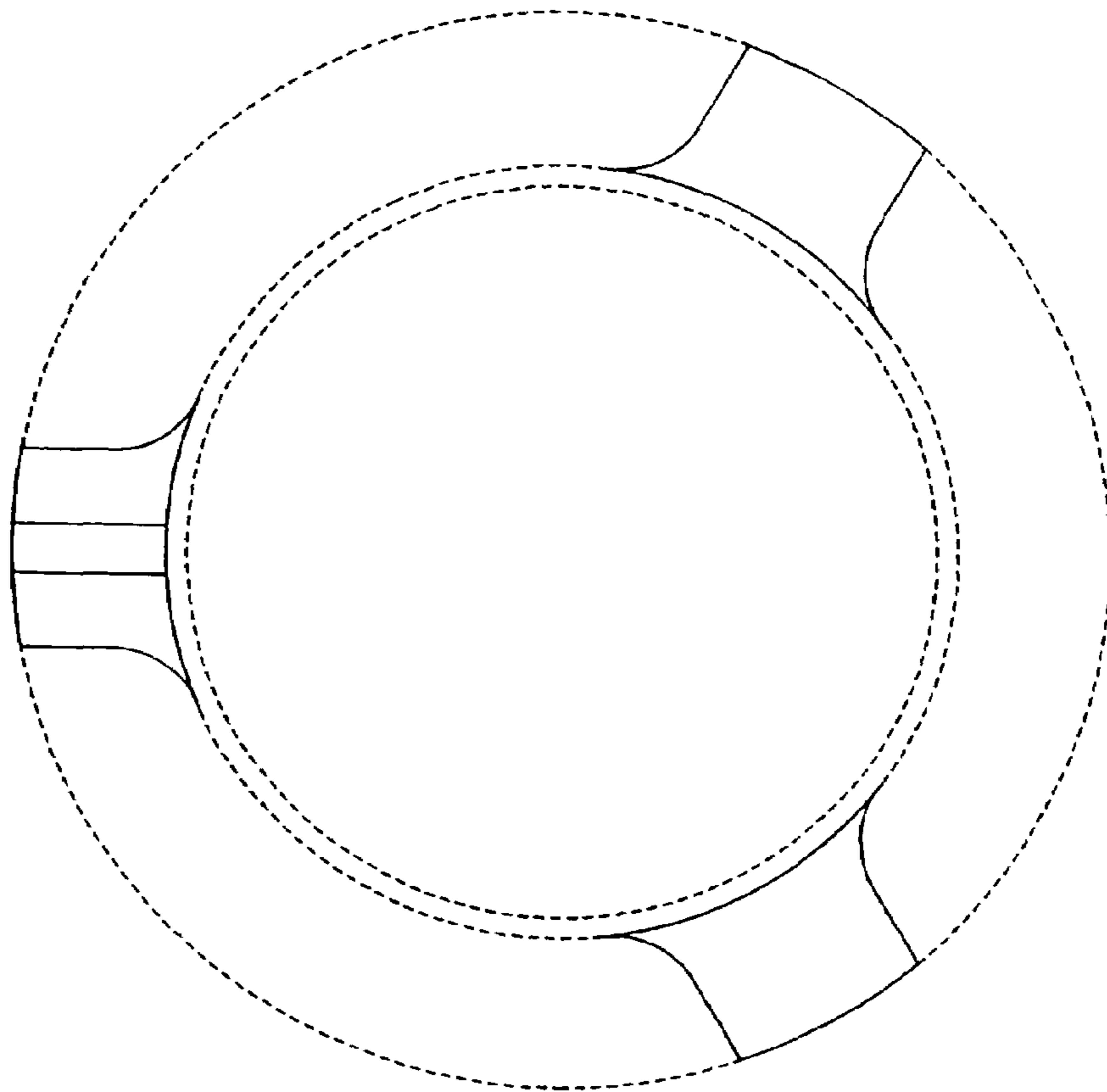


FIGURE 4

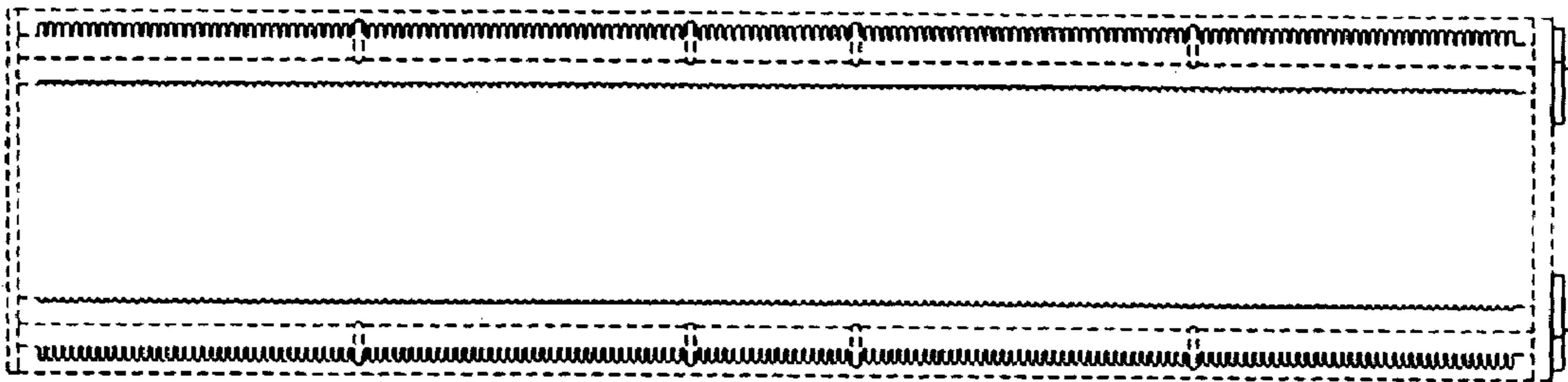


FIGURE 5

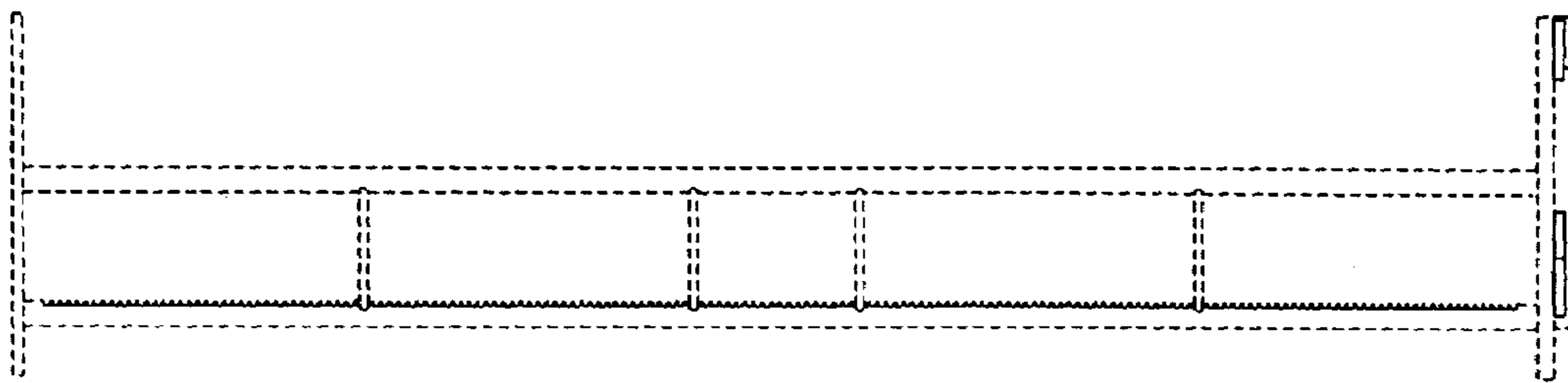


FIGURE 6

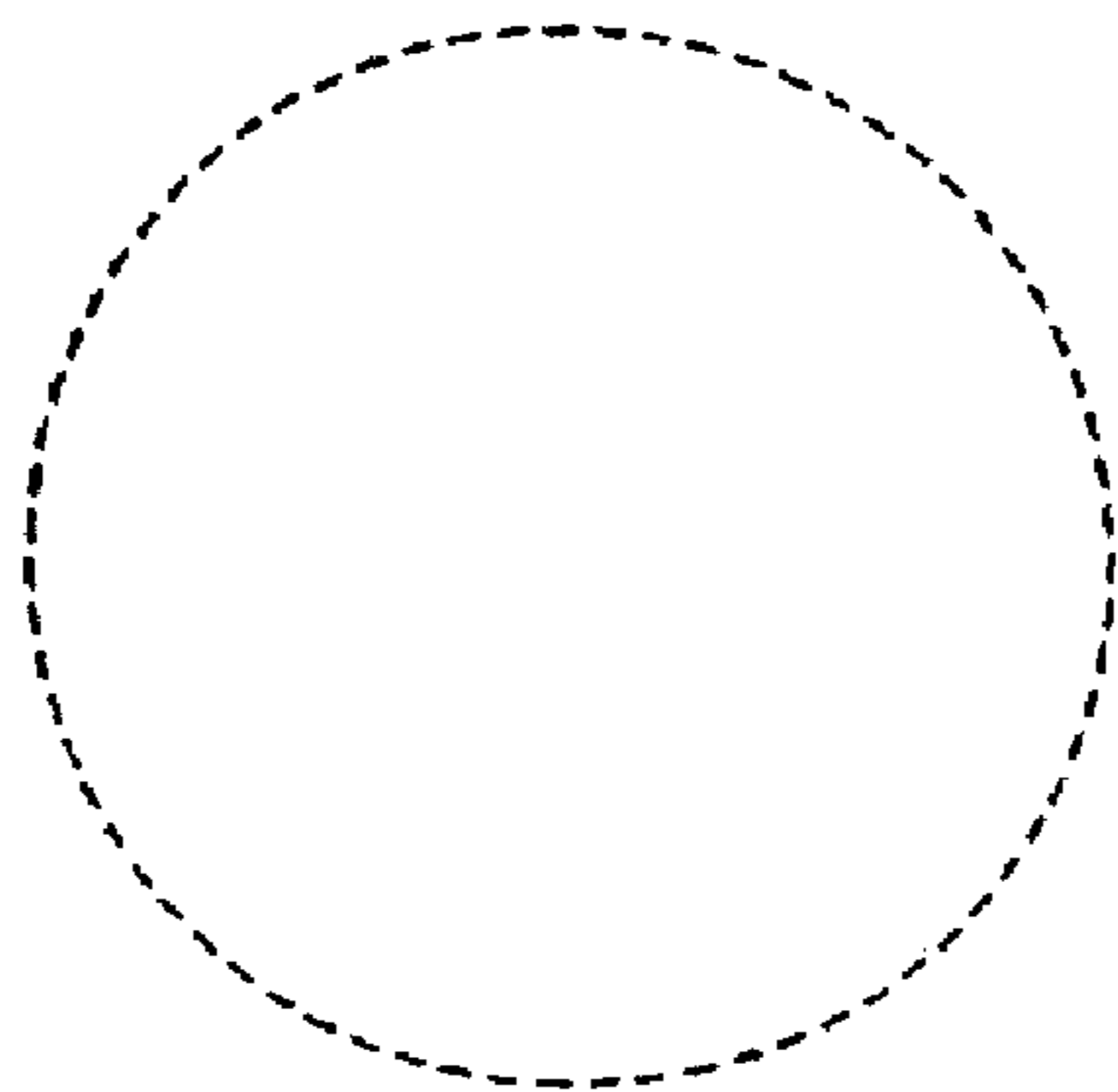


FIGURE 7

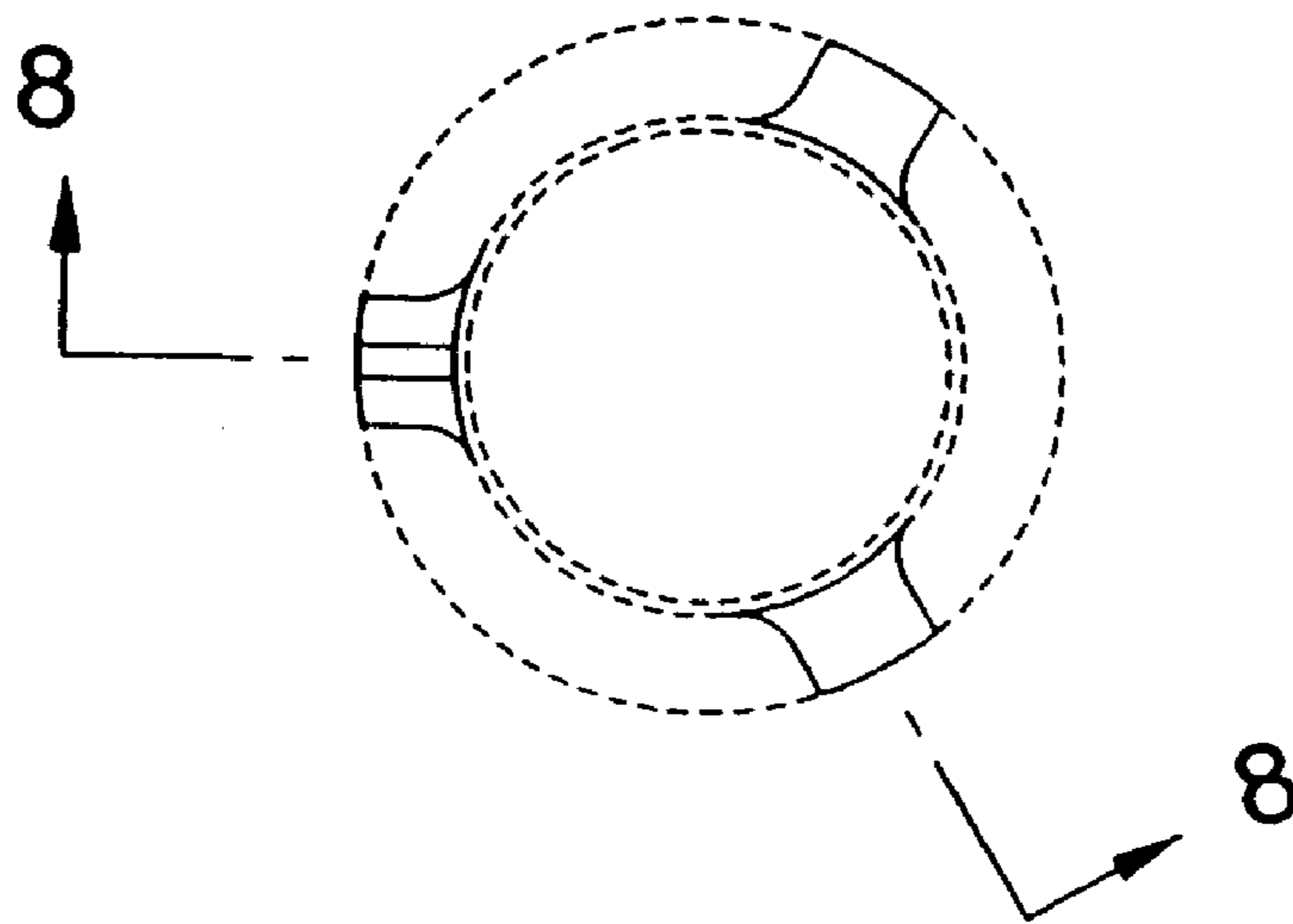


FIG. 8

