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(12) **United States Design Patent**
Nada et al.

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(45) **Date of Patent:** **** Aug. 25, 2009**

(54) **PROGRAMMABLE LOGIC CONTROLLER**

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(JP)

(73) Assignee: **OMRON Corporation**, Kyoto (JP)

(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**

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Apr. 18, 2008	(JP)	2008-010035
Apr. 18, 2008	(JP)	2008-010036

(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.** **D13/162.1; D13/178; D13/184**

(58) **Field of Classification Search** D13/158,
D13/159, 160, 162, 162.1, 178, 184, 199;
361/600, 601, 627, 641, 686, 687, 690, 729,
361/733, 752, 796; 439/259; 700/1, 2, 11,
700/23

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a programmable logic controller,
as shown and described.

DESCRIPTION

FIG. 1 is a front, top and right side perspective view of an
embodiment of a programmable logic controller showing our
new design;

FIG. 2 is a front, bottom and left side perspective view
thereof;

FIG. 3 is a front elevational view thereof;

FIG. 4 is a top plan view thereof;

FIG. 5 is a bottom plan view thereof;

FIG. 6 is a right side elevational view thereof;

FIG. 7 is a left side elevational view thereof;

FIG. 8 is a front, top and right side perspective view showing
a condition in which all covers are removed thereof;

FIG. 9 is a front elevational view showing a condition in
which all covers are removed thereof;

FIG. 10 is an enlarged rear perspective view of a removed
media slot cover thereof; and,

FIG. 11 is an enlarged rear perspective view of a removed
cable connector cover thereof.

The broken lines are shown in the figures for illustrative
purposes only and form no part of the claimed design.

1 Claim, 9 Drawing Sheets

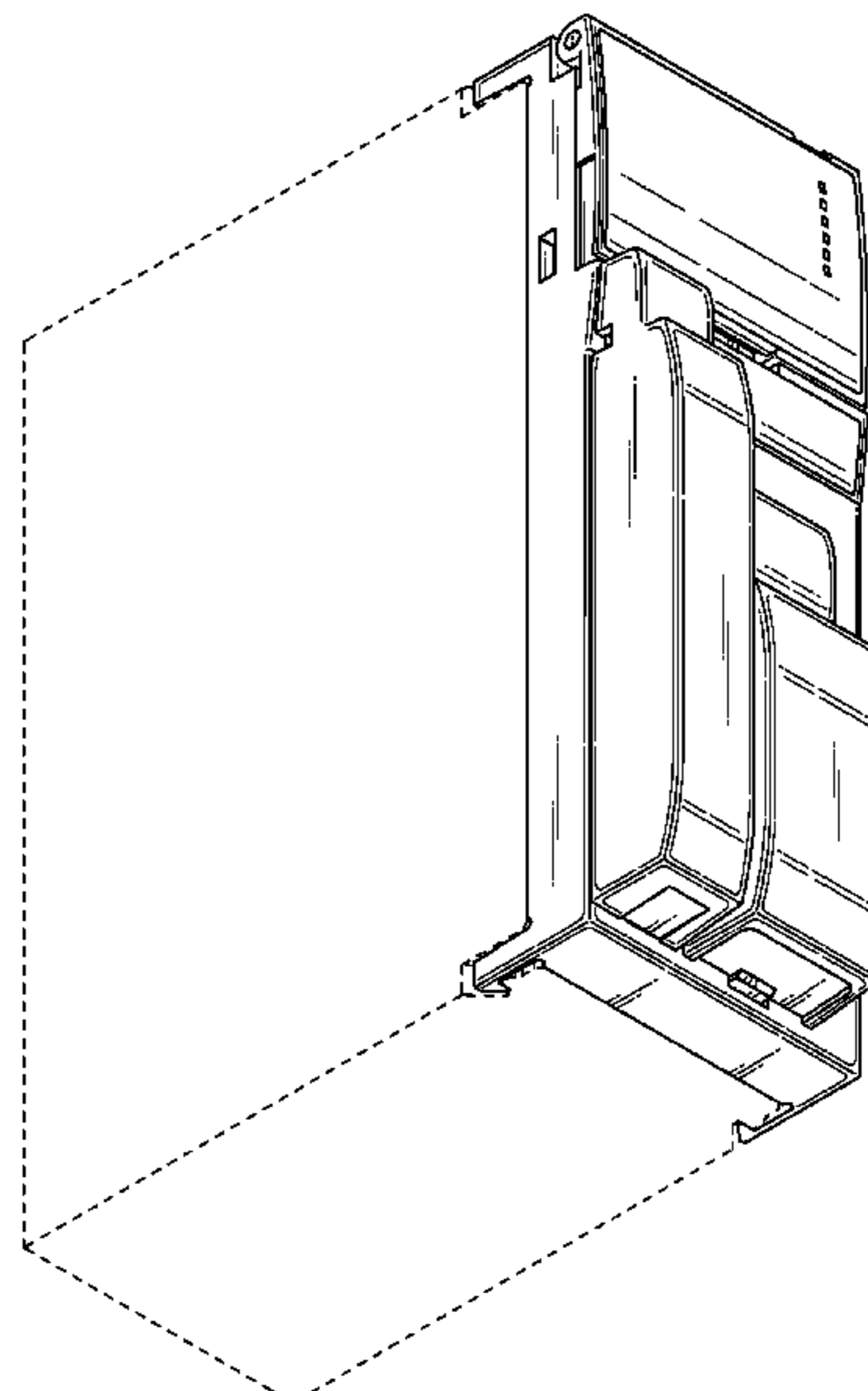
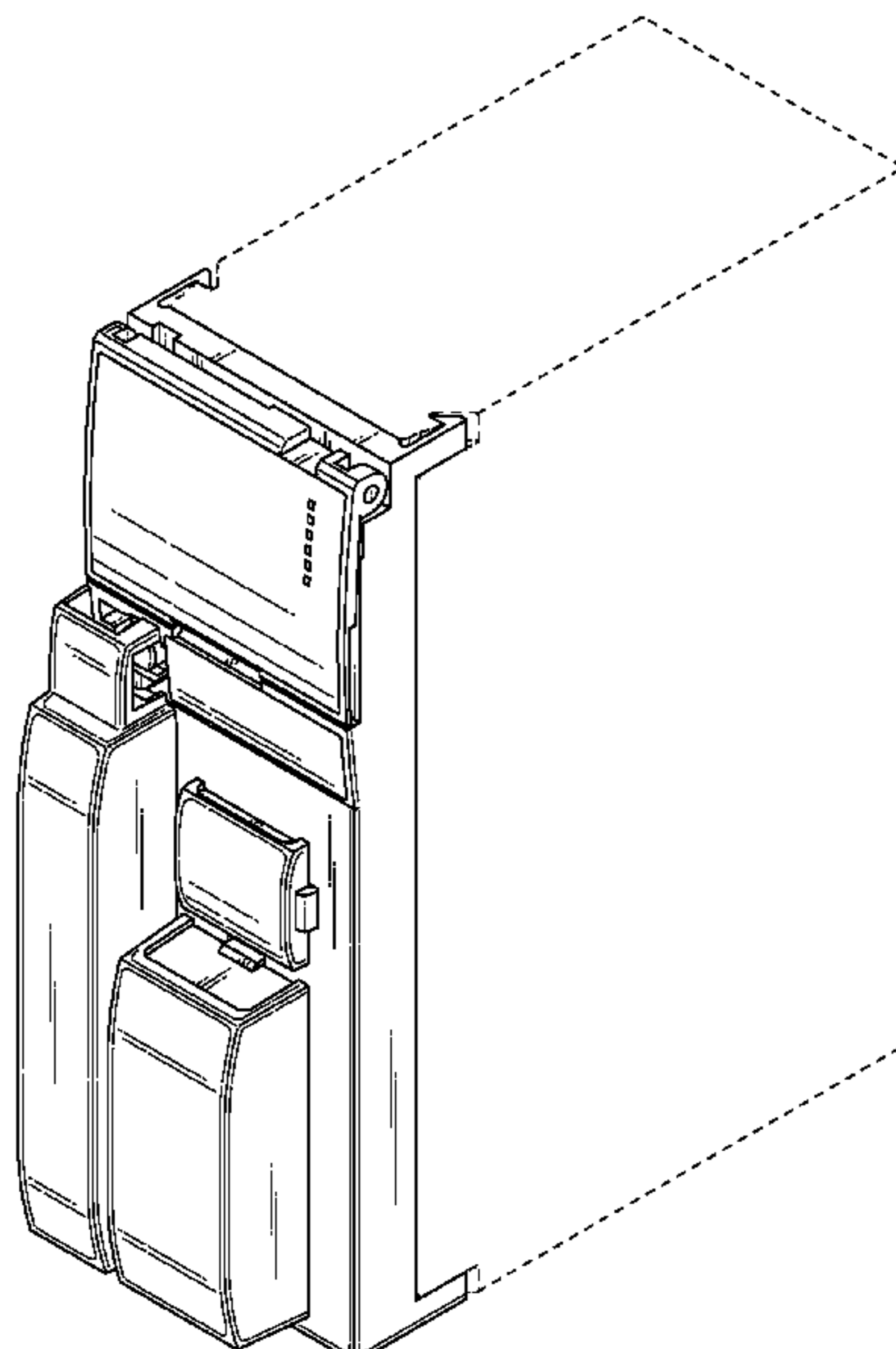


FIG. 1

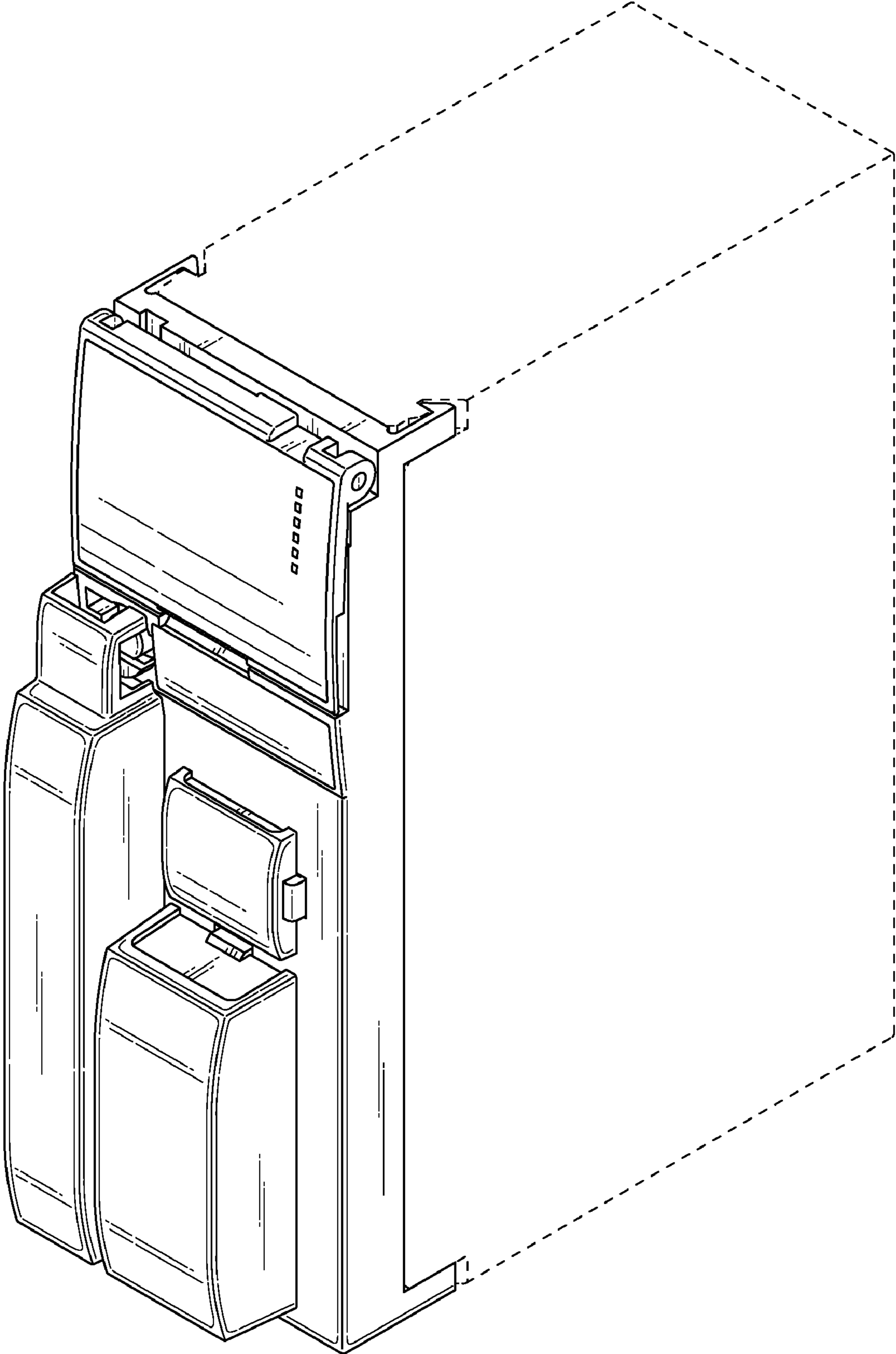


FIG. 2

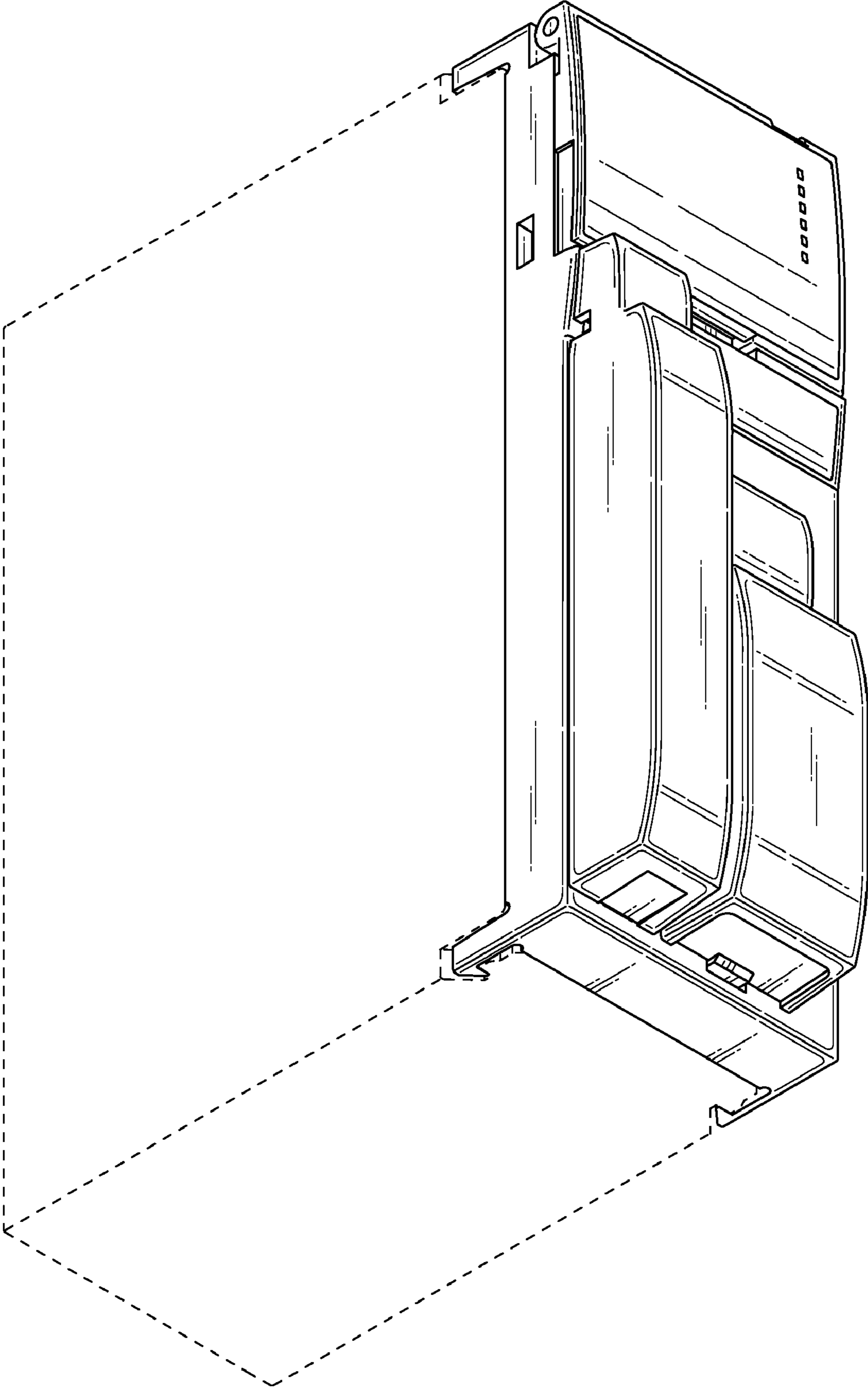


FIG. 3

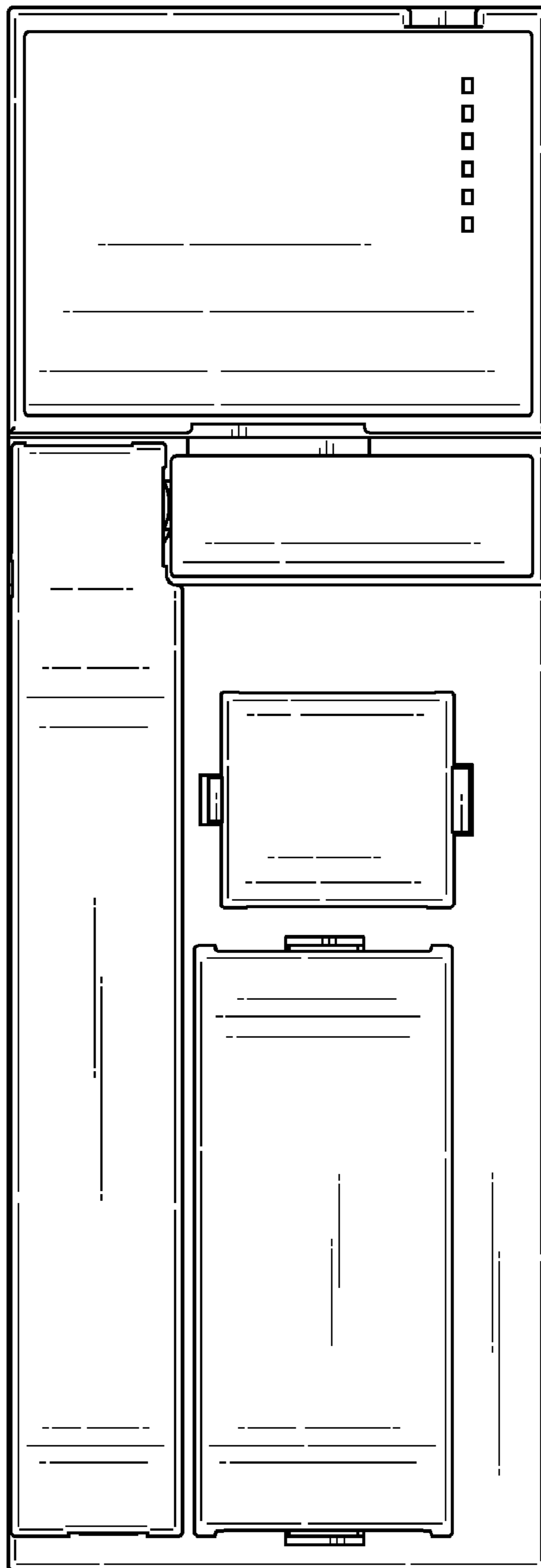


Fig.4

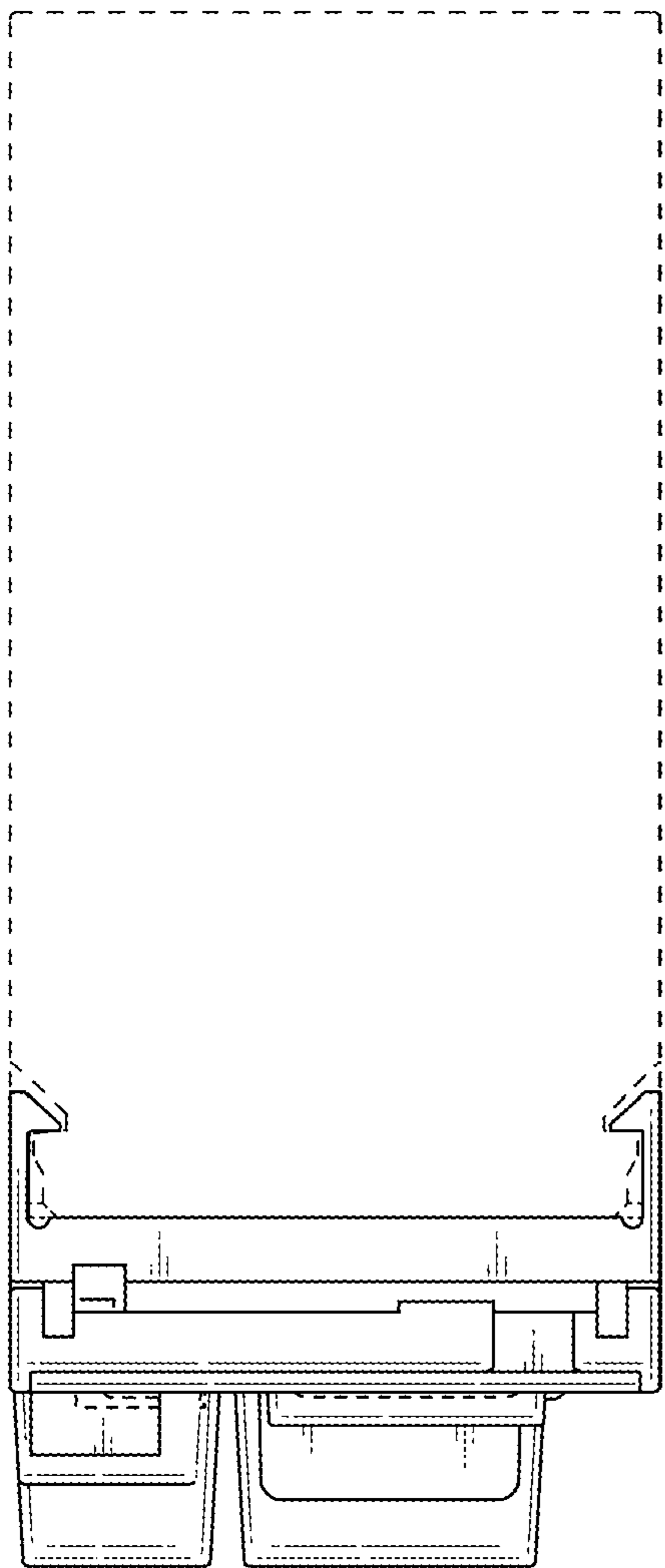


Fig. 5

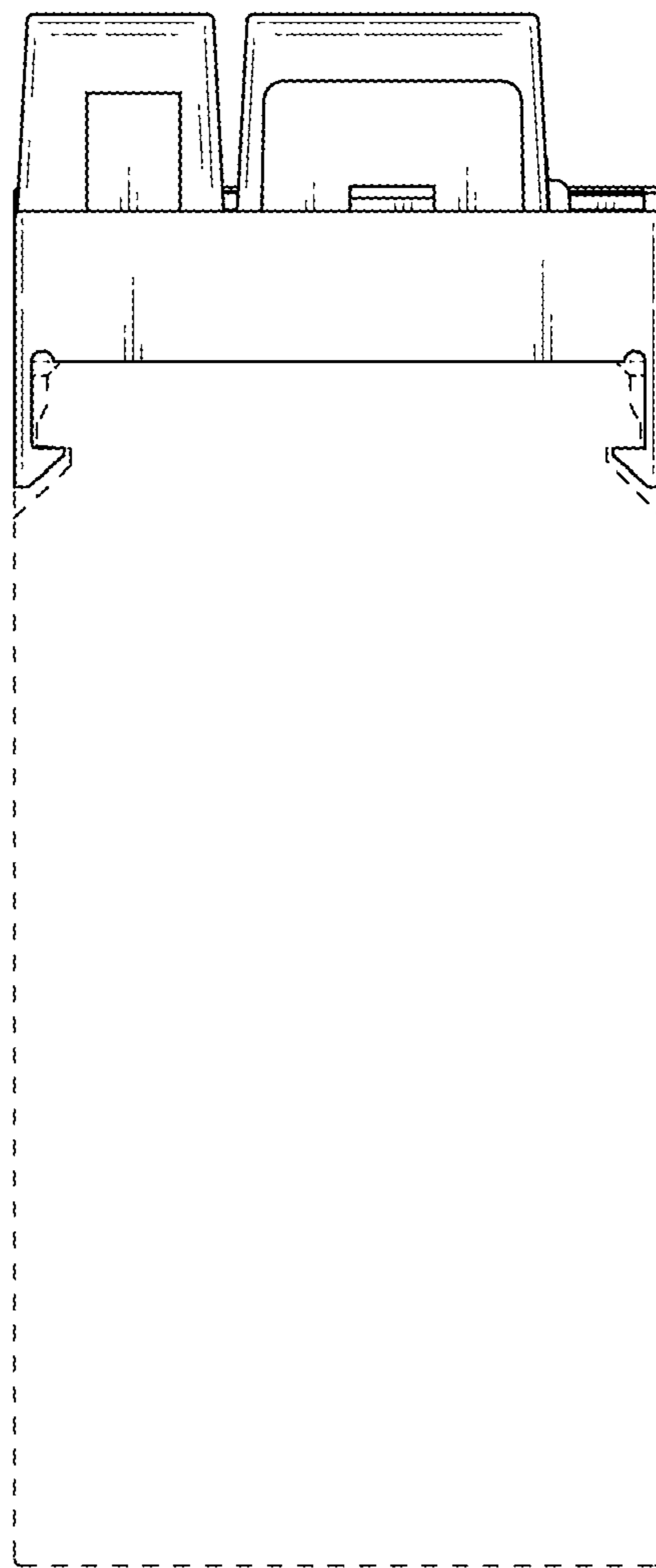


FIG. 6

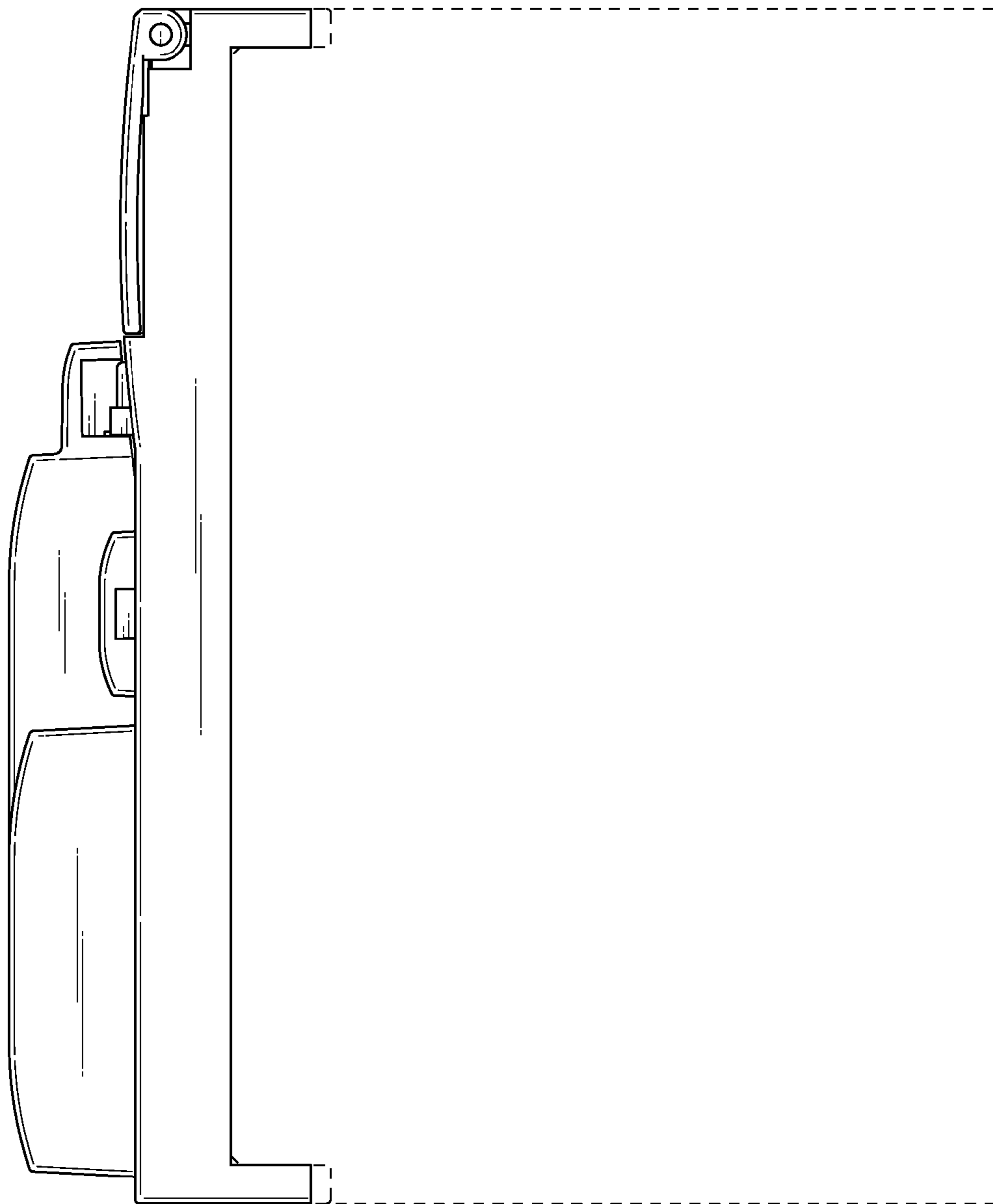


Fig.7

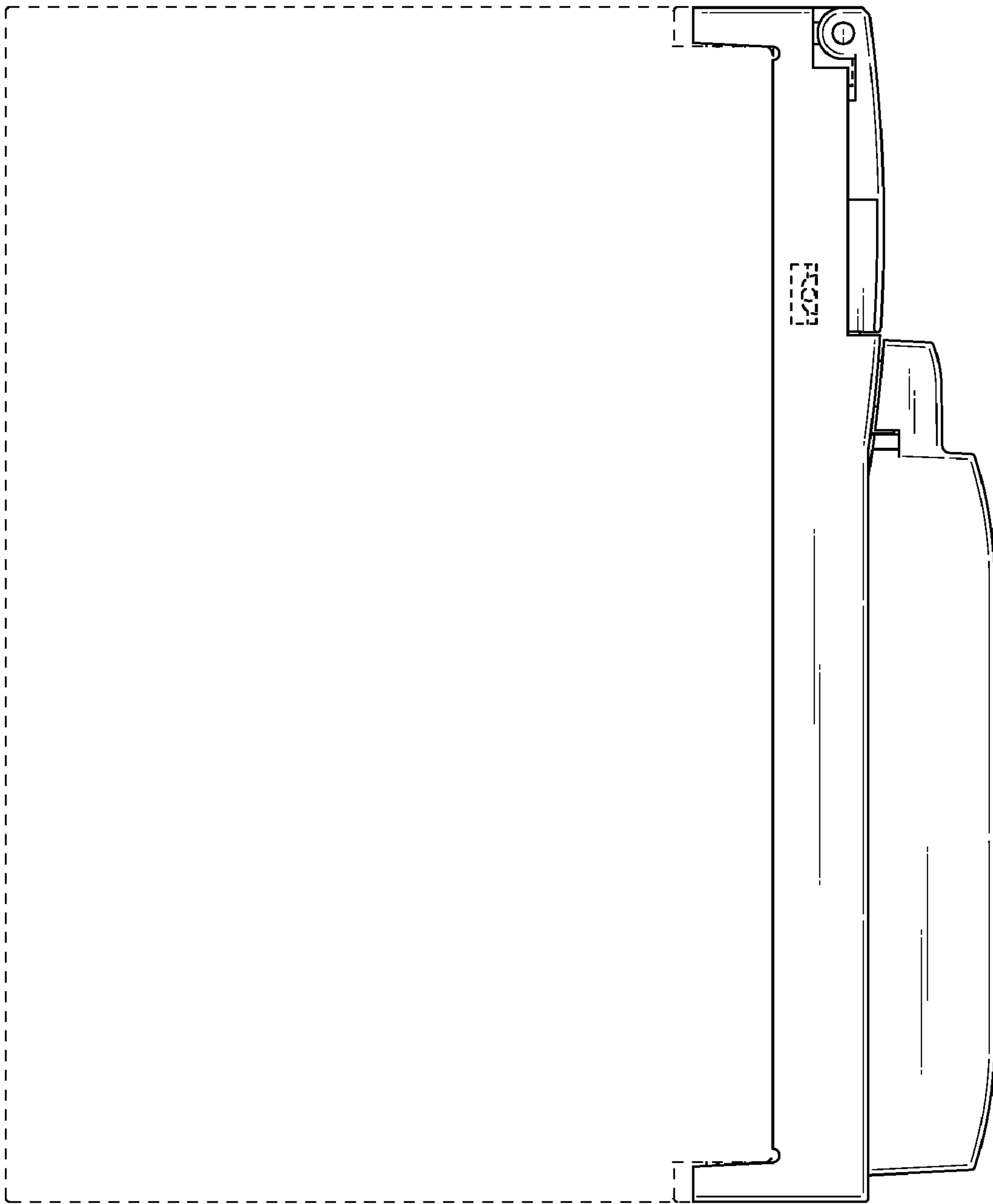


FIG. 8

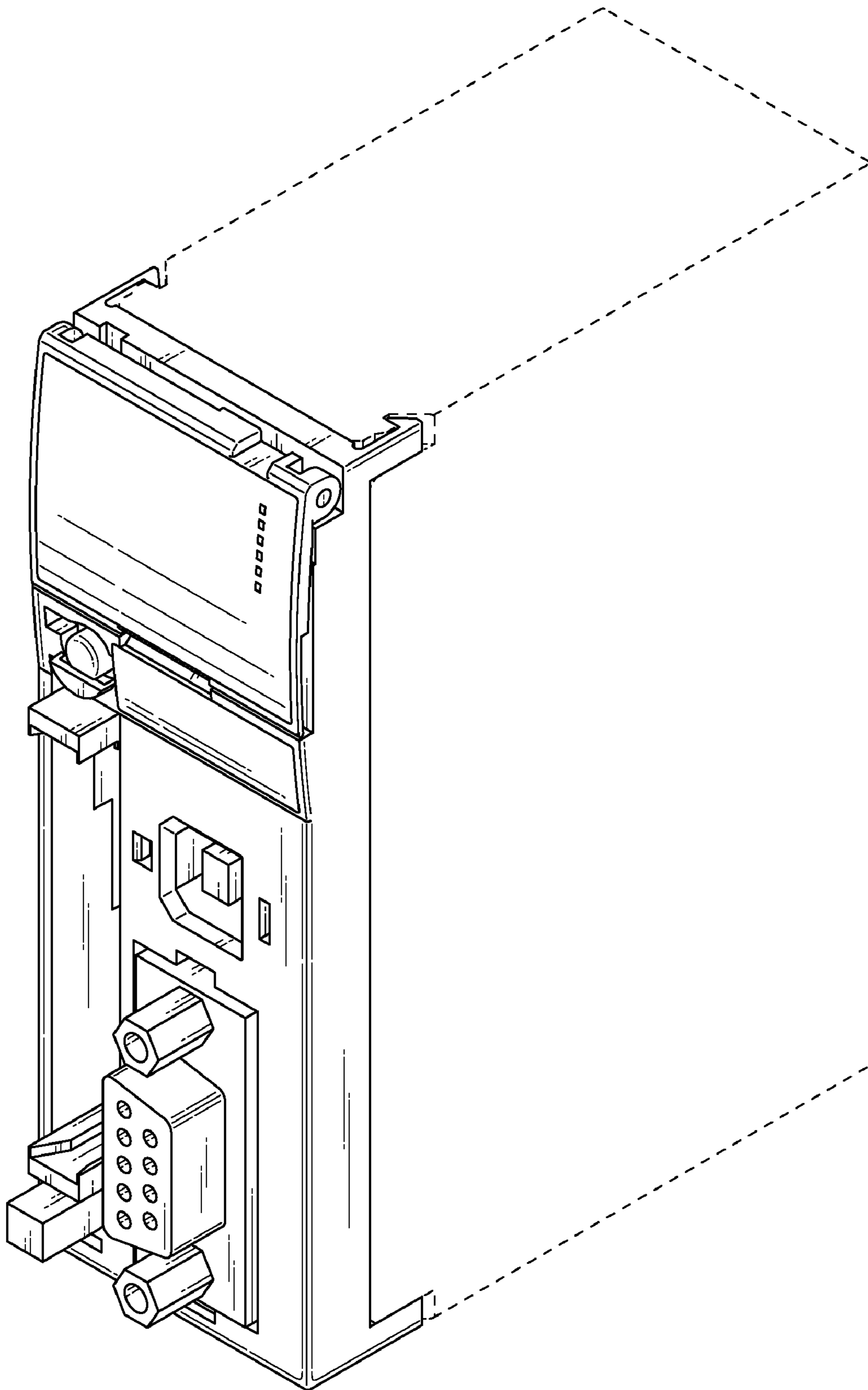


Fig.9

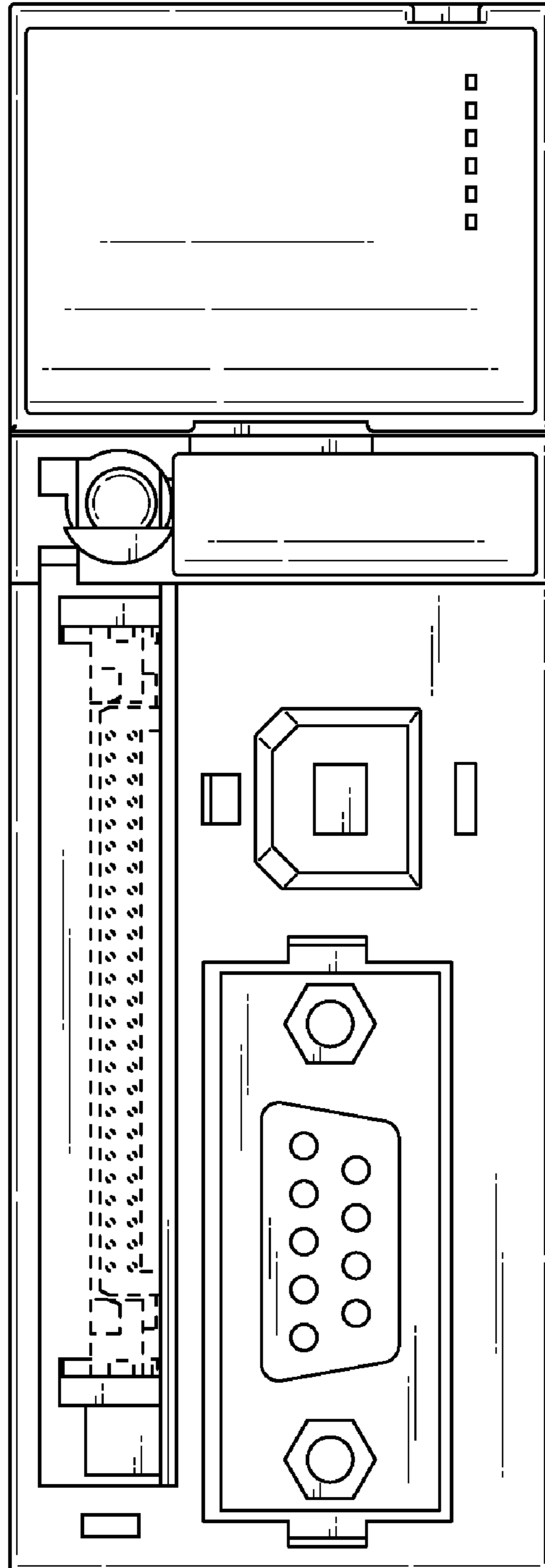


FIG. 10

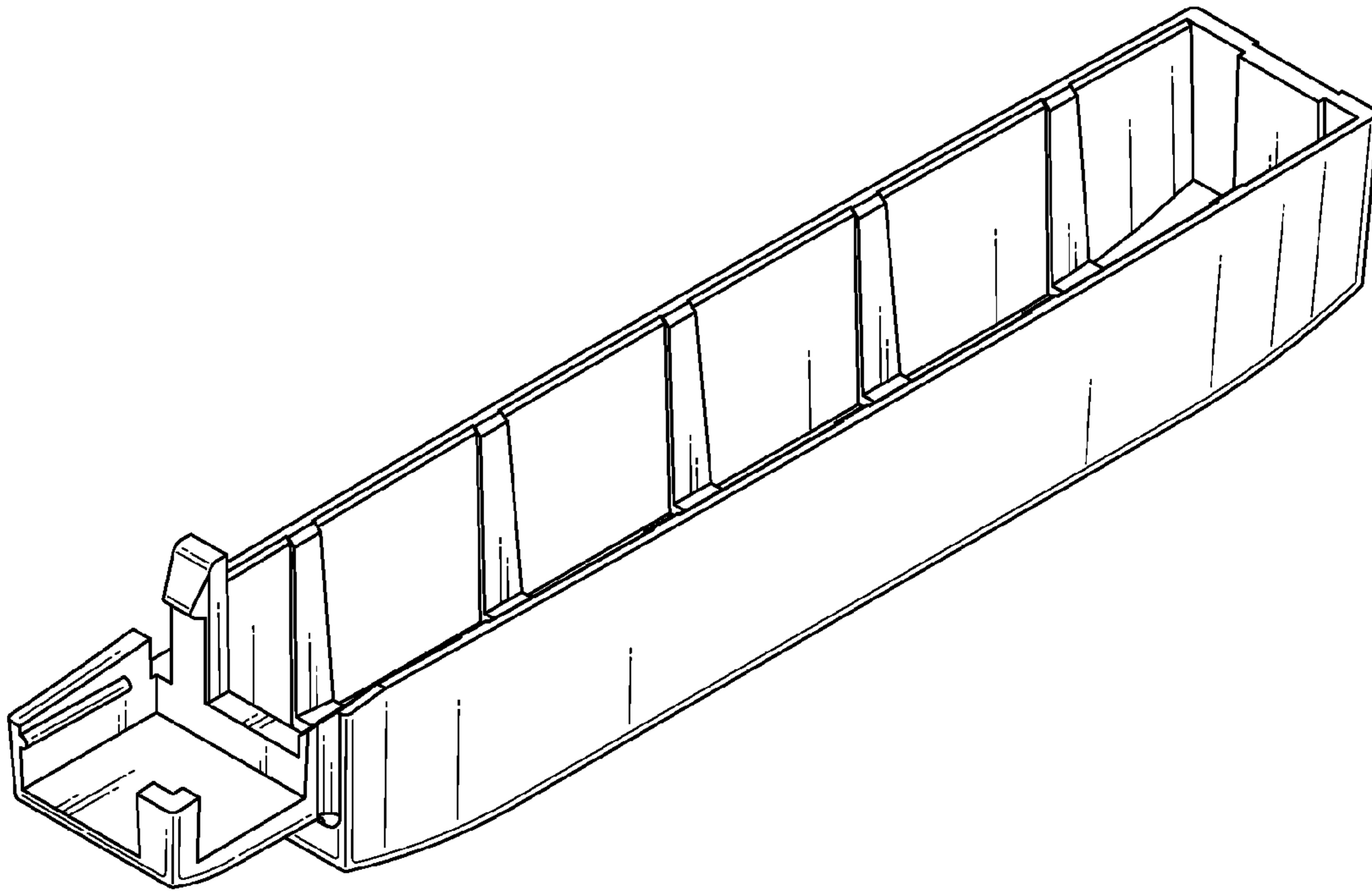


FIG. 11

