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(12) **United States Design Patent**
Kobayashi et al.

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(54) **PORTION OF A PRINTED CIRCUIT BOARD**

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(73) Assignee: **Kabushiki Kaisha Toshiba**, Tokyo (JP)

(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**

Nov. 30, 2006 (JP) 2006-033055

(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
29/829; 361/720, 749, 760, 776, 820; 174/250,
174/253, 255

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a portion of a printed circuit board, as shown and described.

DESCRIPTION

FIG. 1 is a front, bottom and right side perspective view of a portion of a printed circuit board, showing our new design;

FIG. 2 is a front elevational view thereof;

FIG. 3 is a rear elevational view thereof;

FIG. 4 is a top plan view thereof;

FIG. 5 is a bottom plan view thereof;

FIG. 6 is a right side elevational view thereof;

FIG. 7 is a left side elevational view thereof;

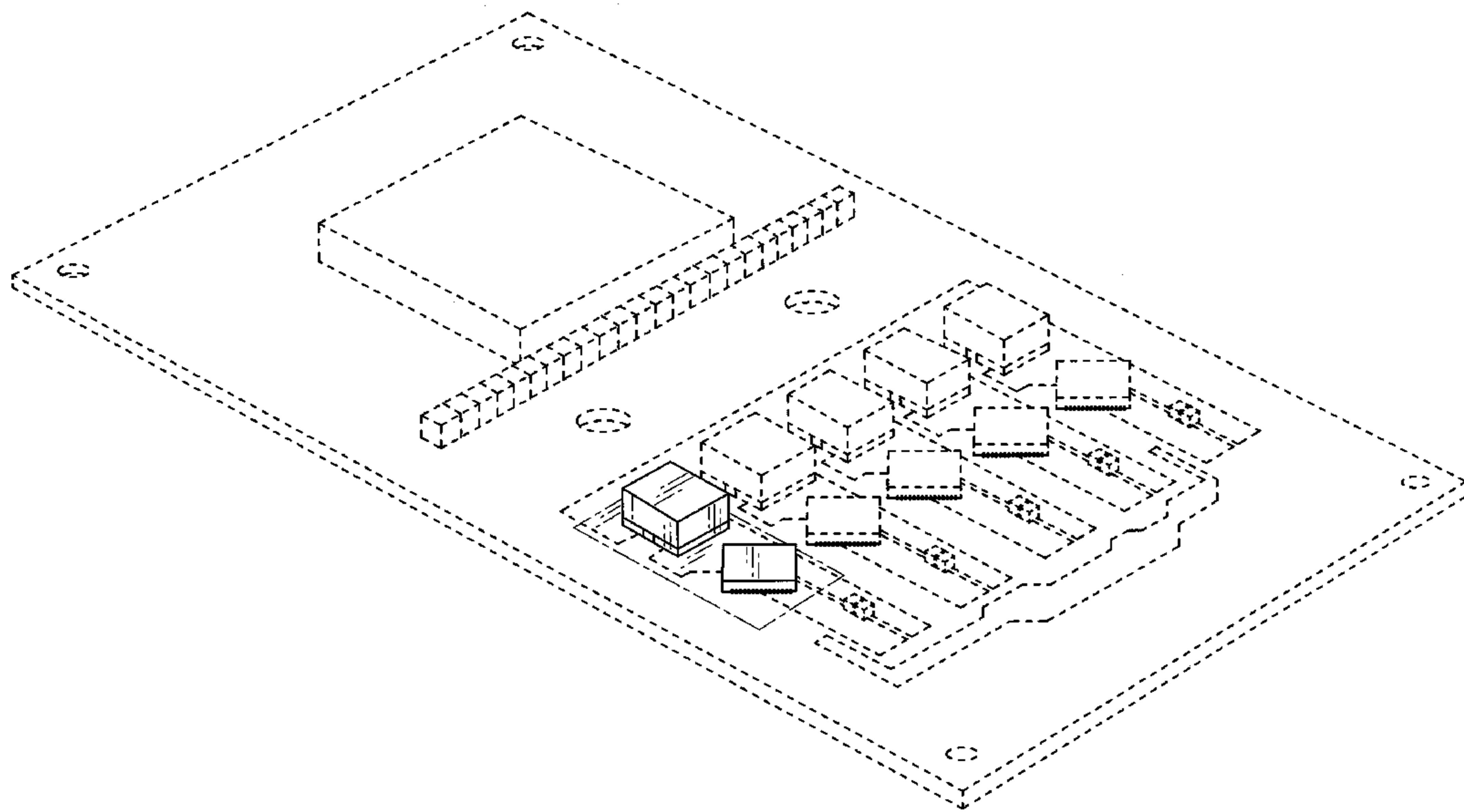
FIG. 8 is an enlarged view thereof showing the portion marked with F—F, G—G in FIG. 2;

FIG. 9 is an enlarged view thereof showing the portion marked with 9—9 in FIG. 6; and,

FIG. 10 is an enlarged view thereof showing the portion marked with 10—10 in FIG. 5.

The uneven spaced broken lines define the bounds of the claimed design and form no part thereof. The even spaced broken line showing of the printed circuit board is for illustrative purpose only and forms no part of the claimed design.

1 Claim, 6 Drawing Sheets



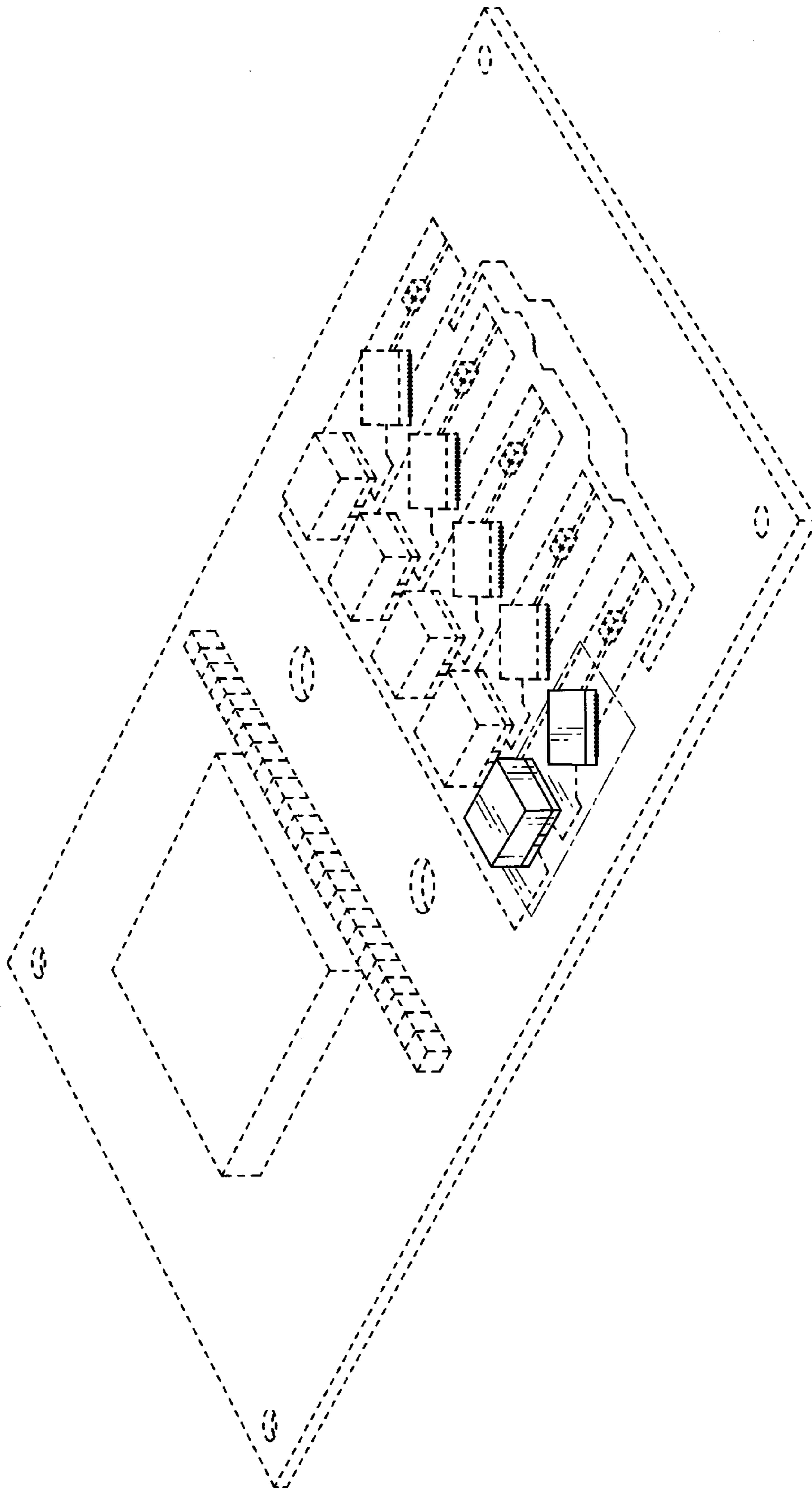


FIG.1

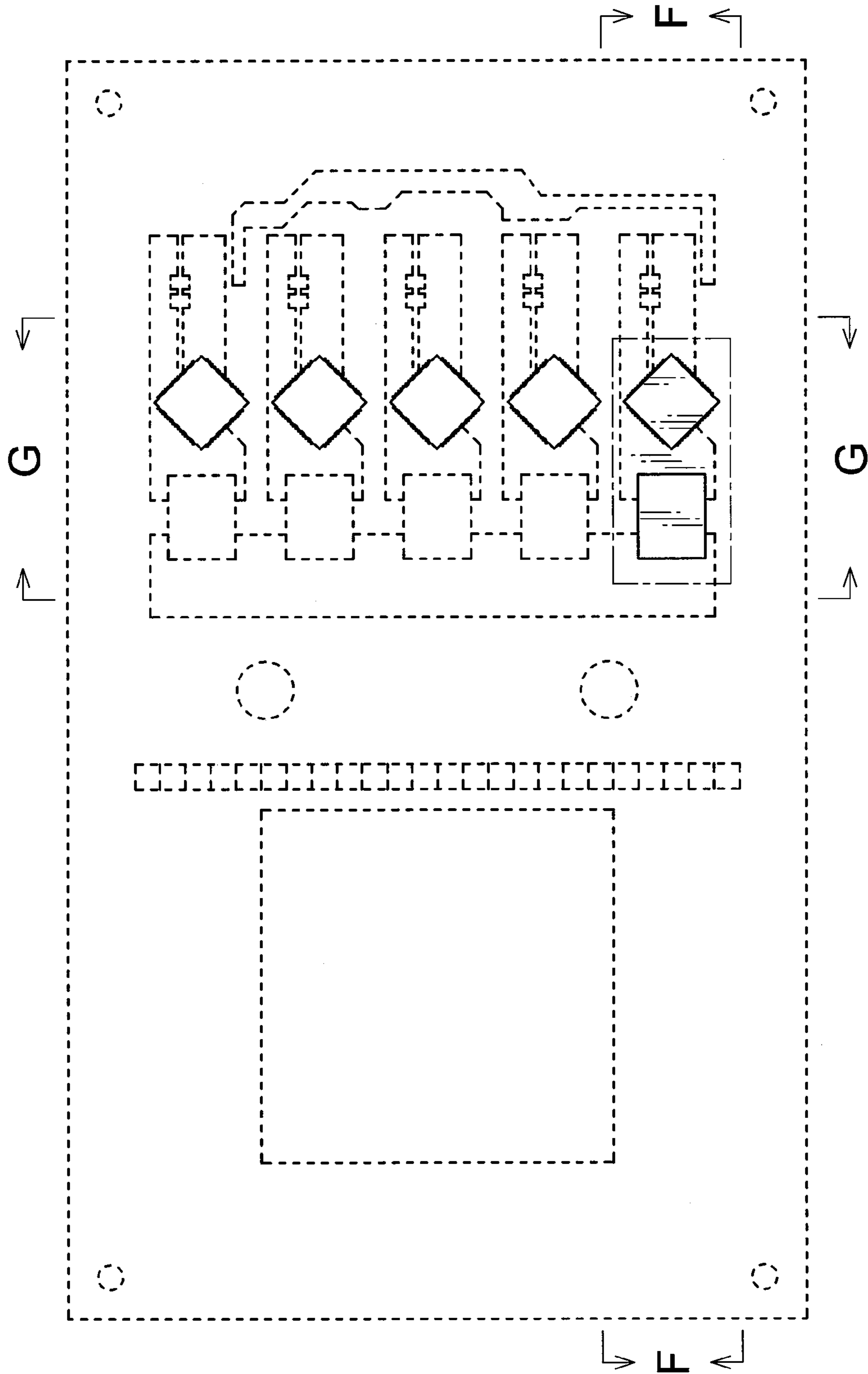


FIG. 2

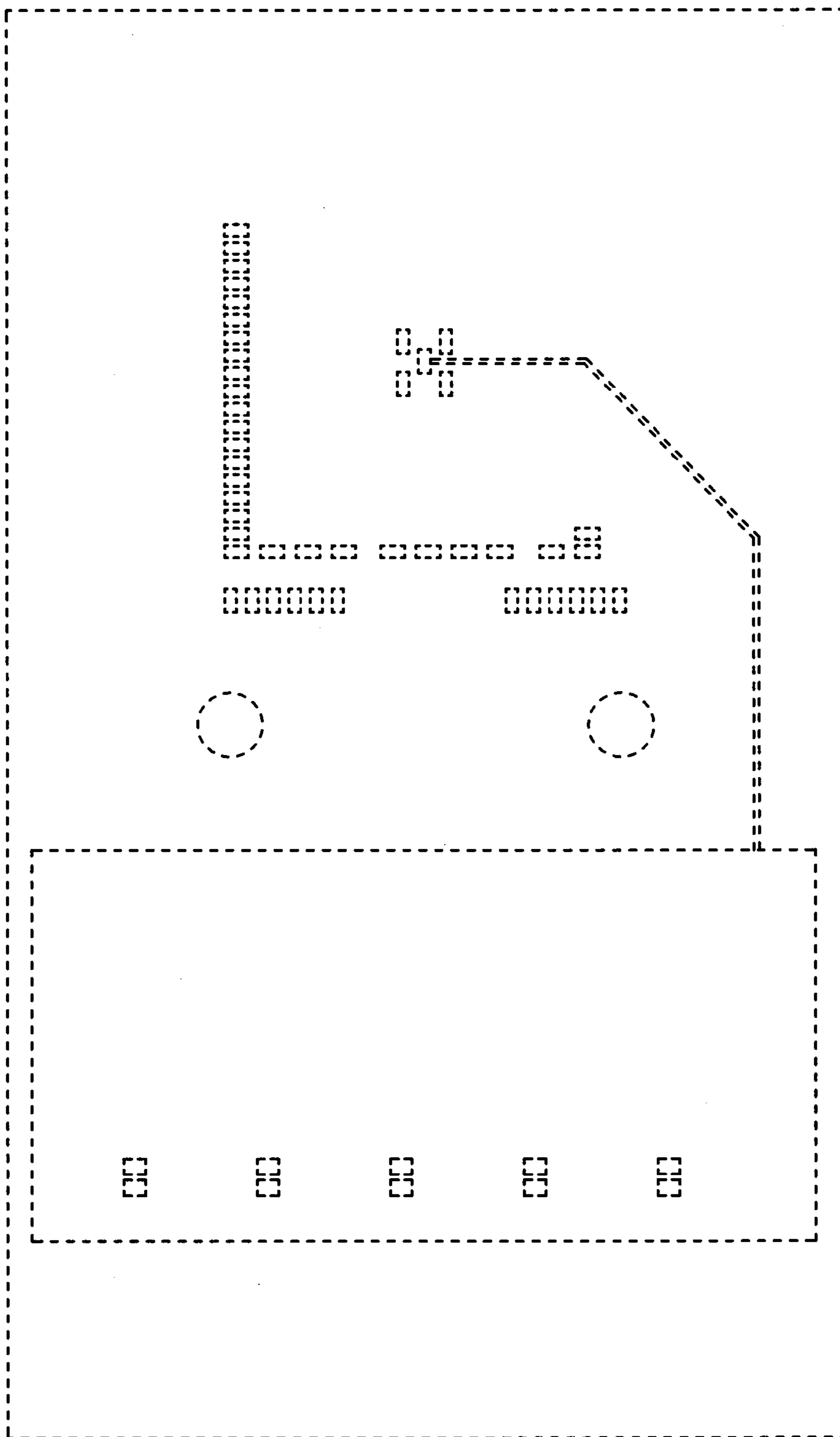


FIG. 3

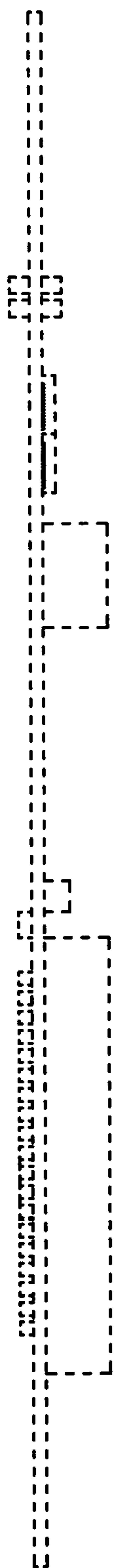


FIG. 4

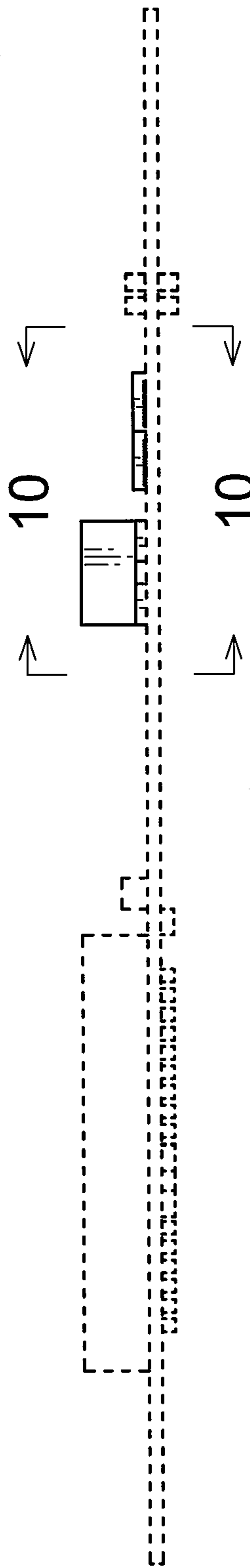


FIG. 5

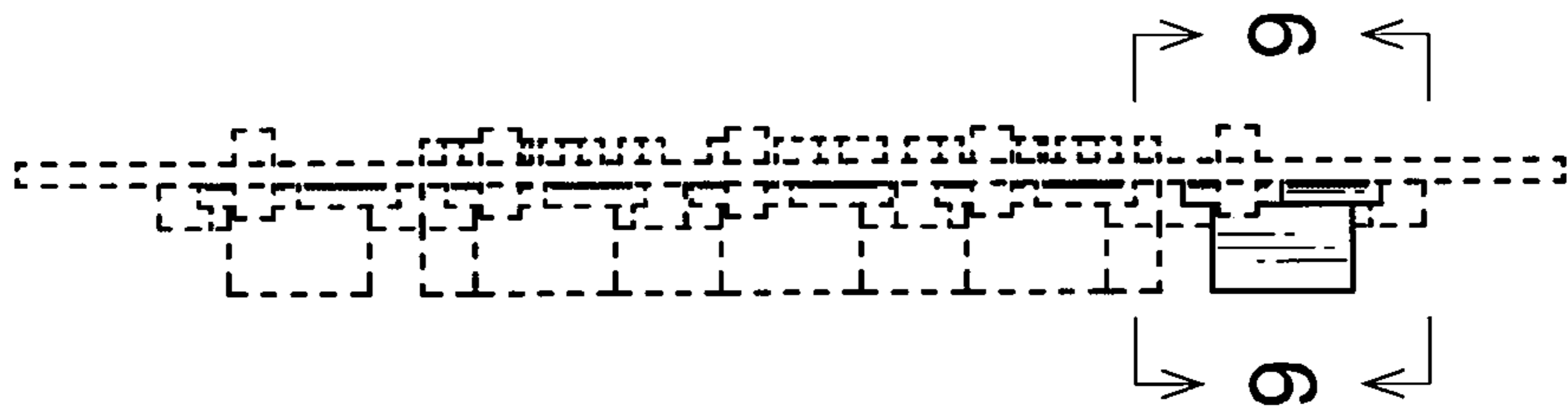


FIG. 6

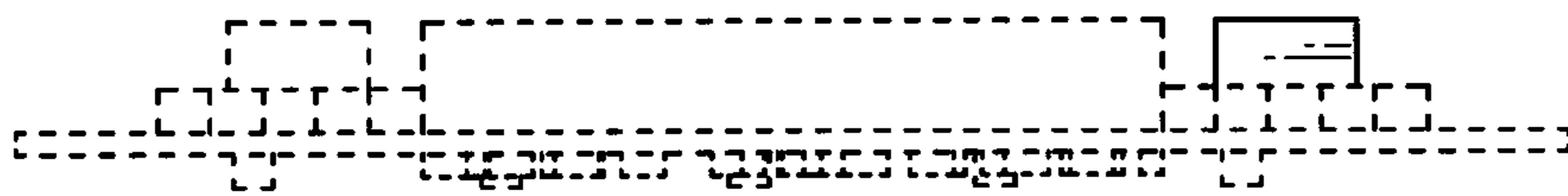


FIG. 7

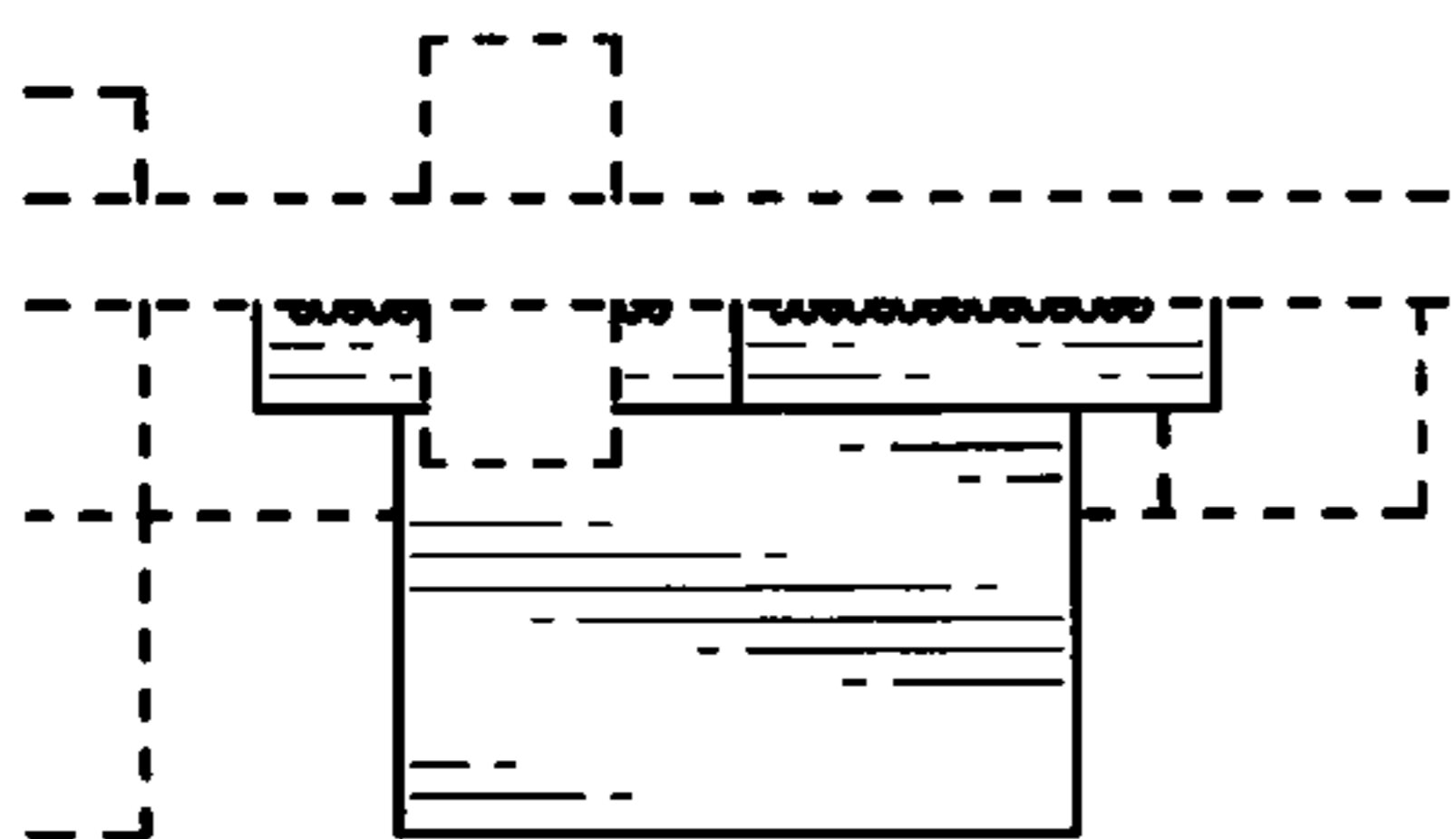


FIG. 9

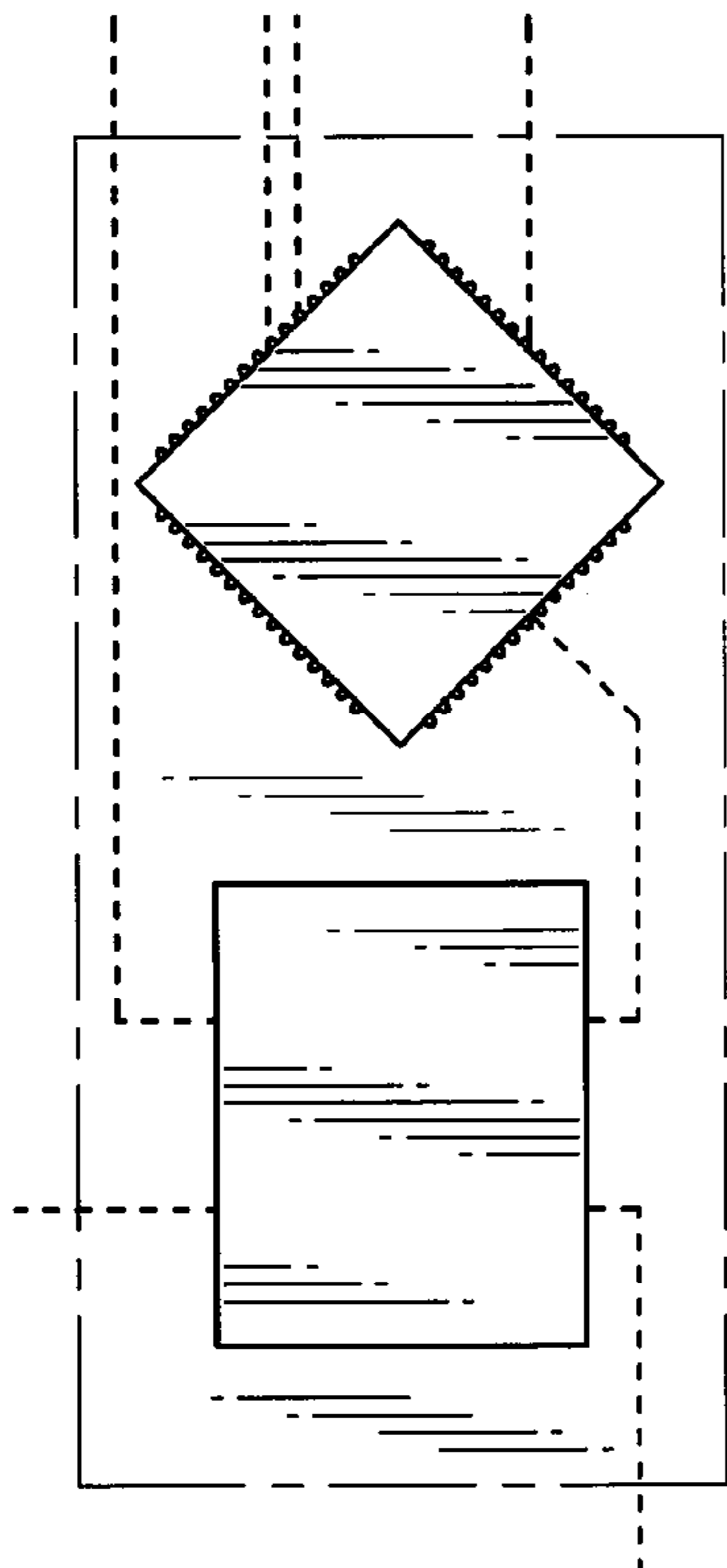


FIG. 8

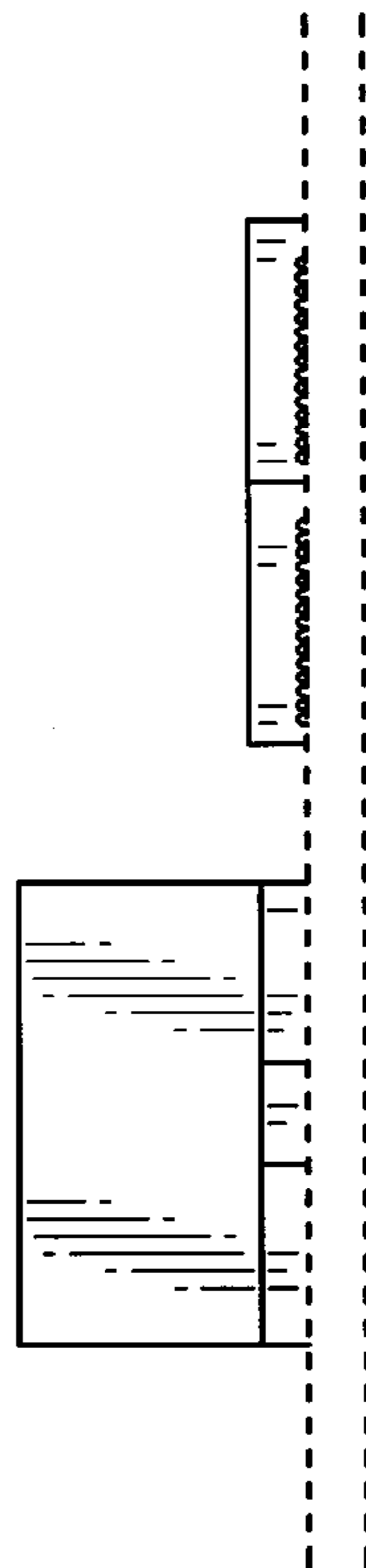


FIG. 10