US00D597504S

(12) United States Design Patent

Kobayashi et al.

(10) Patent No.: US D597,504 S
(45) Date of Patent: ** Aug. 4, 2009

(54) **PORTION OF A PRINTED CIRCUIT BOARD**

(75) Inventors: **Atsushi Kobayashi**, Tokyo (JP); **Hiroshi Takei**, Tokyo (JP)

(73) Assignee: **Kabushiki Kaisha Toshiba**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/279,827**

(22) Filed: **May 8, 2007**

(30) **Foreign Application Priority Data**

Nov. 30, 2006 (JP) 2006-033055

(51) **LOC (9) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Classification Search** D13/182; 29/829; 361/720, 749, 760, 776, 820; 174/250, 174/253, 255
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,724,514	A *	2/1988	Kaufman	361/710
5,339,219	A *	8/1994	Urich	361/760
D363,920	S	11/1995	Roberts et al.	
5,614,698	A *	3/1997	Estes	174/250
5,661,343	A *	8/1997	Takahashi et al.	257/723
5,838,546	A *	11/1998	Miyoshi	361/749
5,905,639	A *	5/1999	Warren	361/776
D428,860	S	8/2000	Siperek	
D466,093	S	11/2002	Ebihara et al.	
D471,167	S *	3/2003	Ebihara et al.	D13/182
D471,524	S *	3/2003	Ebihara et al.	D13/182
6,585,525	B2 *	7/2003	Jung et al.	439/55
6,721,821	B1 *	4/2004	Rent	710/29
6,985,341	B2 *	1/2006	Vinciarelli et al.	361/58
D570,307	S *	6/2008	Kobayashi et al.	D13/180
D576,577	S *	9/2008	Kobayashi et al.	D13/182
2002/0189083	A1 *	12/2002	Matsumoto et al.	29/743
2006/0126314	A1 *	6/2006	Jeong	361/760
2006/0239037	A1 *	10/2006	Repetto et al.	362/800
2007/0294889	A1 *	12/2007	Schmitt et al.	29/831
2008/0007926	A1 *	1/2008	Lee et al.	361/760

* cited by examiner

Primary Examiner—Selina Sikder
(74) *Attorney, Agent, or Firm*—Banner & Witcoff, Ltd.

(57) **CLAIM**

The ornamental design for a portion of a printed circuit board, as shown and described.

DESCRIPTION

FIG. **1** is a front, bottom and right side perspective view of a portion of a printed circuit board, showing our new design;

FIG. **2** is a front elevational view thereof;

FIG. **3** is a rear elevational view thereof;

FIG. **4** is a top plan view thereof;

FIG. **5** is a bottom plan view thereof;

FIG. **6** is a right side elevational view thereof;

FIG. **7** is a left side elevational view thereof;

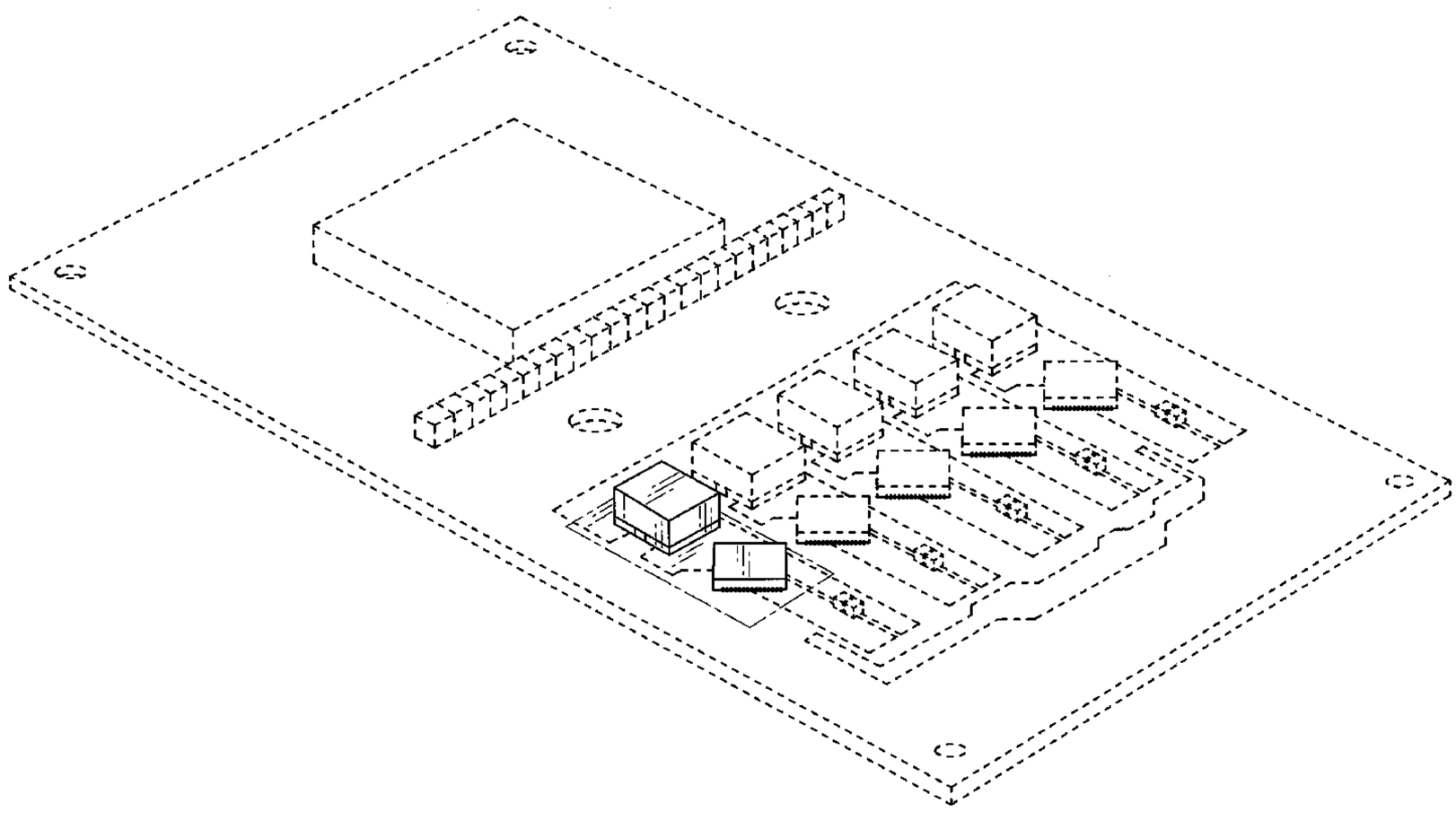
FIG. **8** is an enlarged view thereof showing the portion marked with F—F, G—G in FIG. **2**;

FIG. **9** is an enlarged view thereof showing the portion marked with **9**—**9** in FIG. **6**; and,

FIG. **10** is an enlarged view thereof showing the portion marked with **10**—**10** in FIG. **5**.

The uneven spaced broken lines define the bounds of the claimed design and form no part thereof. The even spaced broken line showing of the printed circuit board is for illustrative purpose only and forms no part of the claimed design.

1 Claim, 6 Drawing Sheets



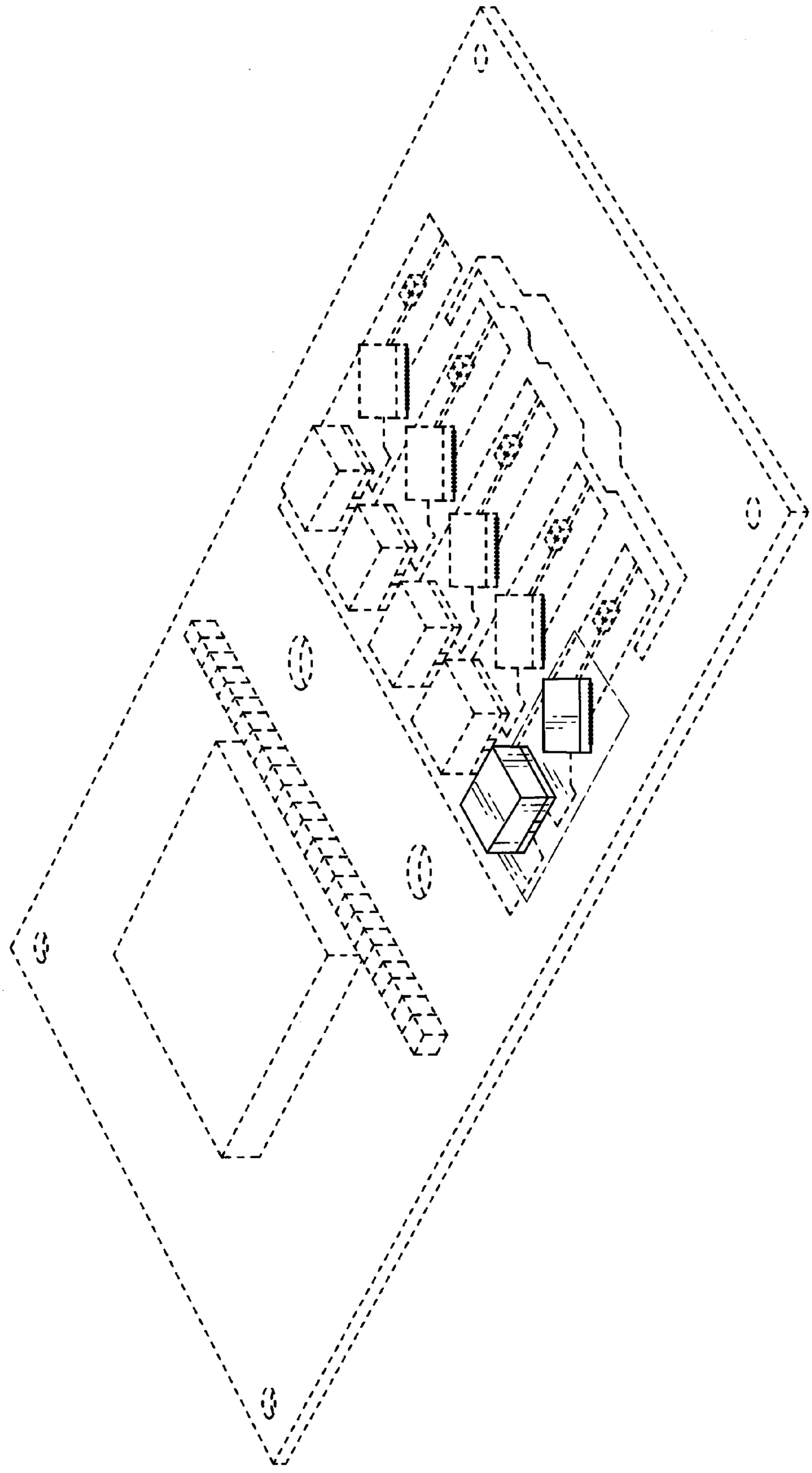


FIG.1

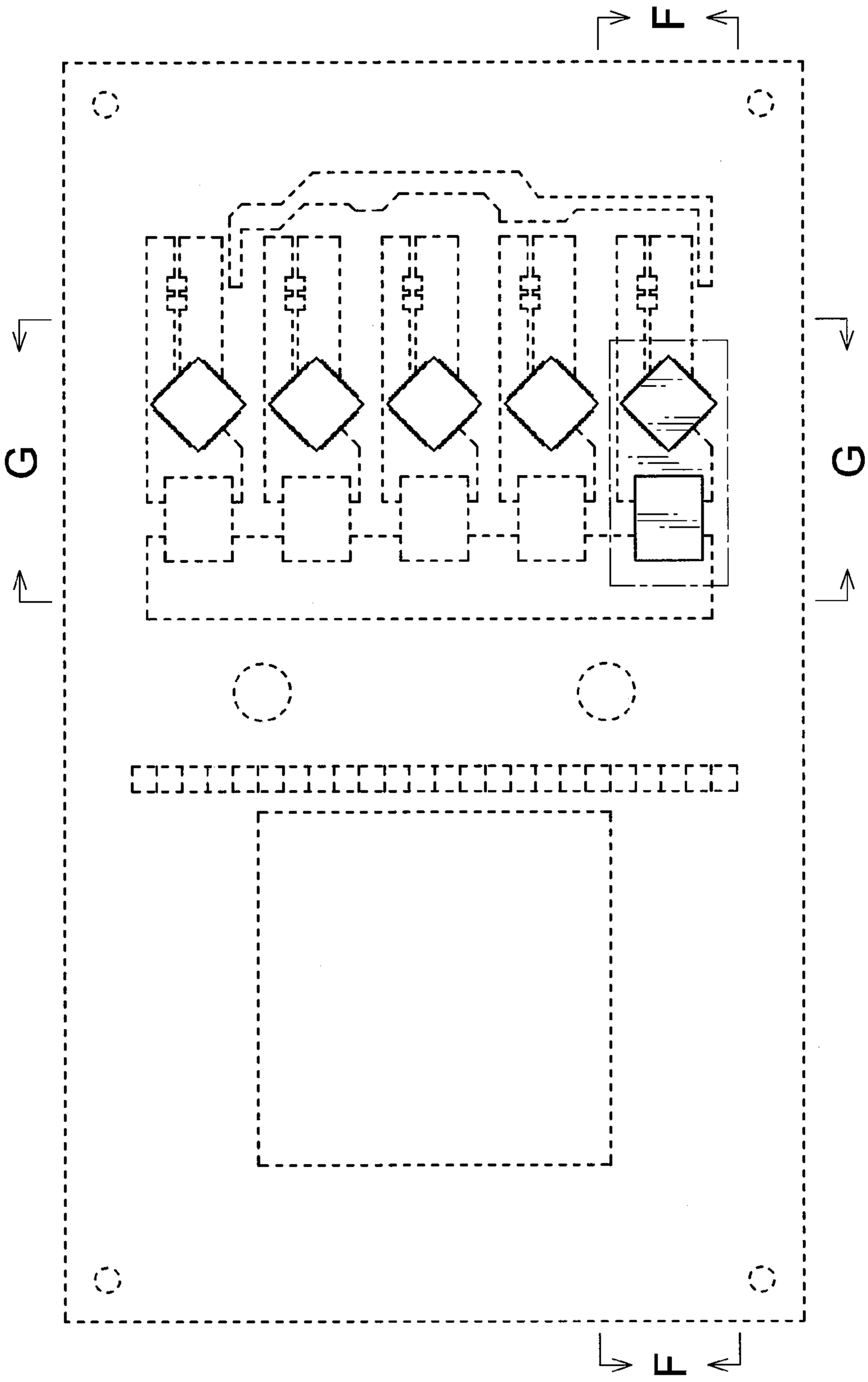


FIG.2

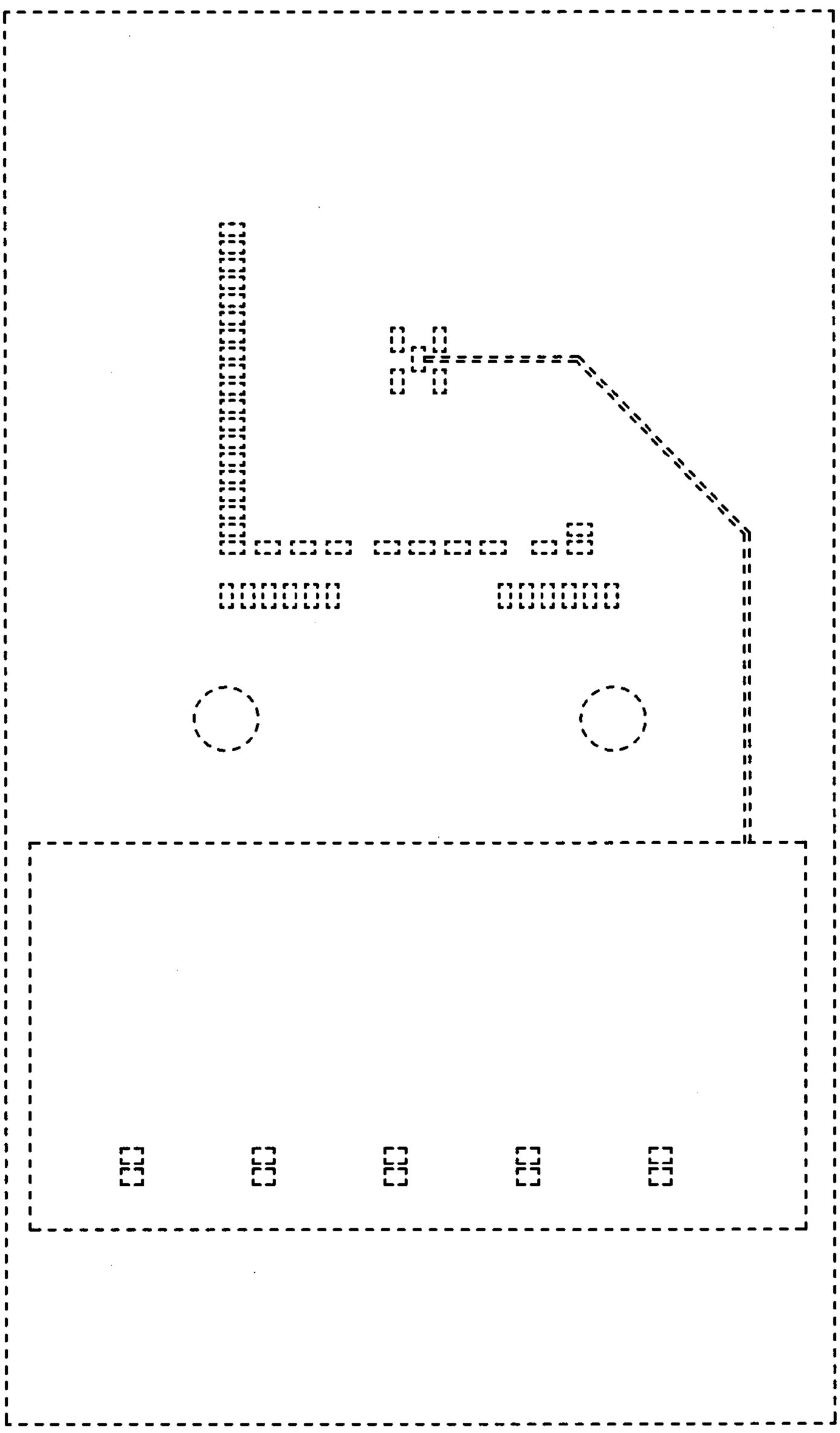


FIG.3

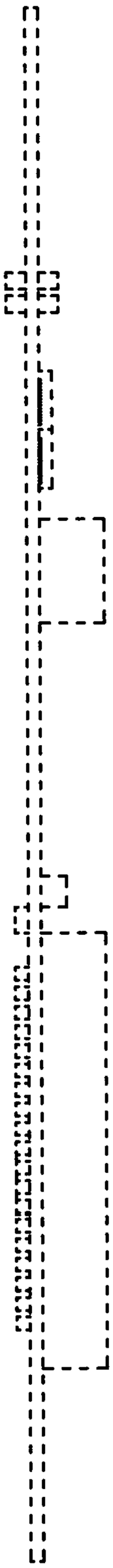


FIG.4

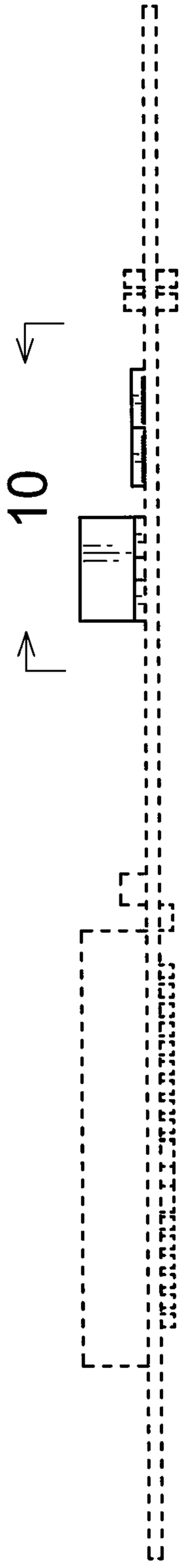


FIG.5

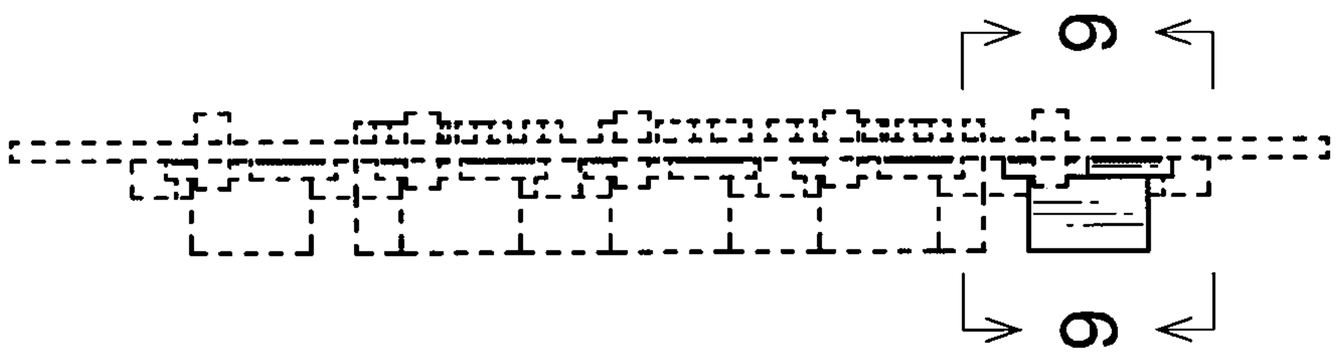


FIG.6

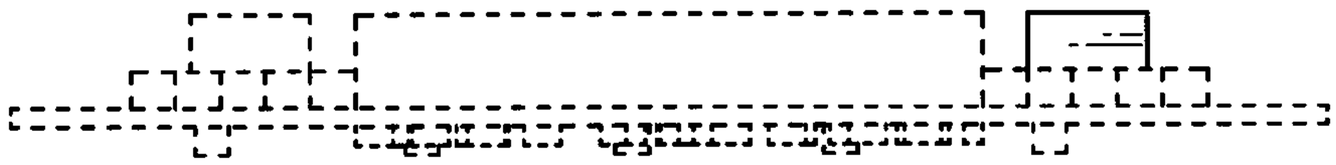


FIG.7

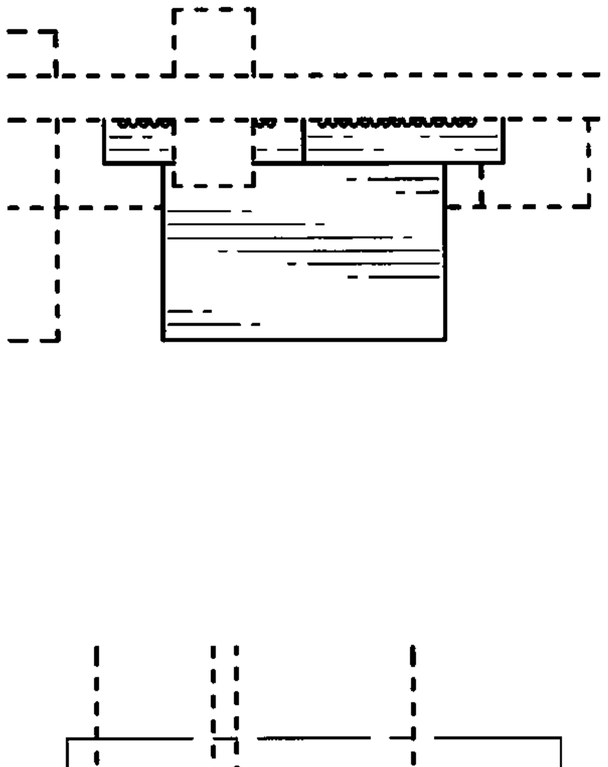


FIG.9

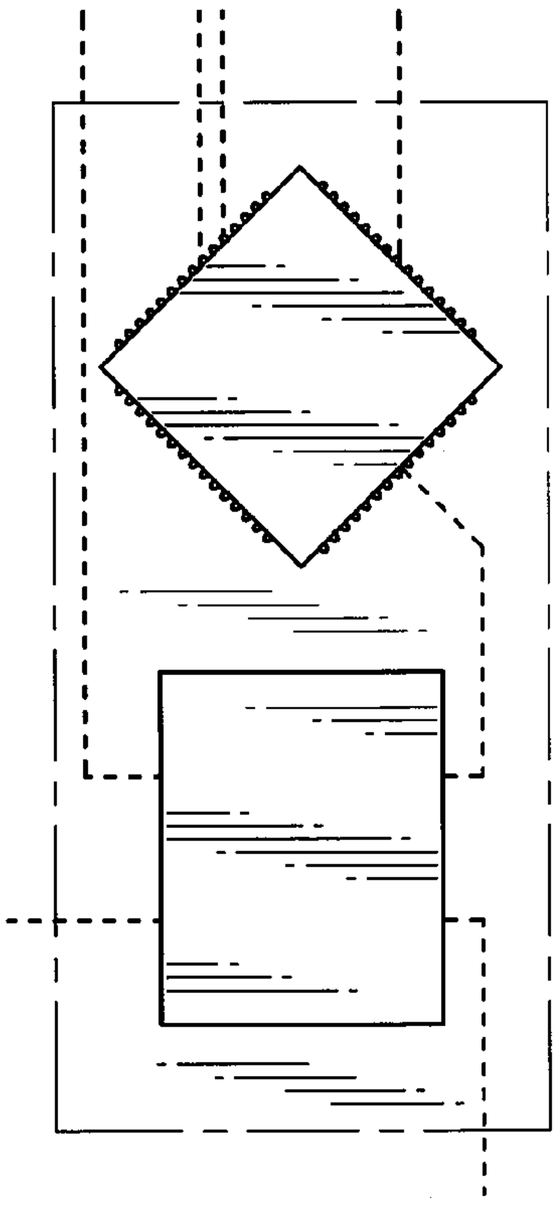


FIG.8

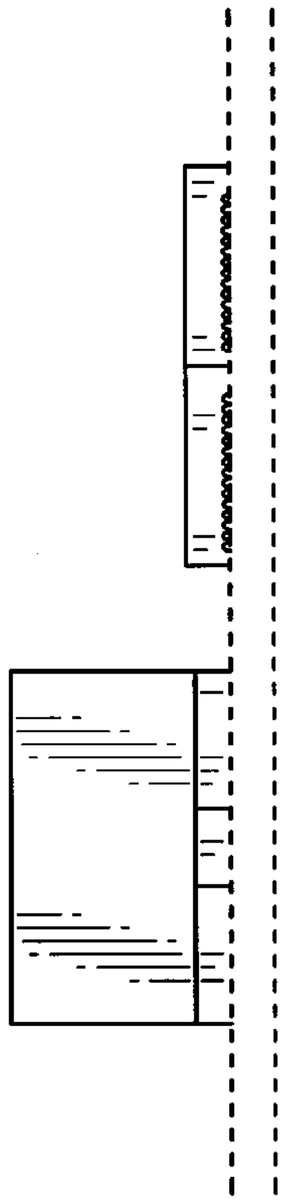


FIG.10