



US00D595226S

(12) **United States Design Patent**
Jidaisho

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(45) **Date of Patent:** **** Jun. 30, 2009**

(54) **TRANSFORMER FOR ELECTRONIC CIRCUIT**

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* cited by examiner

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(**) Term: **14 Years**

(21) Appl. No.: **29/302,255**

(22) Filed: **Jan. 14, 2008**

(57) **CLAIM**

The ornamental design for a transformer for electronic circuit, as shown and described.

(51) **LOC (9) Cl.** **13-02**

(52) **U.S. Cl.** **D13/110**

(58) **Field of Classification Search** D13/110,
D13/101, 117, 123, 184, 199; 307/150; 336/90,
336/107, 192; 361/707, 730; 363/142–144,
363/146, 153, 171

See application file for complete search history.

DESCRIPTION

FIG. 1 is a bottom perspective view of a transformer for electronic circuit showing my new design;

FIG. 2 is a front elevation view thereof;

FIG. 3 is a rear elevation view thereof;

FIG. 4 is a top plan view thereof;

FIG. 5 is a bottom plan view thereof;

FIG. 6 is a left side view thereof; and,

FIG. 7 is a right side view thereof.

The broken lines which define the bounds of the claimed design form no part thereof. The broken lines shown represent unclaimed subject matter and form no part of the claimed design.

(56) **References Cited**

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1 Claim, 7 Drawing Sheets

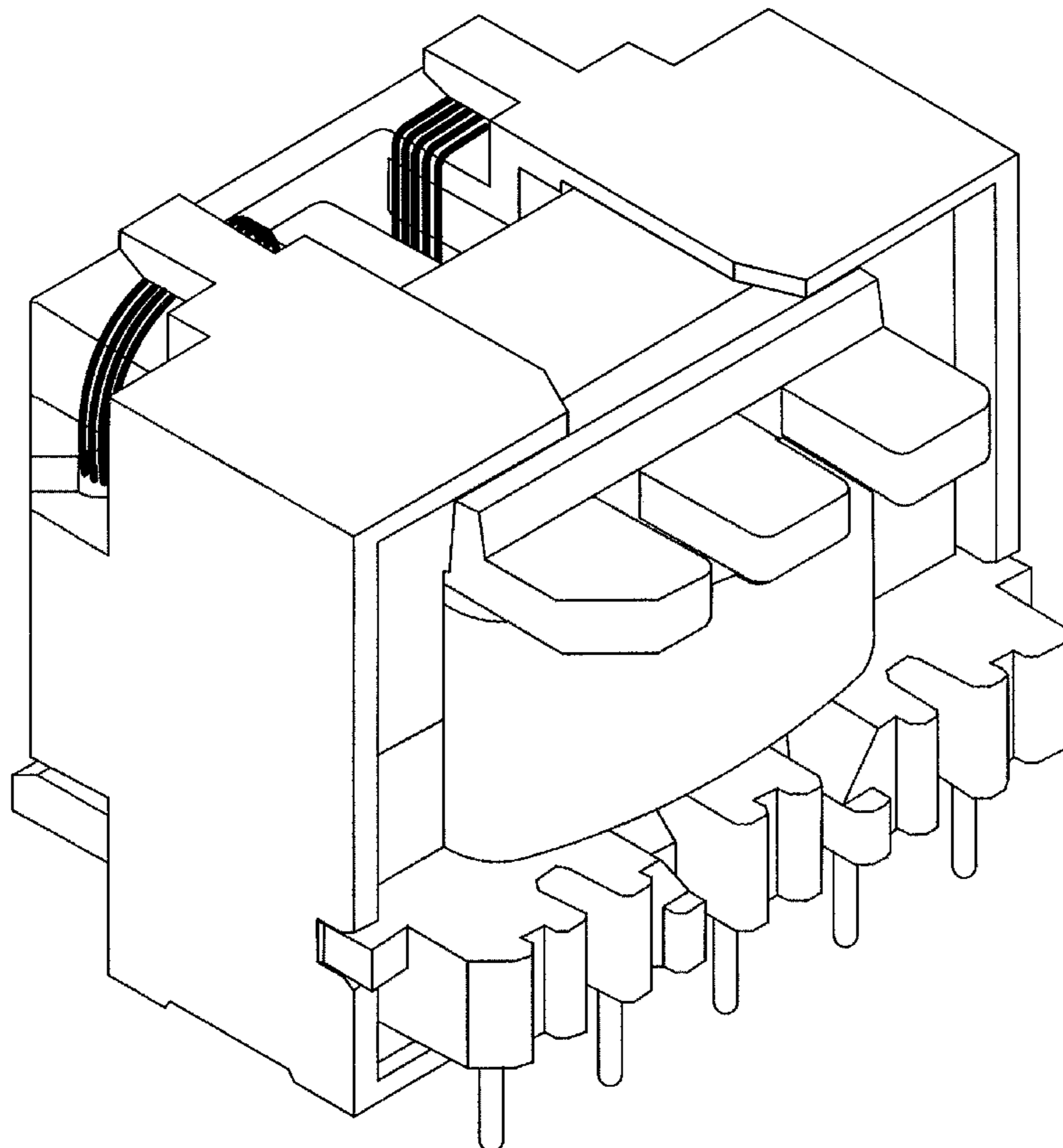
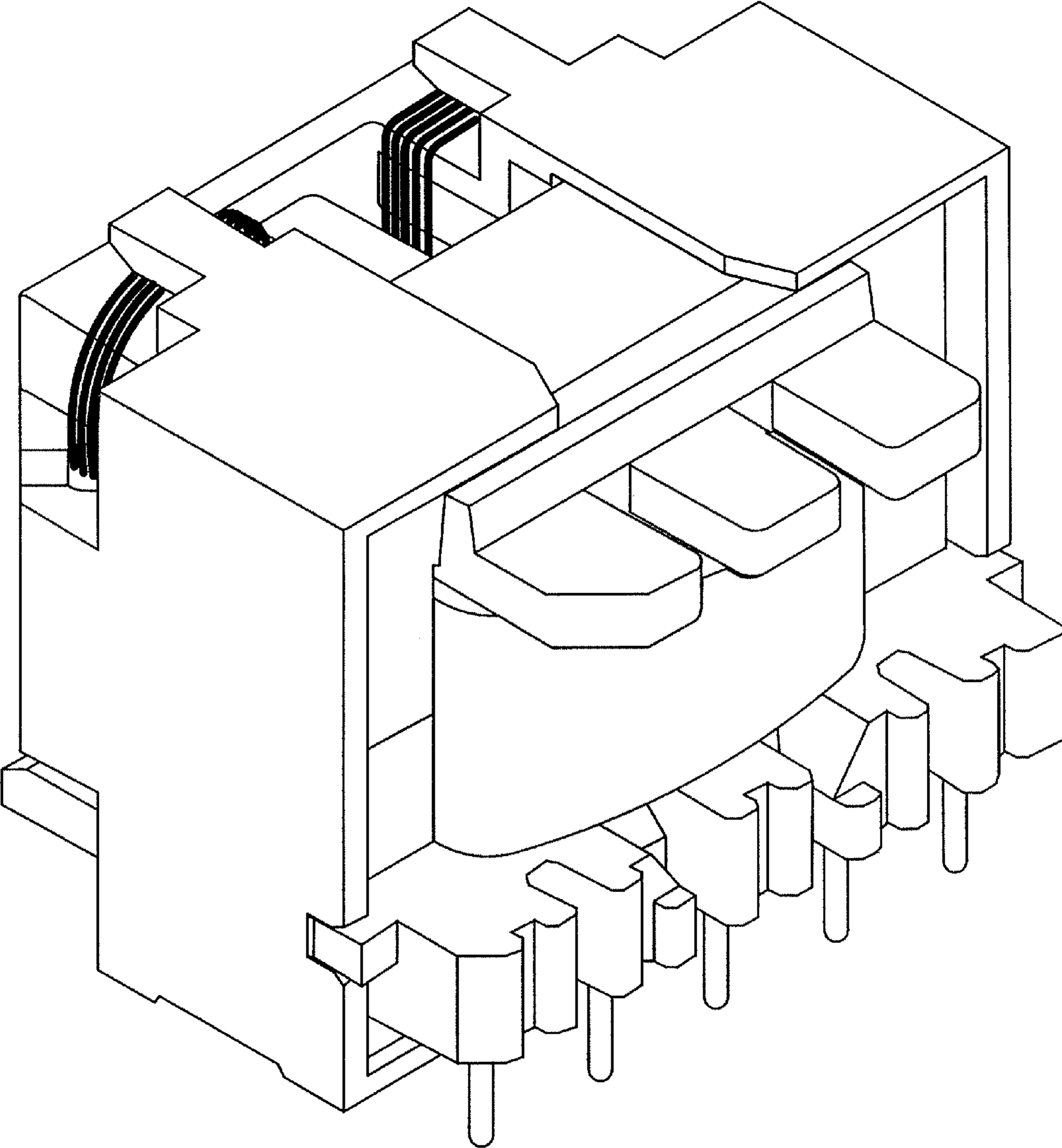


FIGURE 1



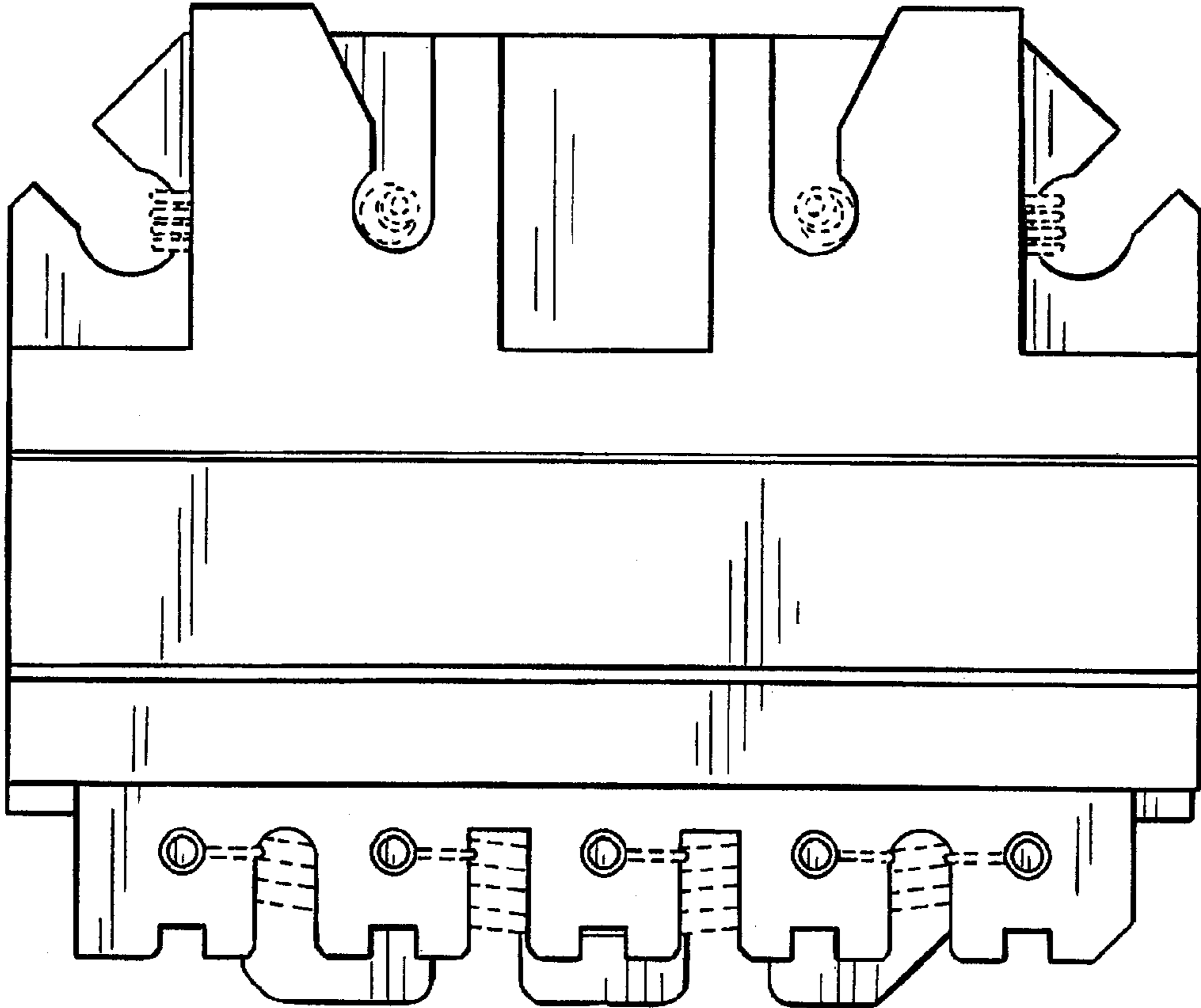


FIG. 2

FIGURE 3

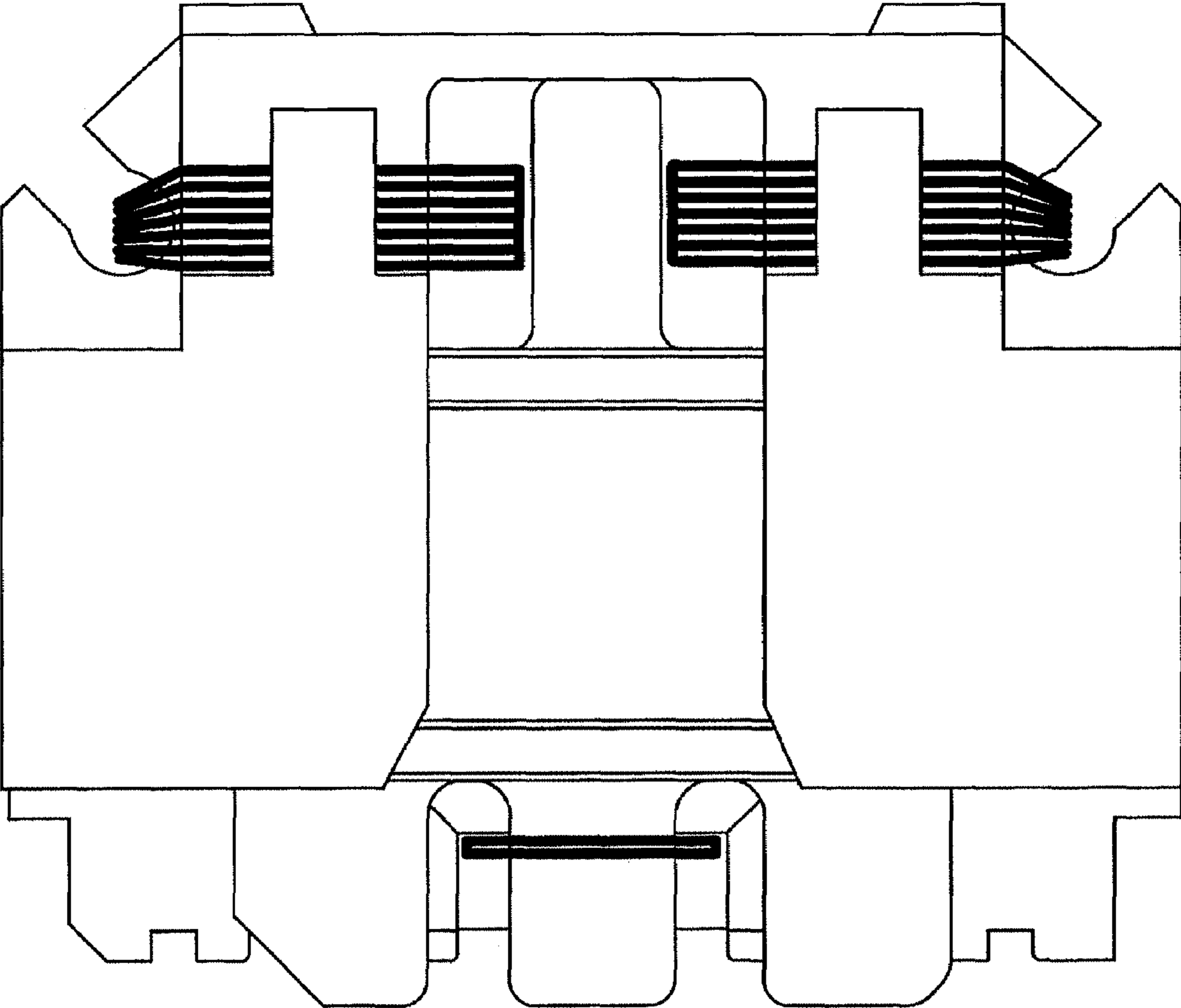


FIGURE 4

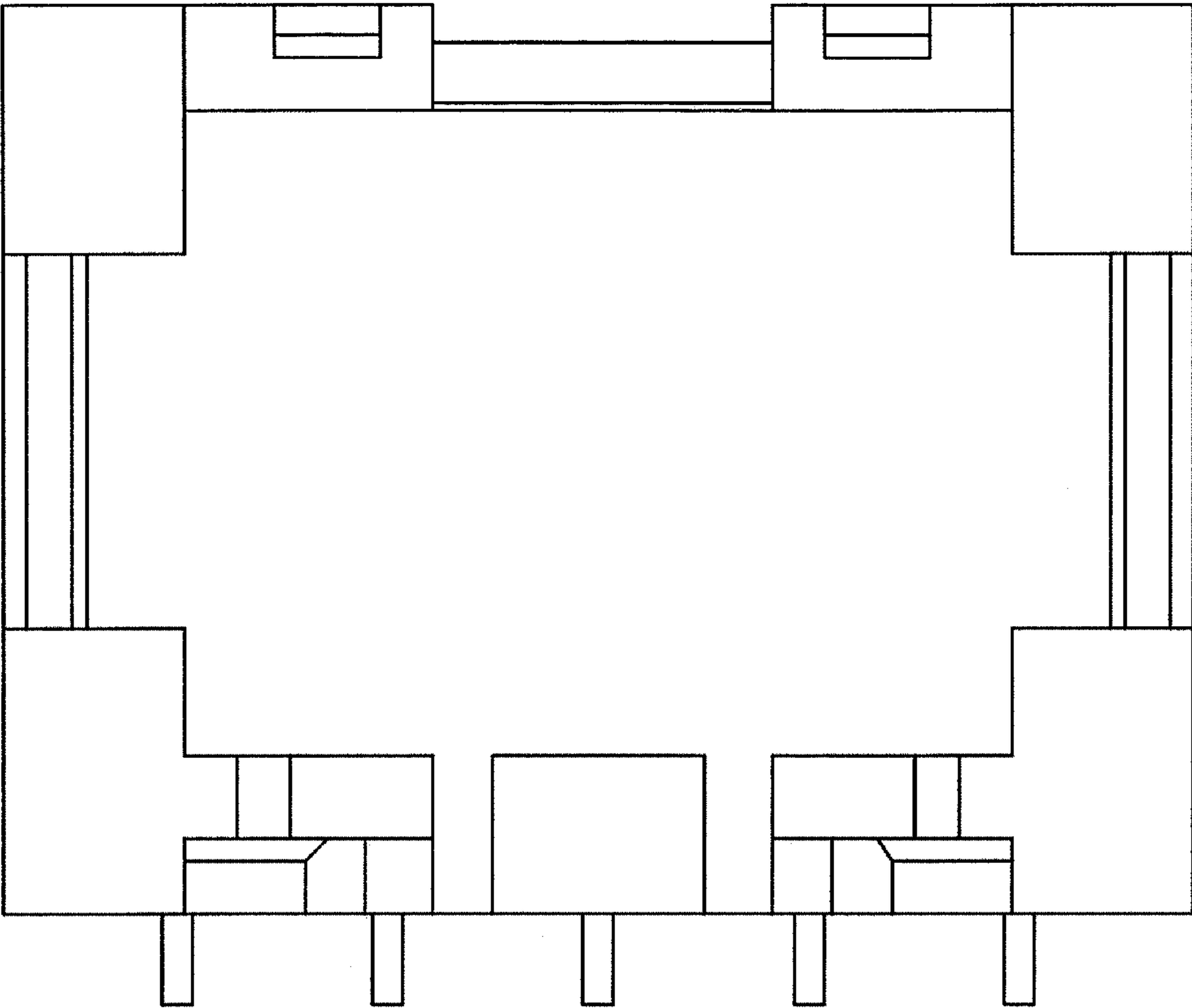


FIGURE 5

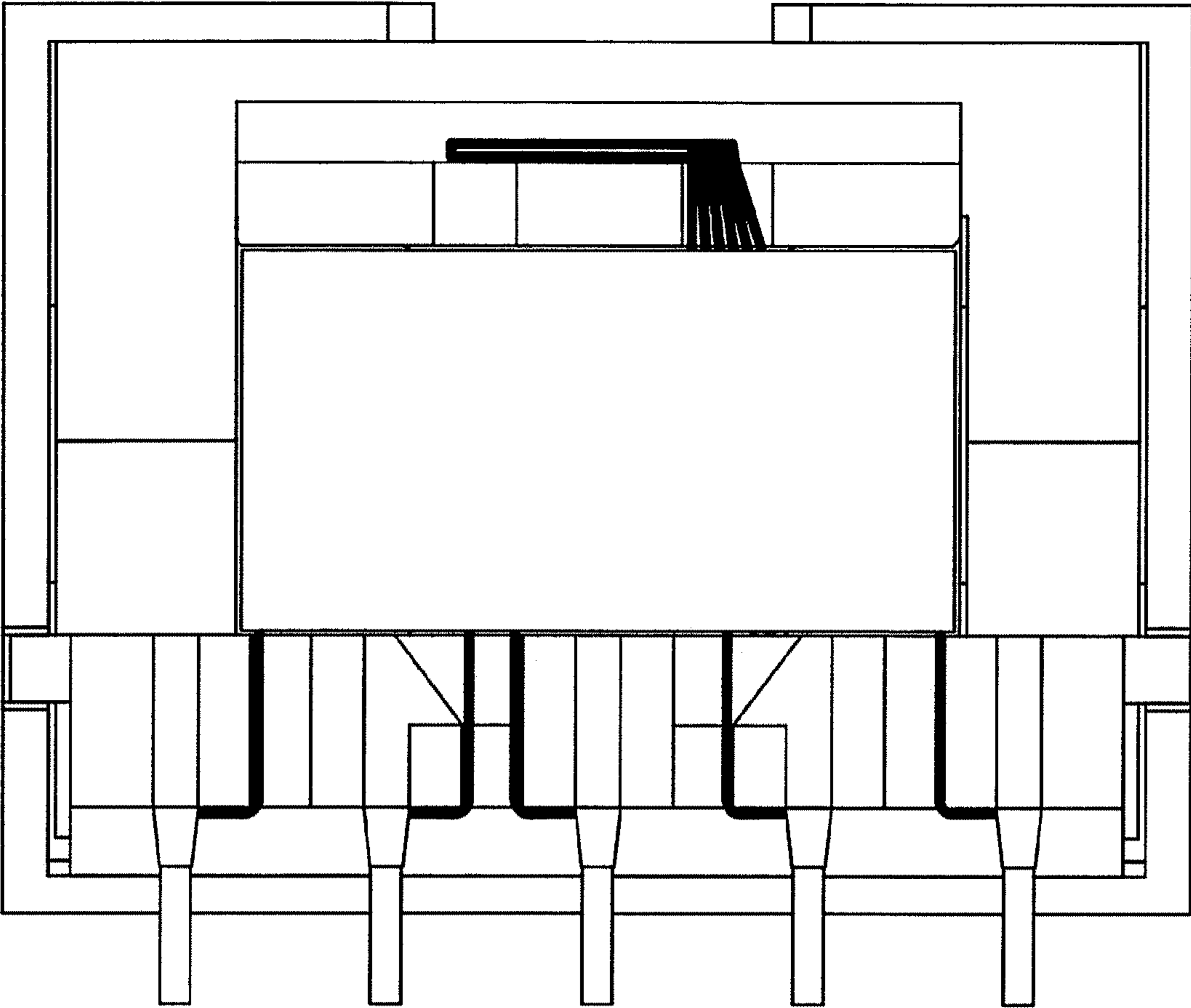


FIGURE 6

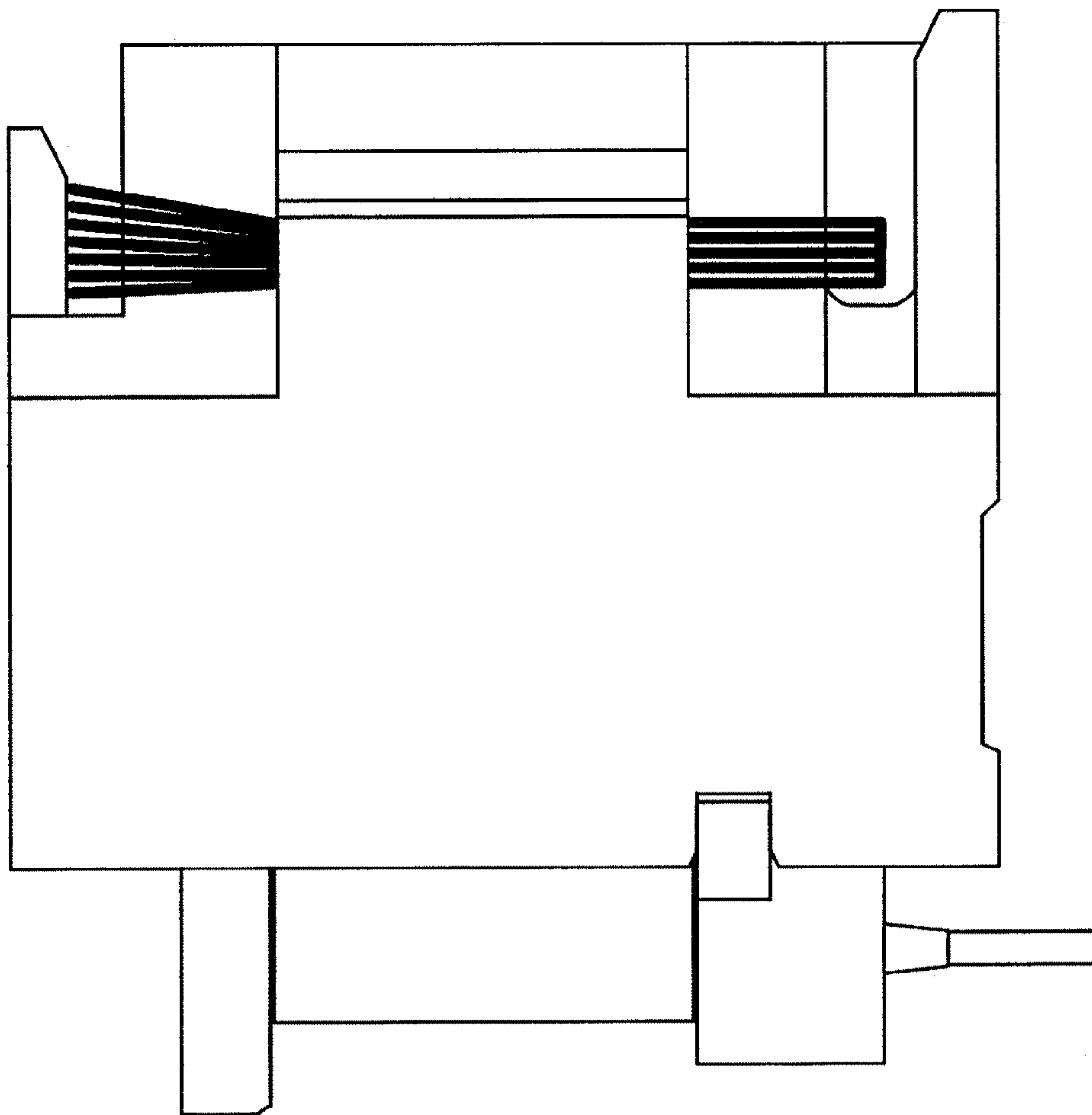


FIGURE 7

