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(12) **United States Design Patent**
Toiya et al.

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(54) **PROCESS TUBE FOR MANUFACTURING SEMICONDUCTOR WAFERS**

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(**) Term: **14 Years**

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(30) **Foreign Application Priority Data**

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(51) **LOC (9) Cl.** **15-09**

(52) **U.S. Cl.** **D15/144.1; D13/182**

(58) **Field of Classification Search** D7/660.2,
D7/701; D13/182; D15/138, 144, 144.1,
D15/199; D23/266; 83/35, 39; 118/715;
138/92, 118, 118.1, 121, 178; 206/41.18;
414/147, 217, 247, 253, 935-941

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a process tube for manufacturing semiconductor wafers, as shown and described.

DESCRIPTION

FIG. 1 is a front view of the design for a process tube for manufacturing semiconductor wafers in accordance with the invention;

FIG. 2 is a rear view thereof;

FIG. 3 is a right side view thereof;

FIG. 4 is a left side view thereof;

FIG. 5 is a bottom view thereof;

FIG. 6 is a top view thereof; and,

FIG. 7 is a front perspective view thereof.

The broken line showings are for the purpose of illustrating environmental structure and forms no part of the claimed design.

1 Claim, 4 Drawing Sheets

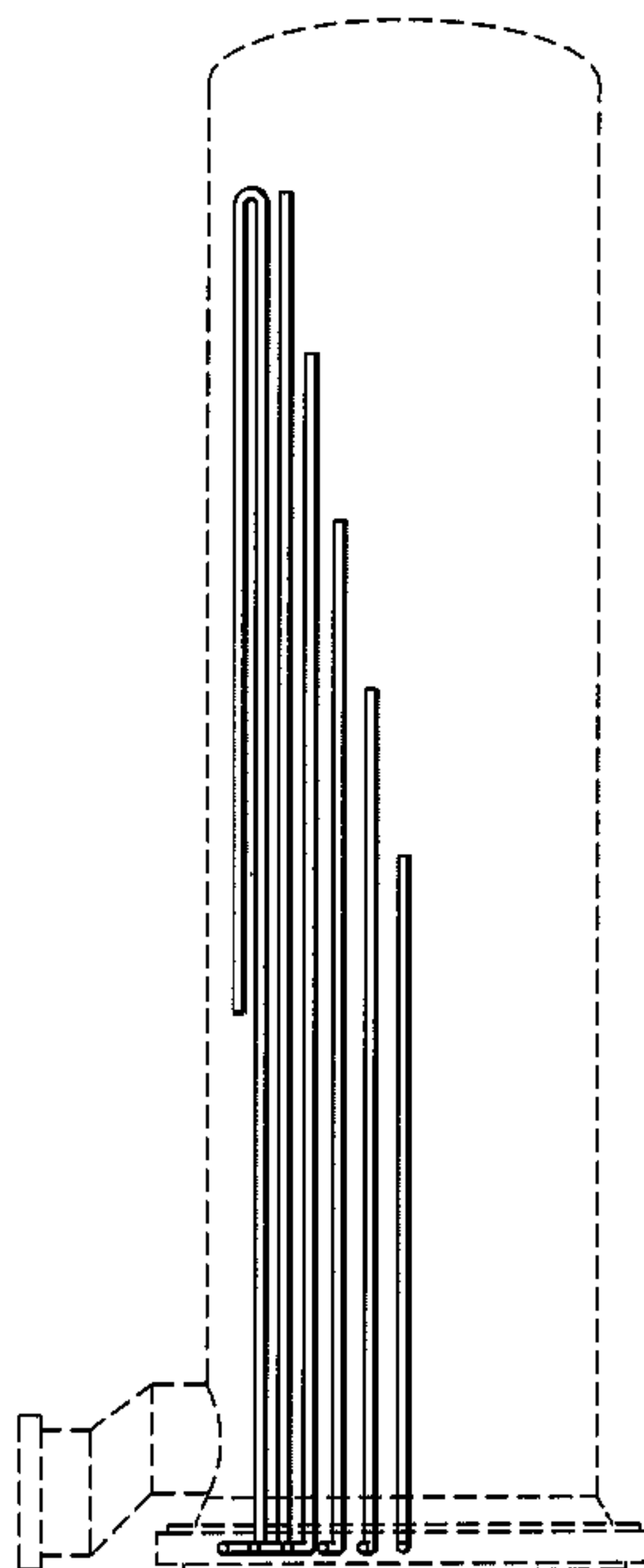


FIG. 1

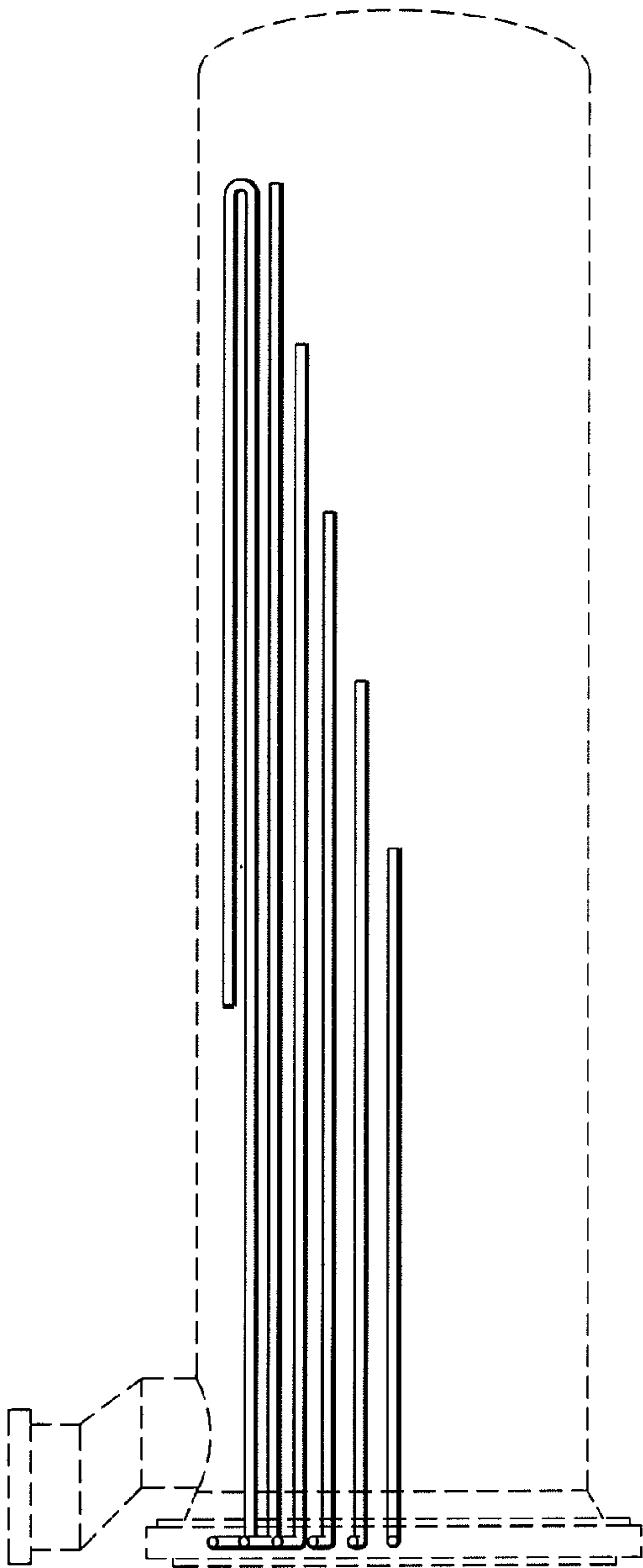


FIG. 2

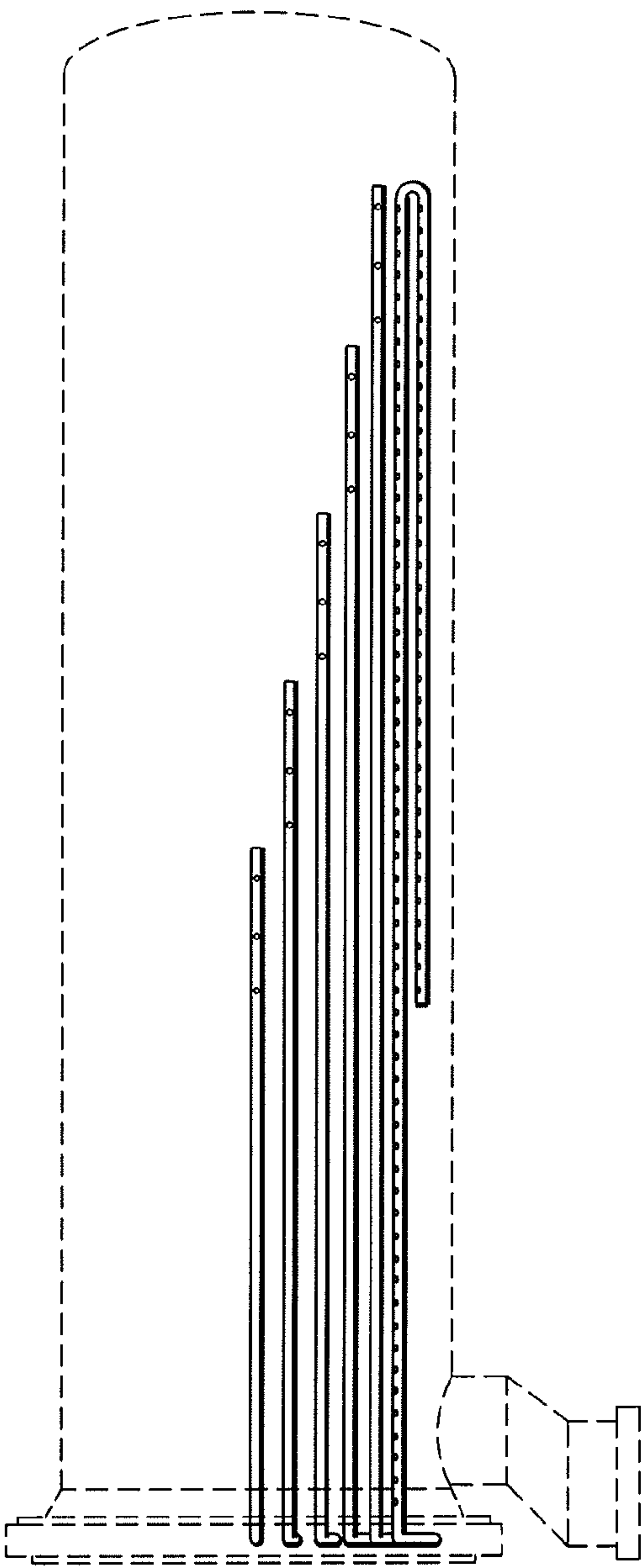


FIG. 3

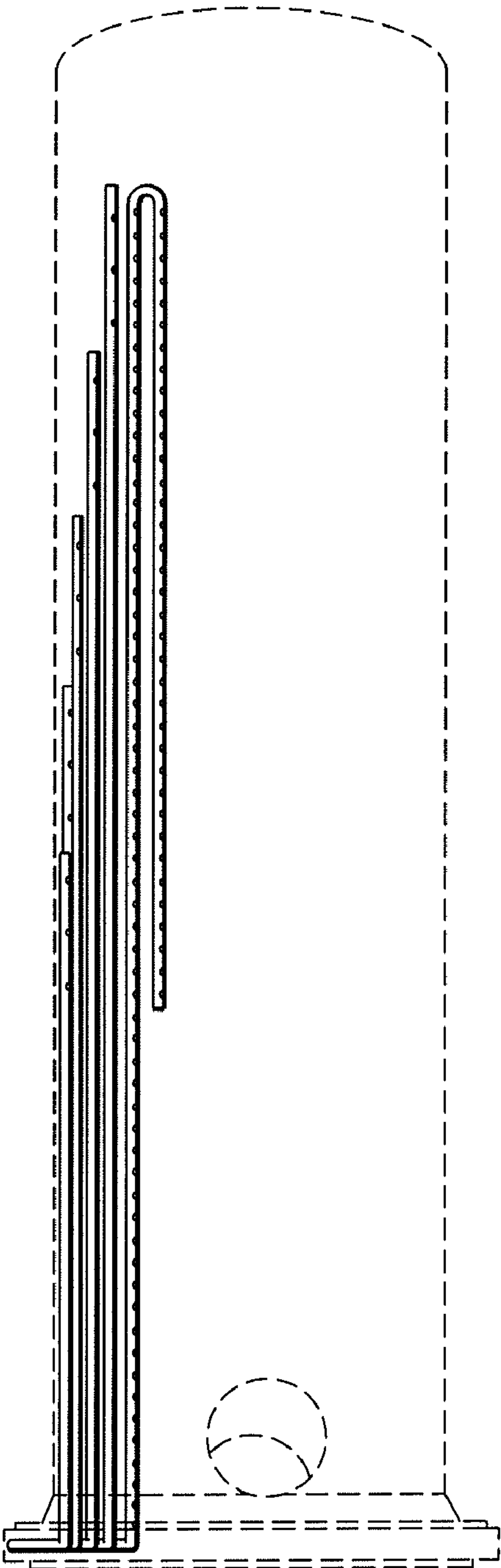


FIG. 4

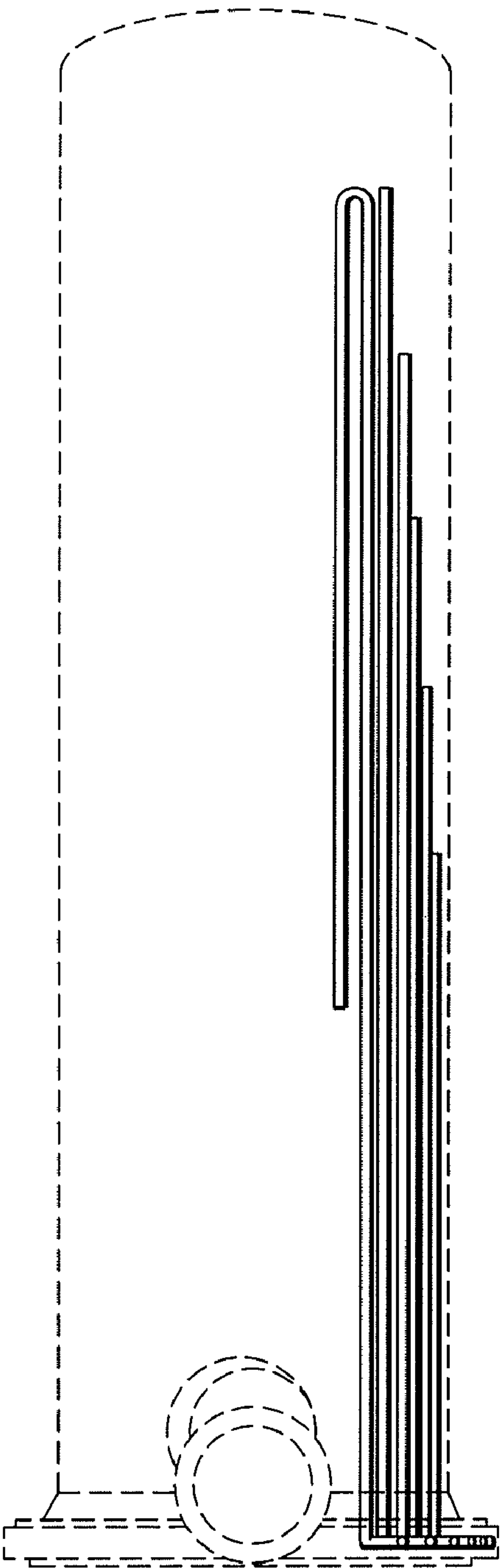


FIG. 5

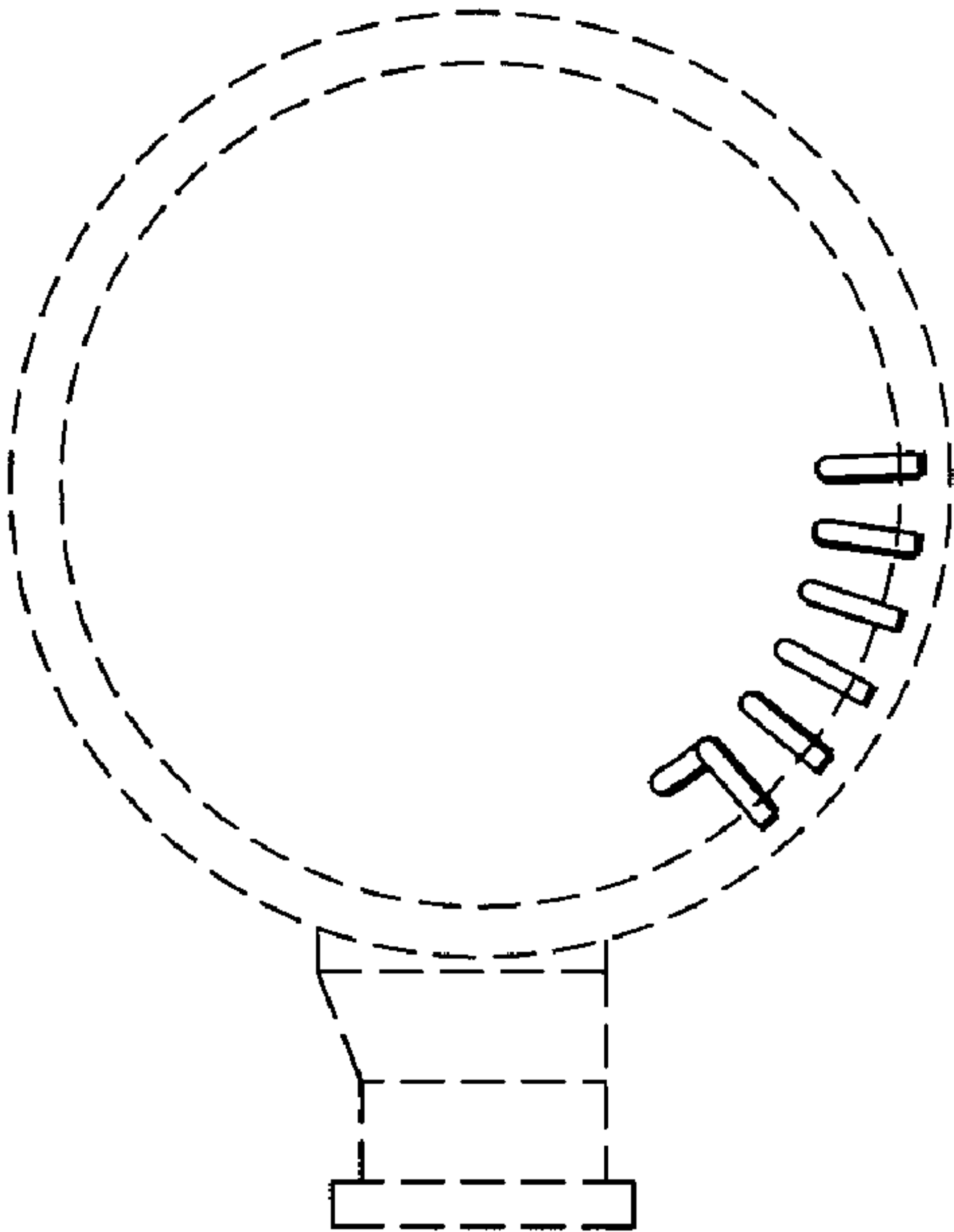


FIG. 6

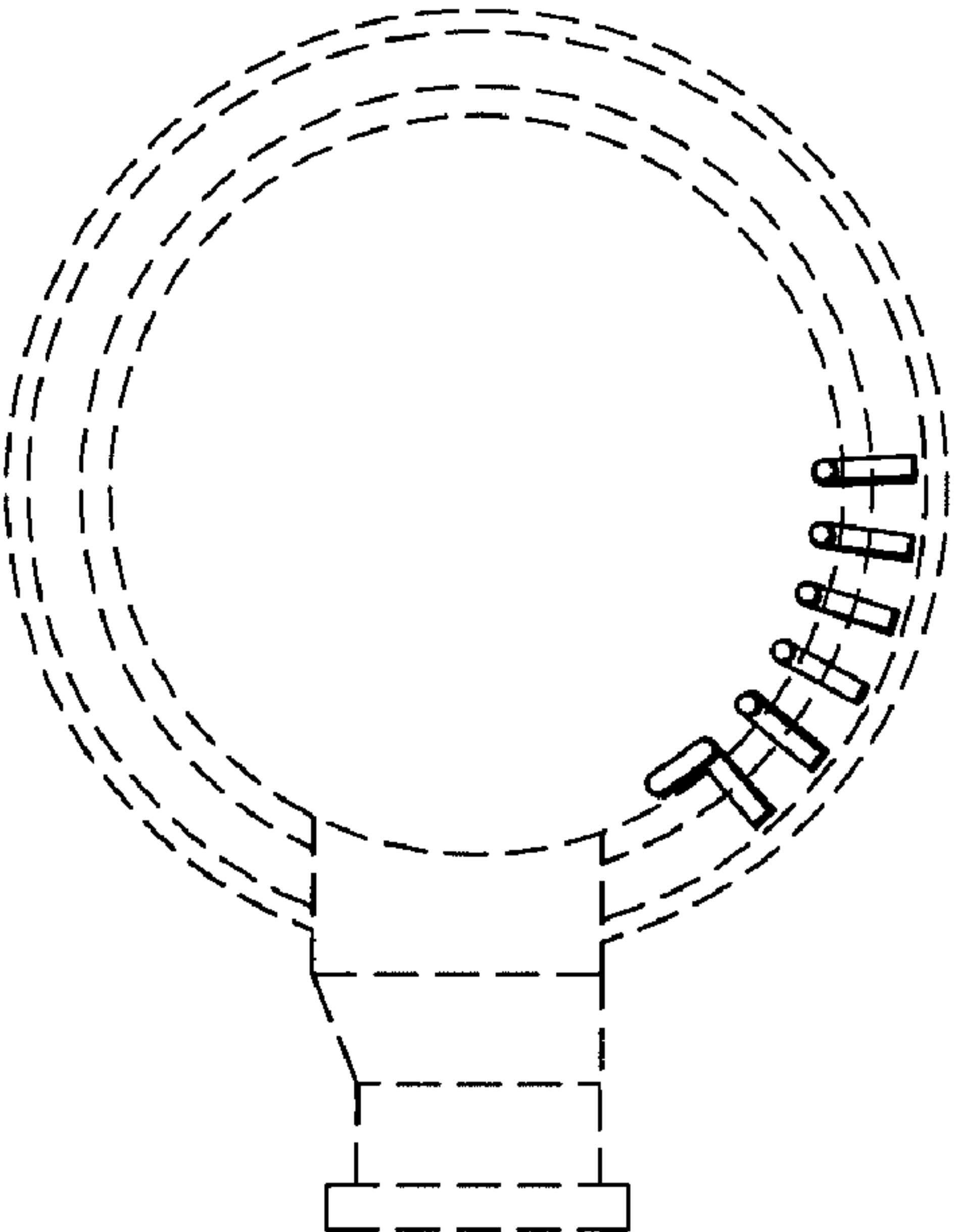


FIG. 7

