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(12) **United States Design Patent**
Kaneko

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(54) **PROCESS TUBE FOR MANUFACTURING SEMICONDUCTOR WAFERS OR THE LIKE**

(75) Inventor: **Hirofumi Kaneko**, Tokyo (JP)

(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/264,779**

(22) Filed: **Aug. 18, 2006**

(30) **Foreign Application Priority Data**

Feb. 20, 2006 (JP) 2006-003838

(51) **LOC (9) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Classification Search** D13/182; 117/102; 118/715, 724, 725; 219/390, 486
See application file for complete search history.

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Primary Examiner—Selina Sikder
(74) *Attorney, Agent, or Firm*—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

(57) **CLAIM**

The ornamental design for a process tube for manufacturing semiconductor wafers or the like, as shown and described.

DESCRIPTION

FIG. **1** is a front elevational view of the process tube for manufacturing semiconductor wafers or the like, showing my new design;

FIG. **2** is a rear elevational view thereof;

FIG. **3** is a top plan view thereof;

FIG. **4** is a bottom plan view thereof;

FIG. **5** is a right side elevational view thereof,

FIG. **6** is a left side elevational view thereof;

FIG. **7** is an enlarged cross-sectional view thereof taken along line **7**—**7** in FIG. **3**

FIG. **8** is an enlarged cross-sectional view thereof taken along line **8**—**8** in FIG. **3**

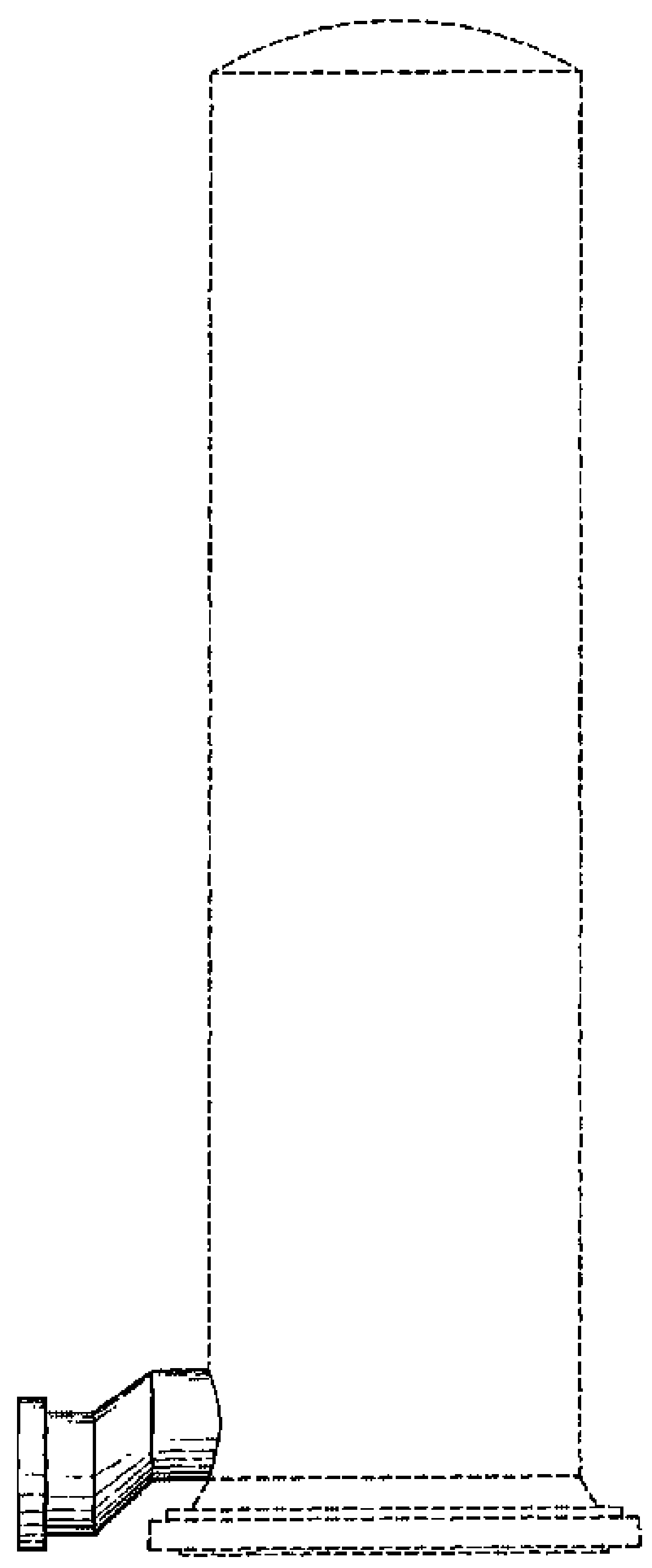
FIG. **9** is an enlarged cross-sectional view thereof taken along line **9**—**9** in FIG. **3**

FIG. **10** is a vertical cross-sectional view thereof taken along line **10**—**10** in FIG. **3**; and,

FIG. **11** is a bottom and right side perspective view thereof shown on reduced scale.

The broken line showing in the figures is for illustrative purposes only and forms no part of the claimed design.

1 Claim, 9 Drawing Sheets



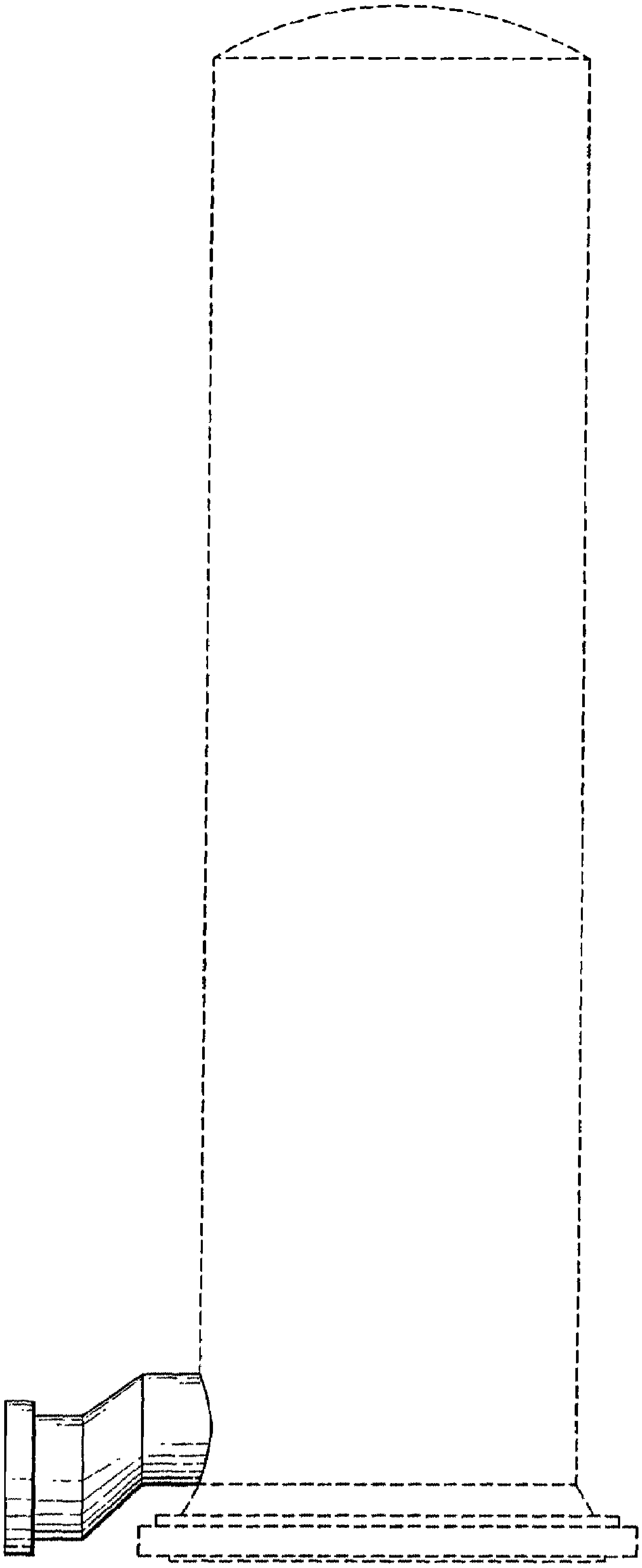


Fig. 1

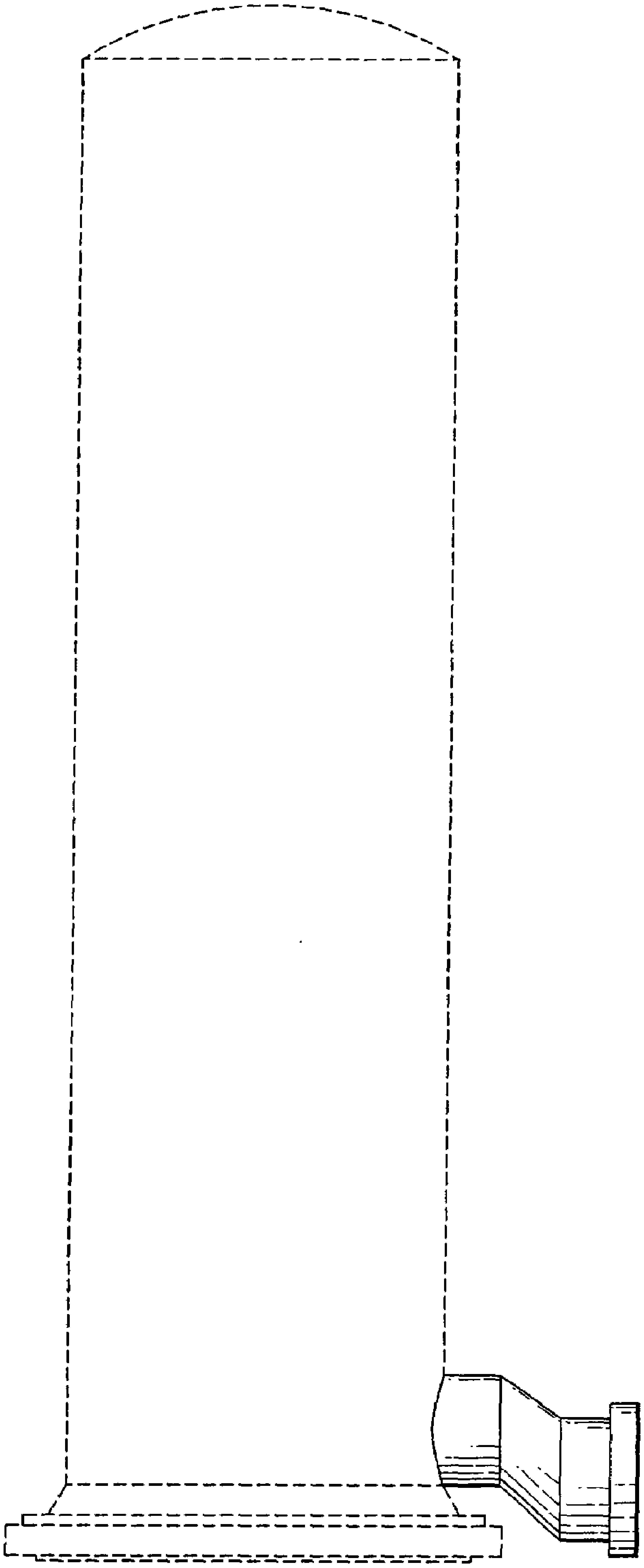


Fig.2

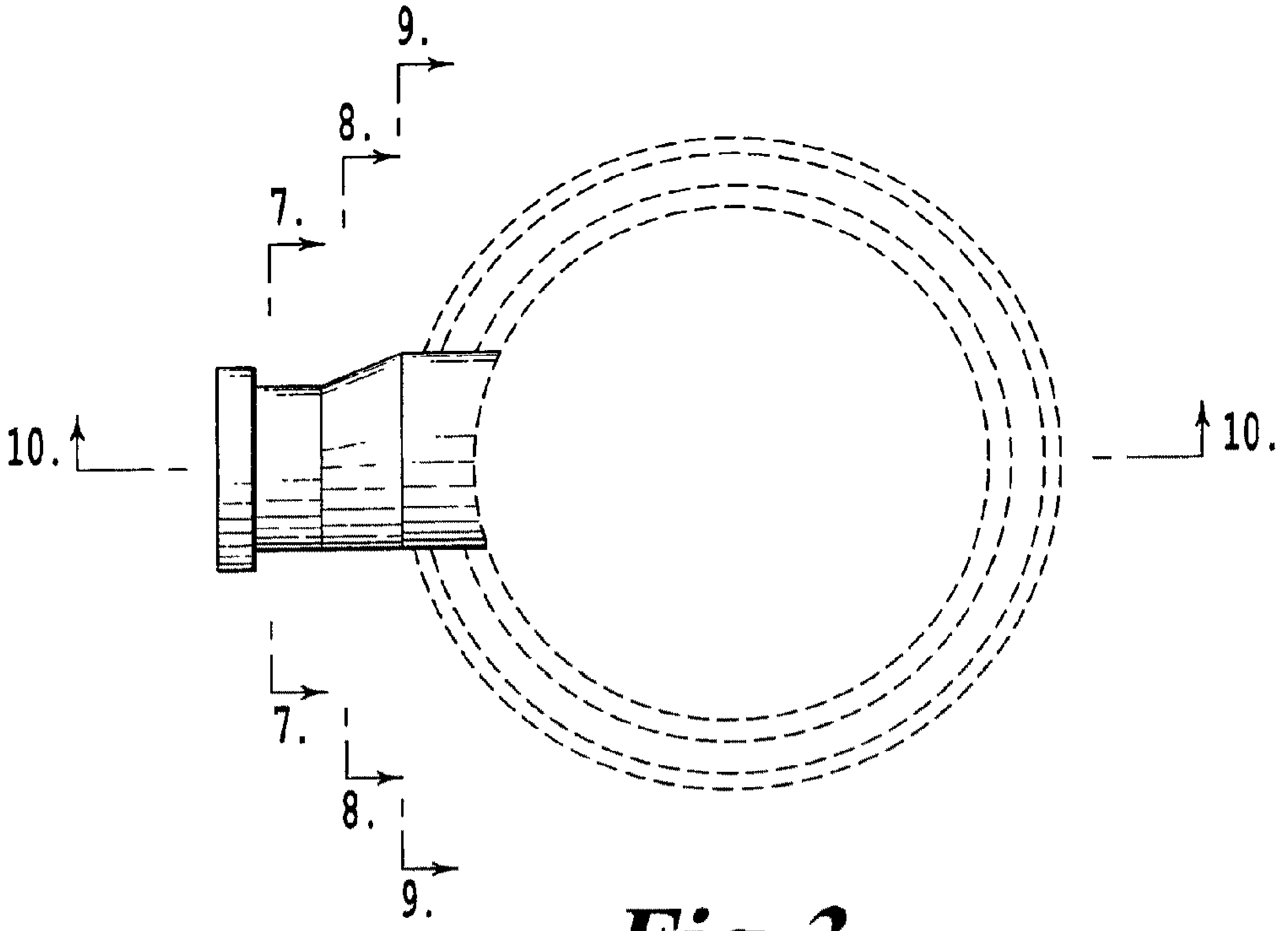


Fig.3

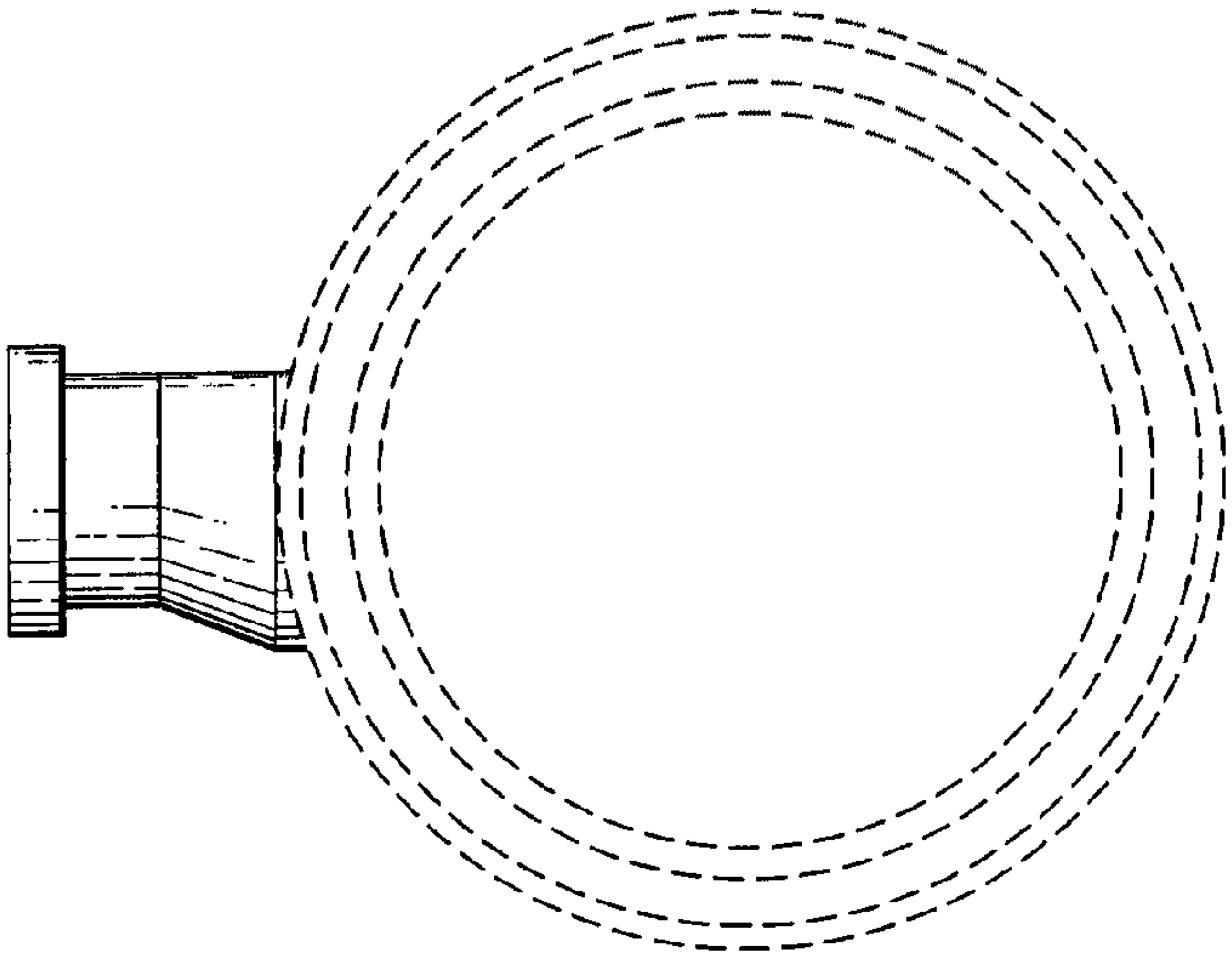


Fig.4

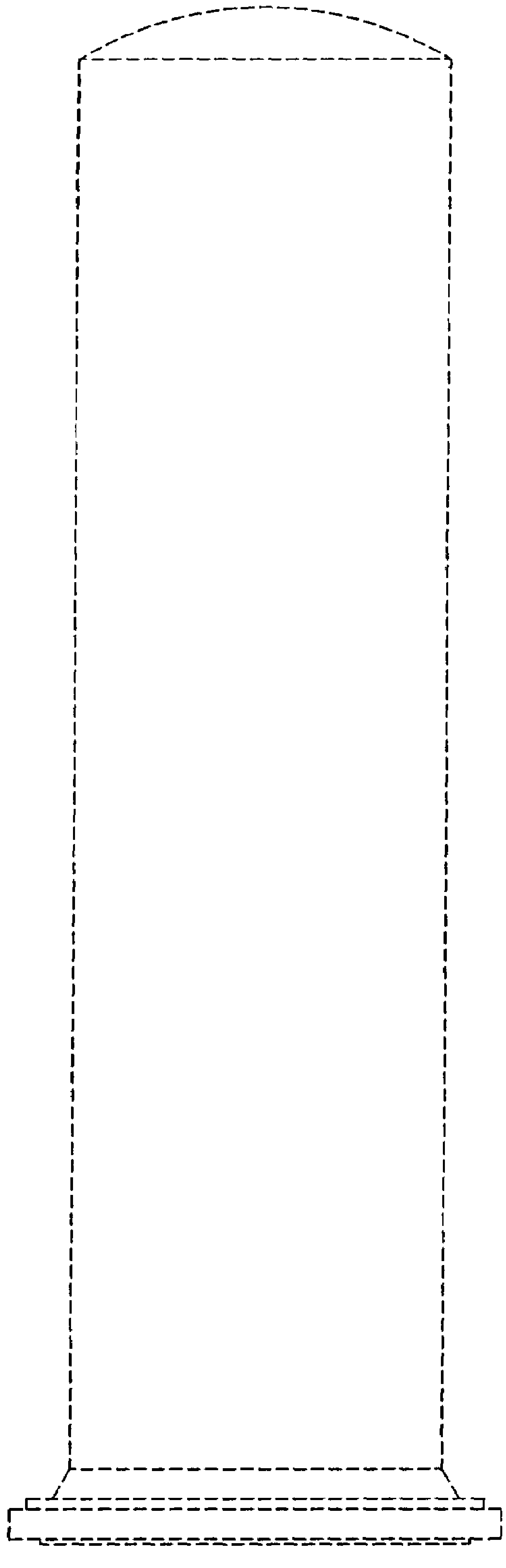


Fig.5

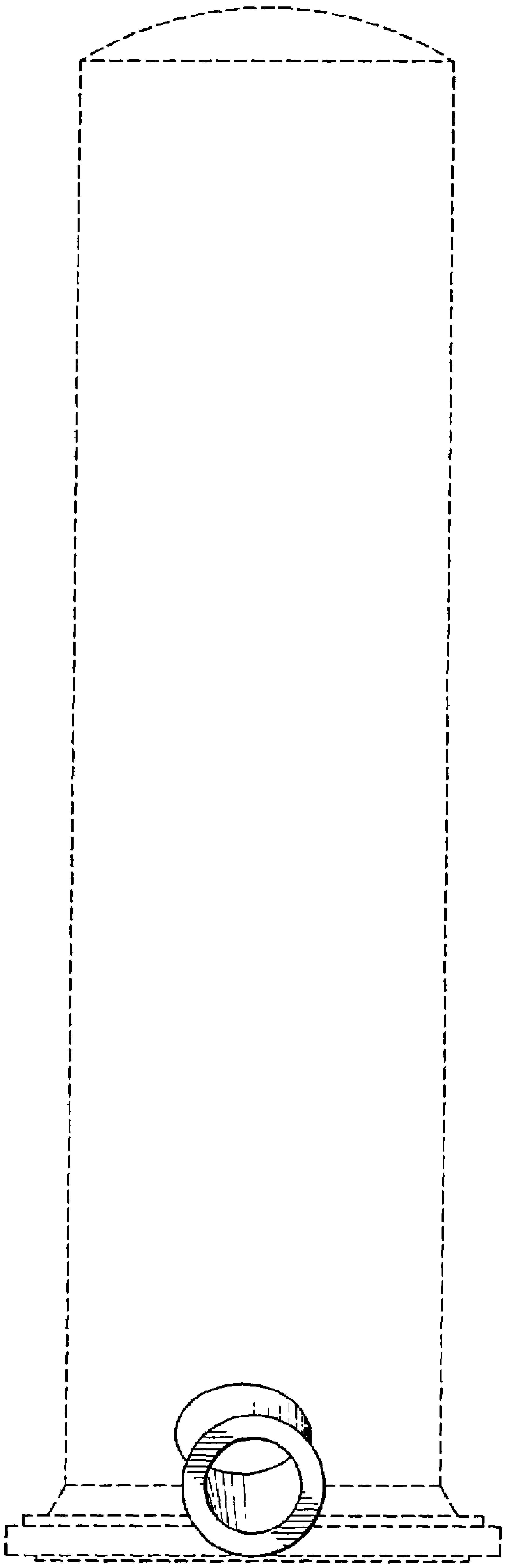


Fig. 6

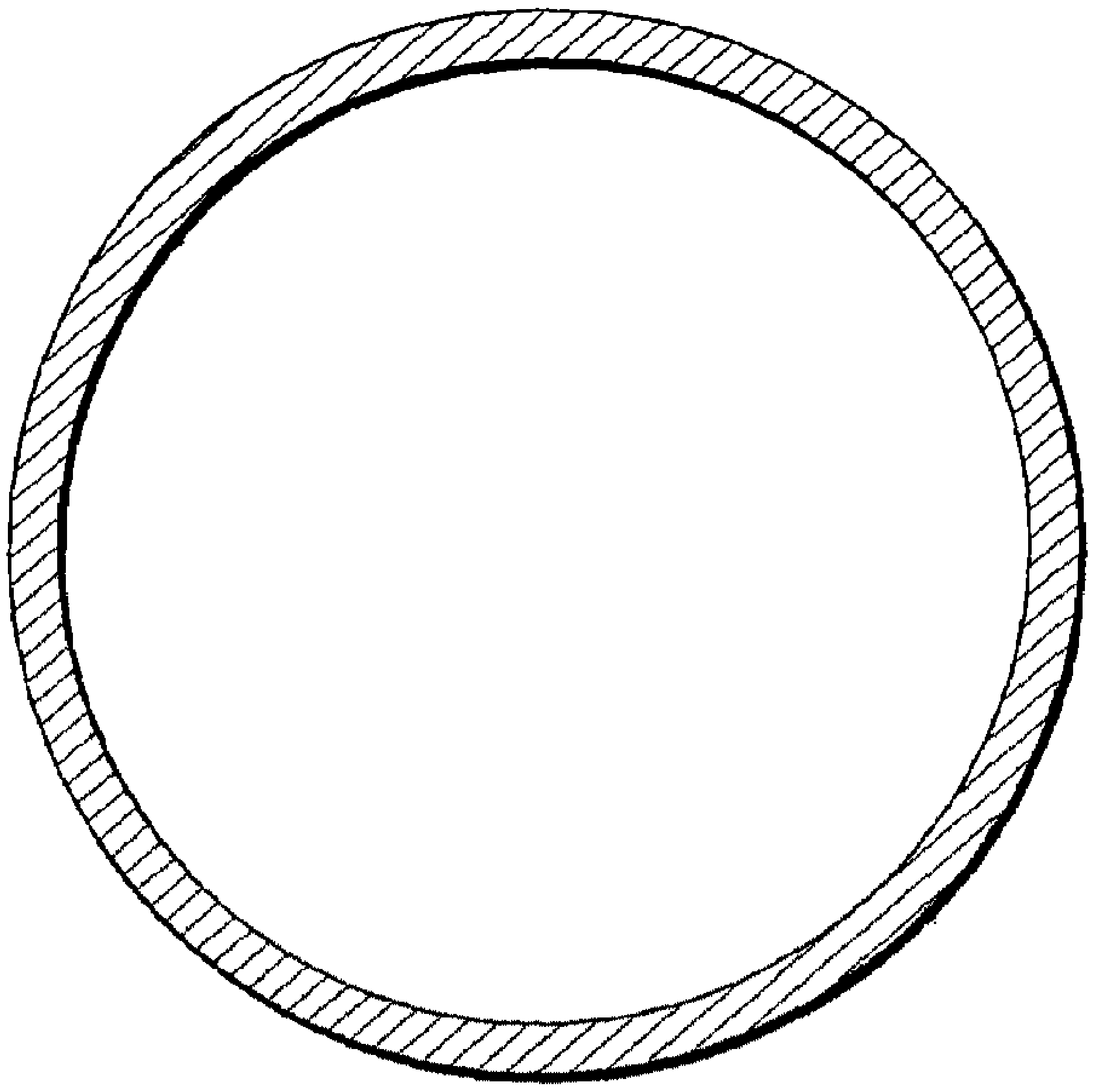


Fig. 7

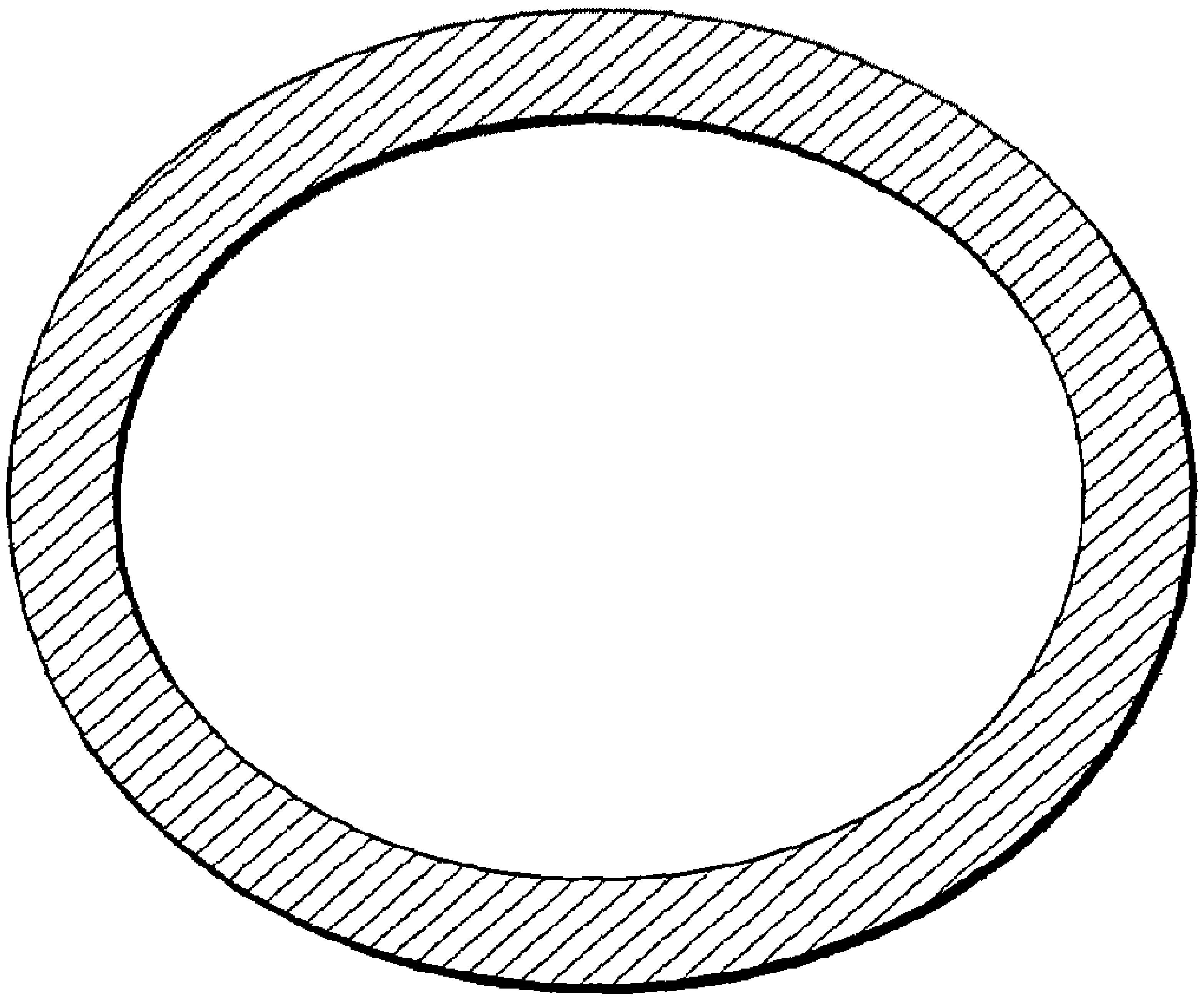


Fig. 8

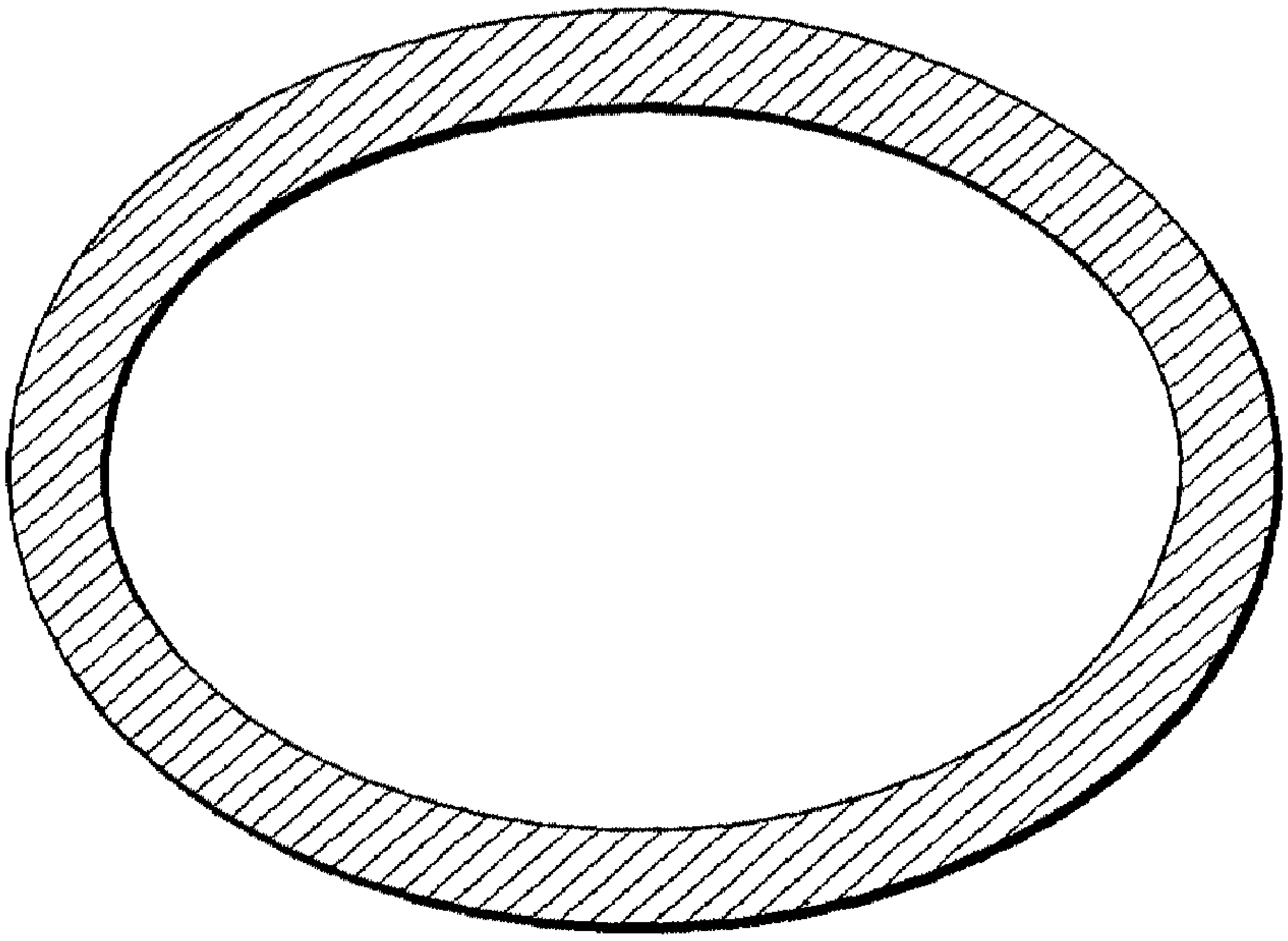


Fig. 9

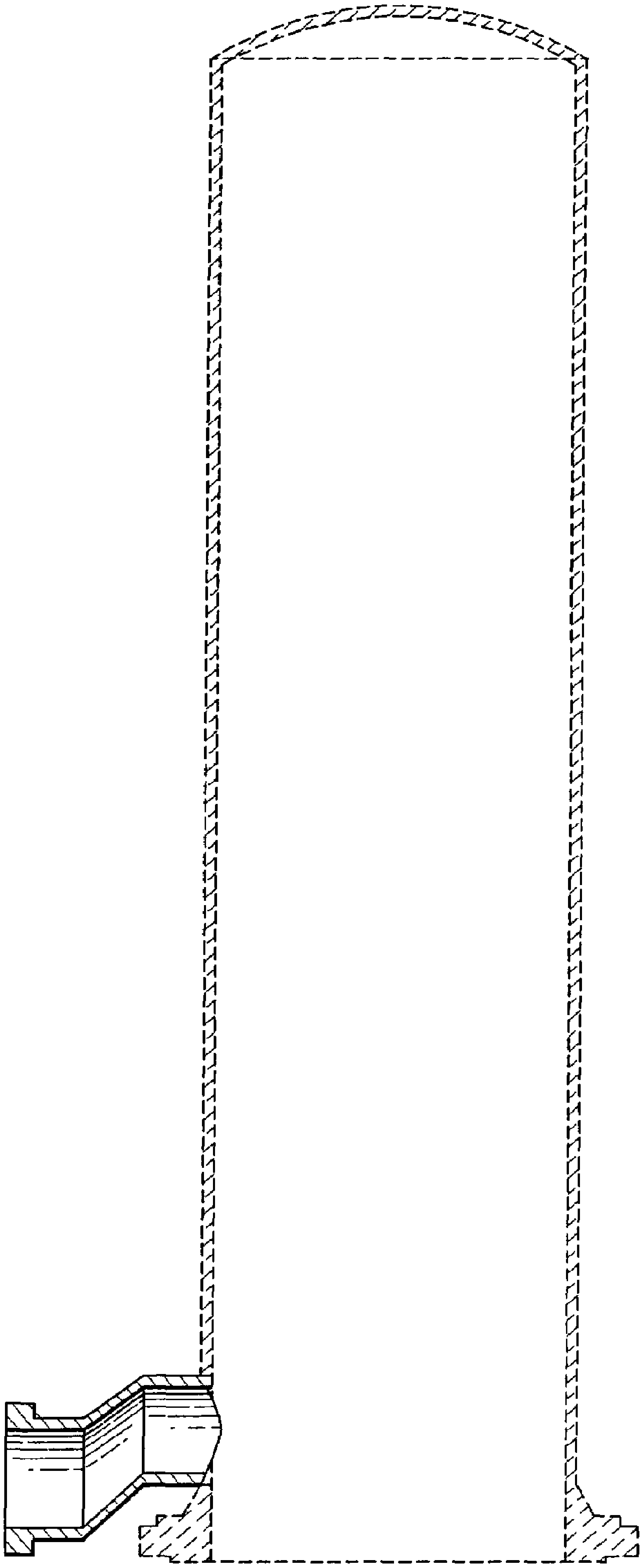


Fig. 10

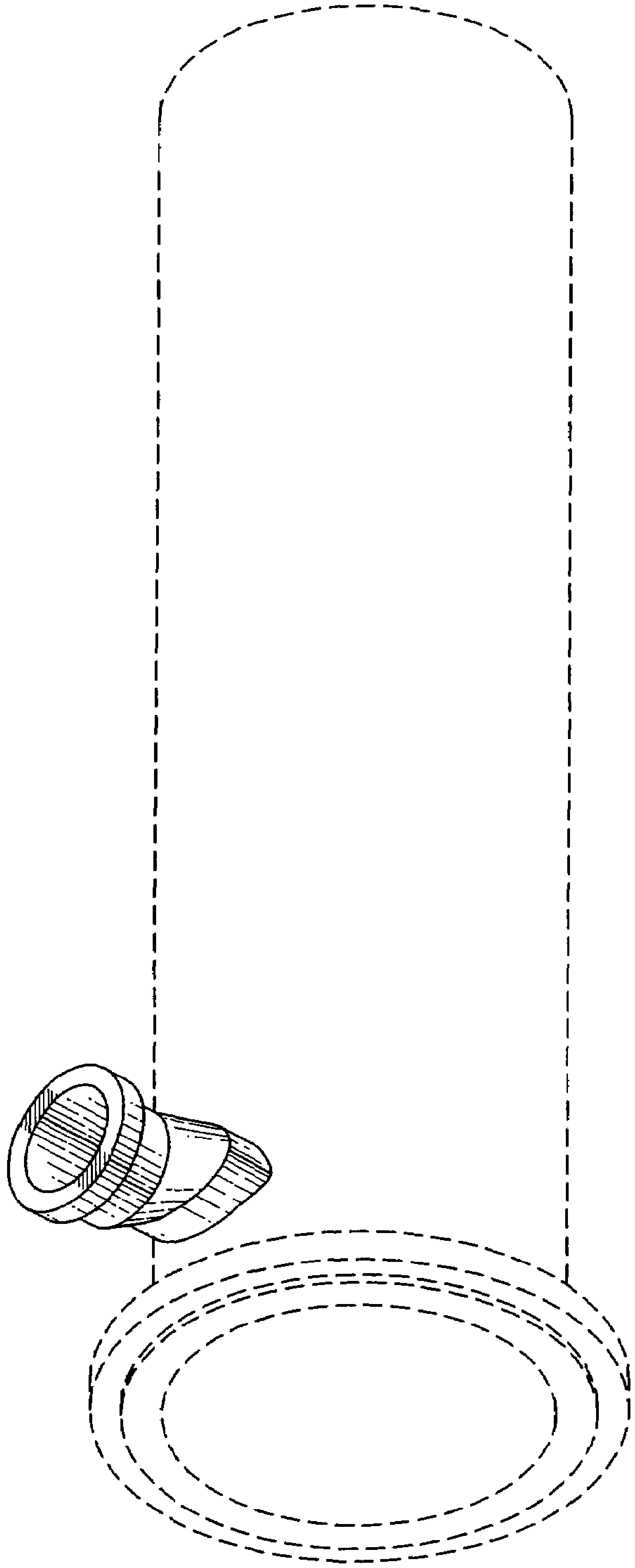


Fig. 11