



US00D589011S

(12) **United States Design Patent**
Di Stefano

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(54) **TRAY FOR SEMICONDUCTOR DEVICES WITH CASTELLATIONS**

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(**) Term: **14 Years**

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(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
206/701, 706, 707, 710, 716, 724, 725
See application file for complete search history.

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(57) **CLAIM**

The ornamental design for tray for semiconductor devices with castellations, as shown and described.

DESCRIPTION

FIG. 1 is a perspective view of a tray for semiconductor devices with castellations showing my new design;

FIG. 2 is a top plan view thereof;

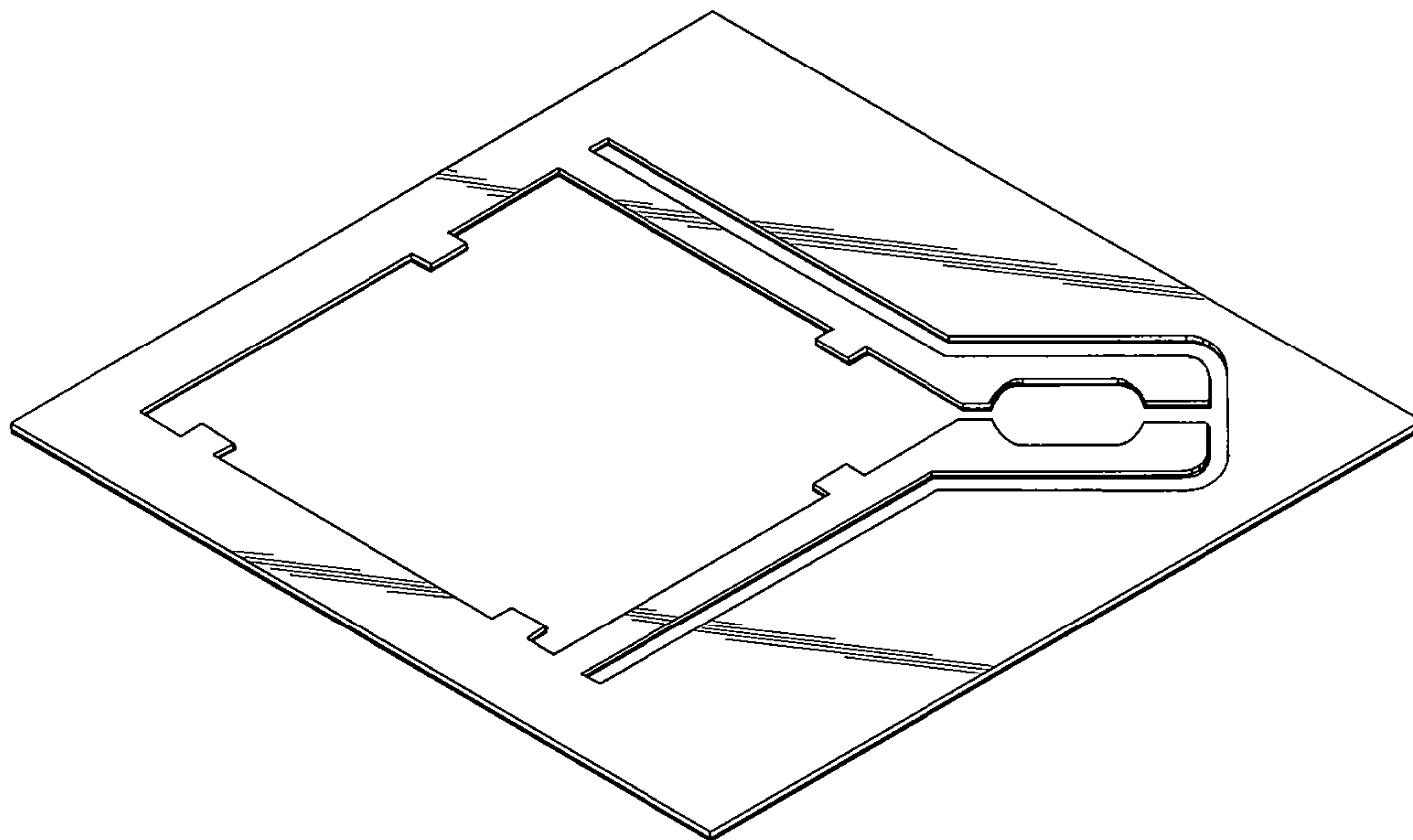
FIG. 3 is a front elevational view, the rear elevational view being a mirror image thereof;

FIG. 4 is a right side elevational view, the left side elevational view being a mirror image thereof; and,

FIG. 5 is a bottom plan view thereof.

The broken line showing of the environment is for illustrative purposes only and forms no part of the claimed design.

1 Claim, 1 Drawing Sheet



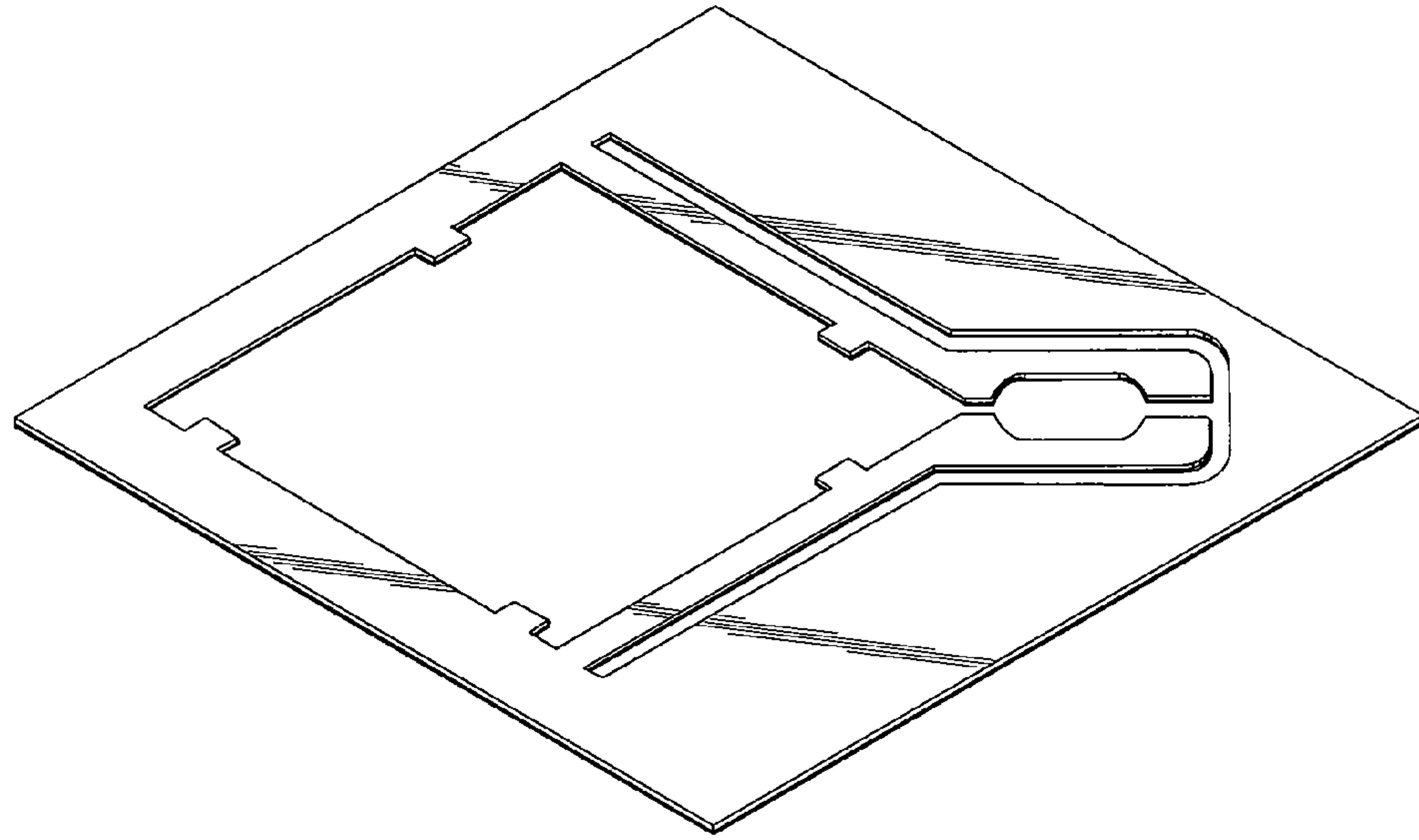


FIG. 1

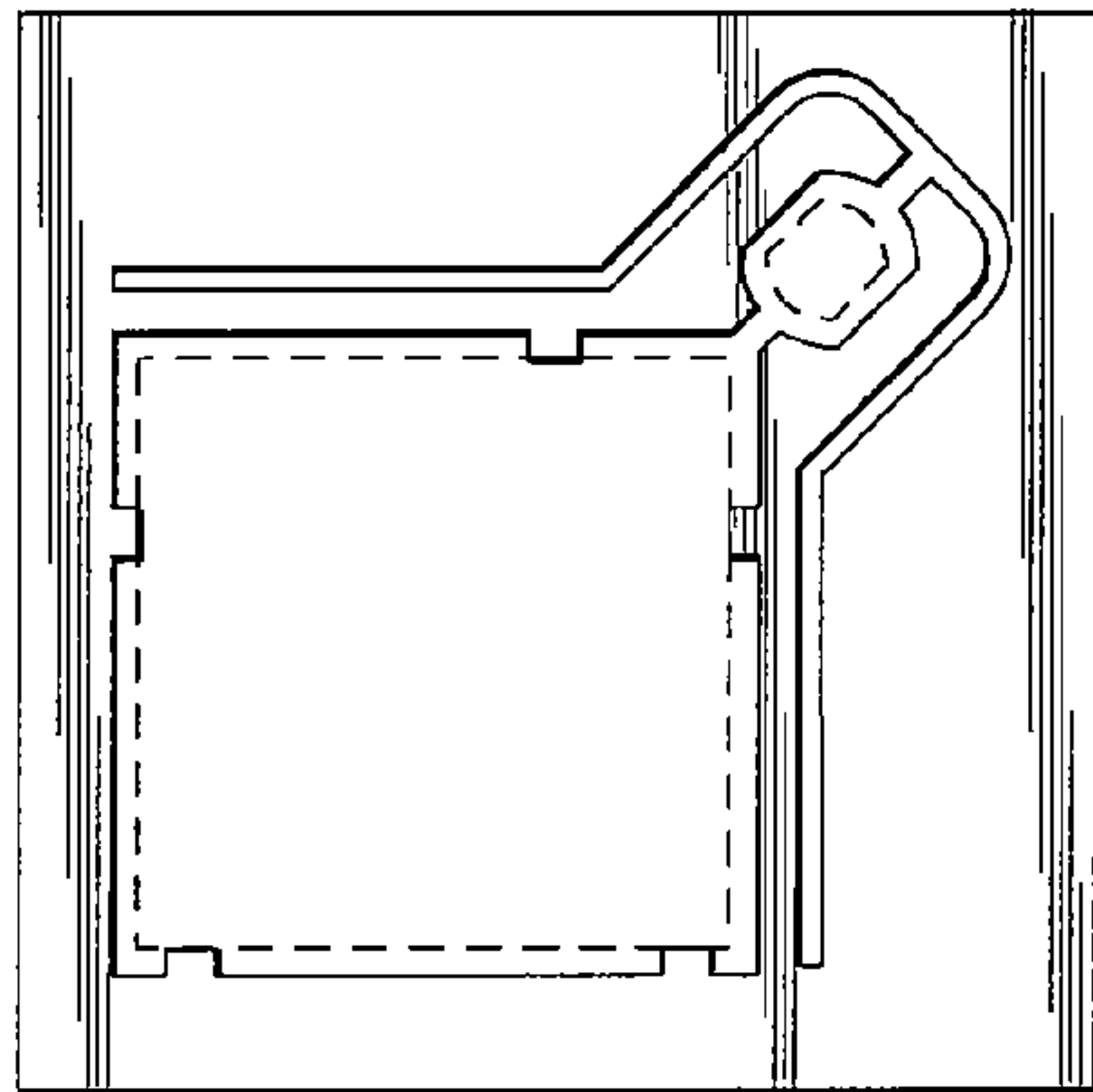


FIG. 2

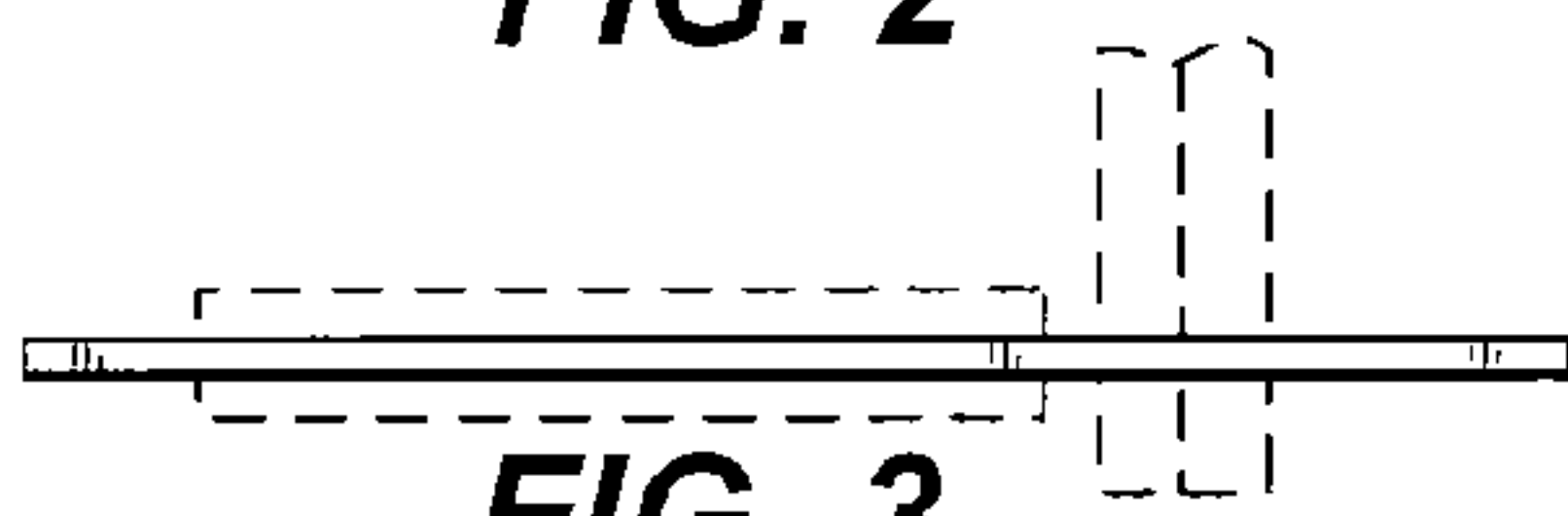


FIG. 3

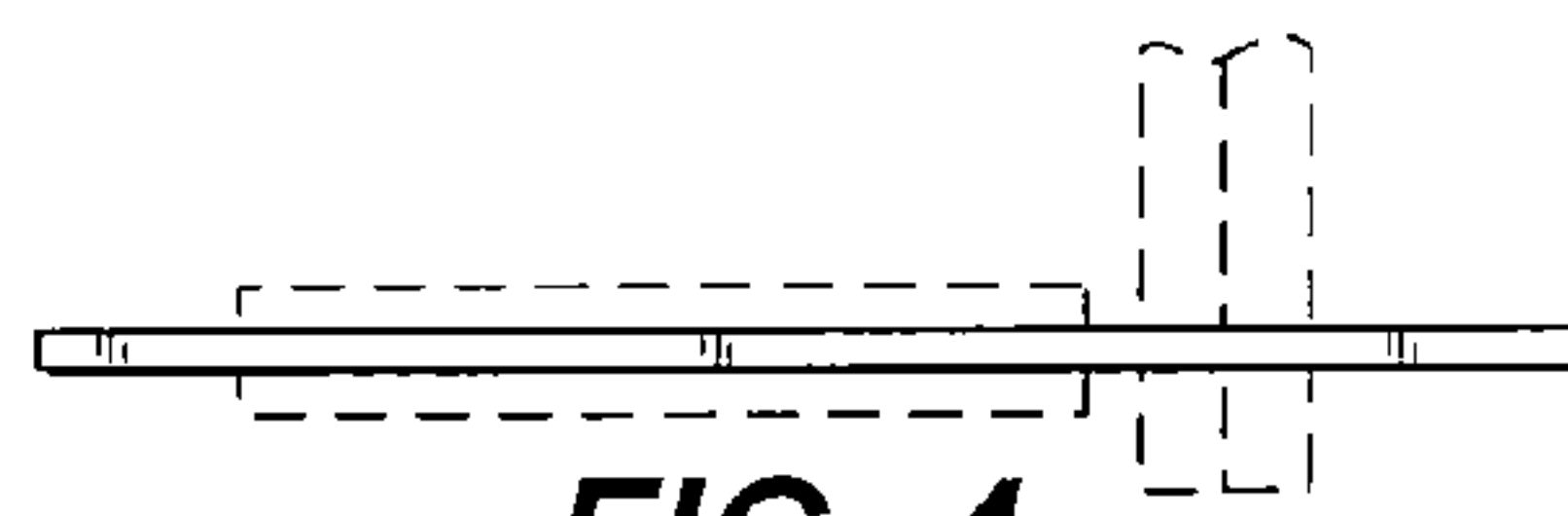


FIG. 4

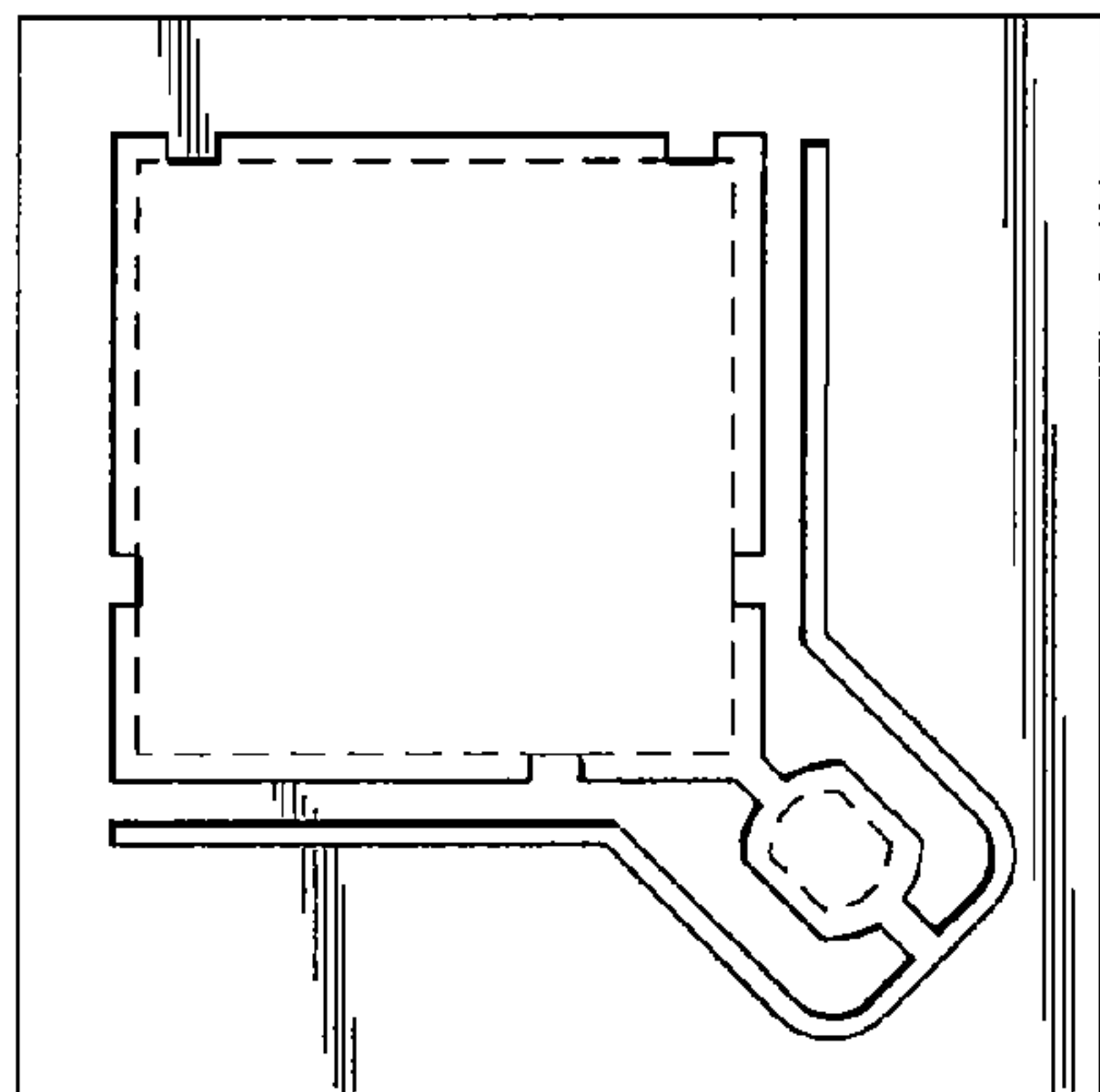


FIG. 5