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(12) **United States Design Patent**
Inoue et al.

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(54) **PROCESS TUBE FOR MANUFACTURING SEMICONDUCTOR WAFERS**

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(57) **CLAIM**

(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)

The ornamental design for a process tube for manufacturing semiconductor wafers, as shown and described.

(**) Term: **14 Years**

(21) Appl. No.: **29/274,293**

DESCRIPTION

(22) Filed: **Apr. 11, 2007**

(30) **Foreign Application Priority Data**

Oct. 12, 2006 (JP) 2006-027524

(51) **LOC (9) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
118/715, 724, 725; 219/390, 486, 523; 432/247
See application file for complete search history.

FIG. 1 is a front view of the design for a process tube for manufacturing semiconductor wafers in accordance with the invention;

FIG. 2 is a rear view thereof;

FIG. 3 is a right side view thereof;

FIG. 4 is a left side view thereof;

FIG. 5 is a top view thereof;

FIG. 6 is a bottom view thereof;

FIG. 7 is a sectional view thereof along line 7—7 of FIG. 5;

FIG. 8 is a sectional view thereof along line 8—8 of FIG. 5;

FIG. 9 is a sectional view thereof along line 9—9 of FIG. 1; and,

FIG. 10 is a front, perspective view thereof.

In the preferred embodiment, the entire body of the process tube is transparent such that the inside of the tube can be seen. Dash lines show the boundary of the claimed design.

The broken lines define portions of the process tube that form no part of the claimed design.

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1 Claim, 5 Drawing Sheets

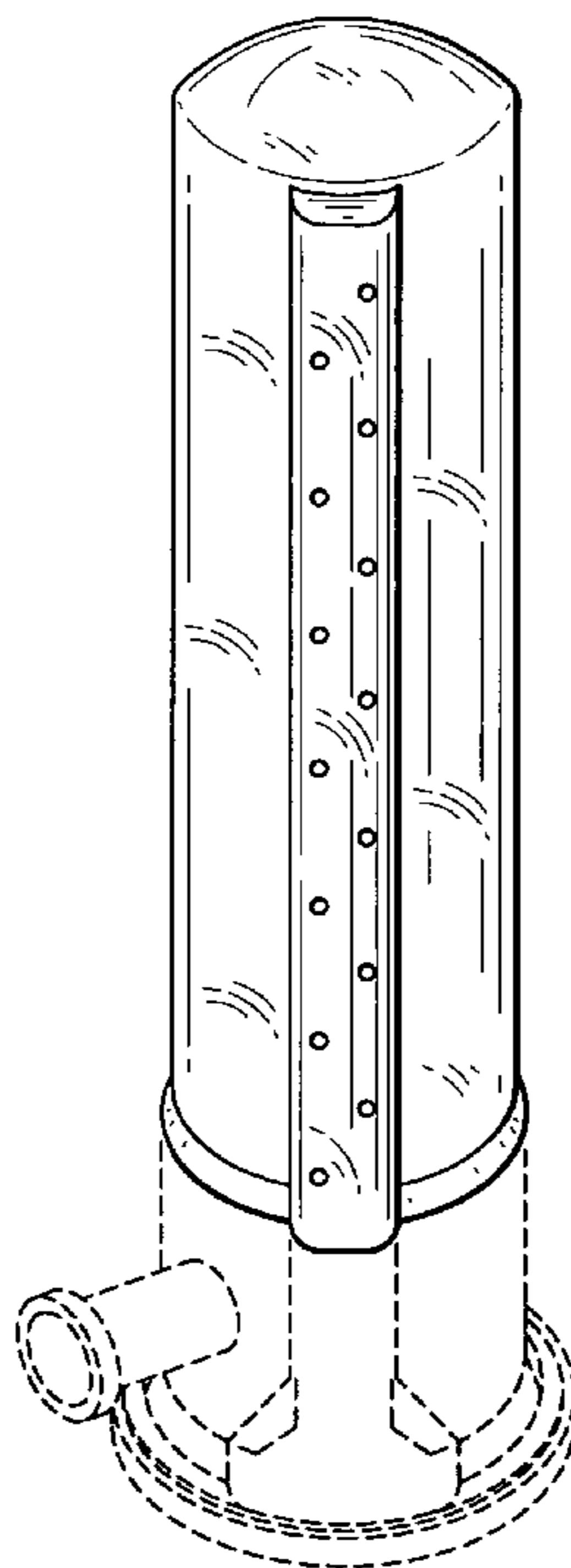


FIG. 1

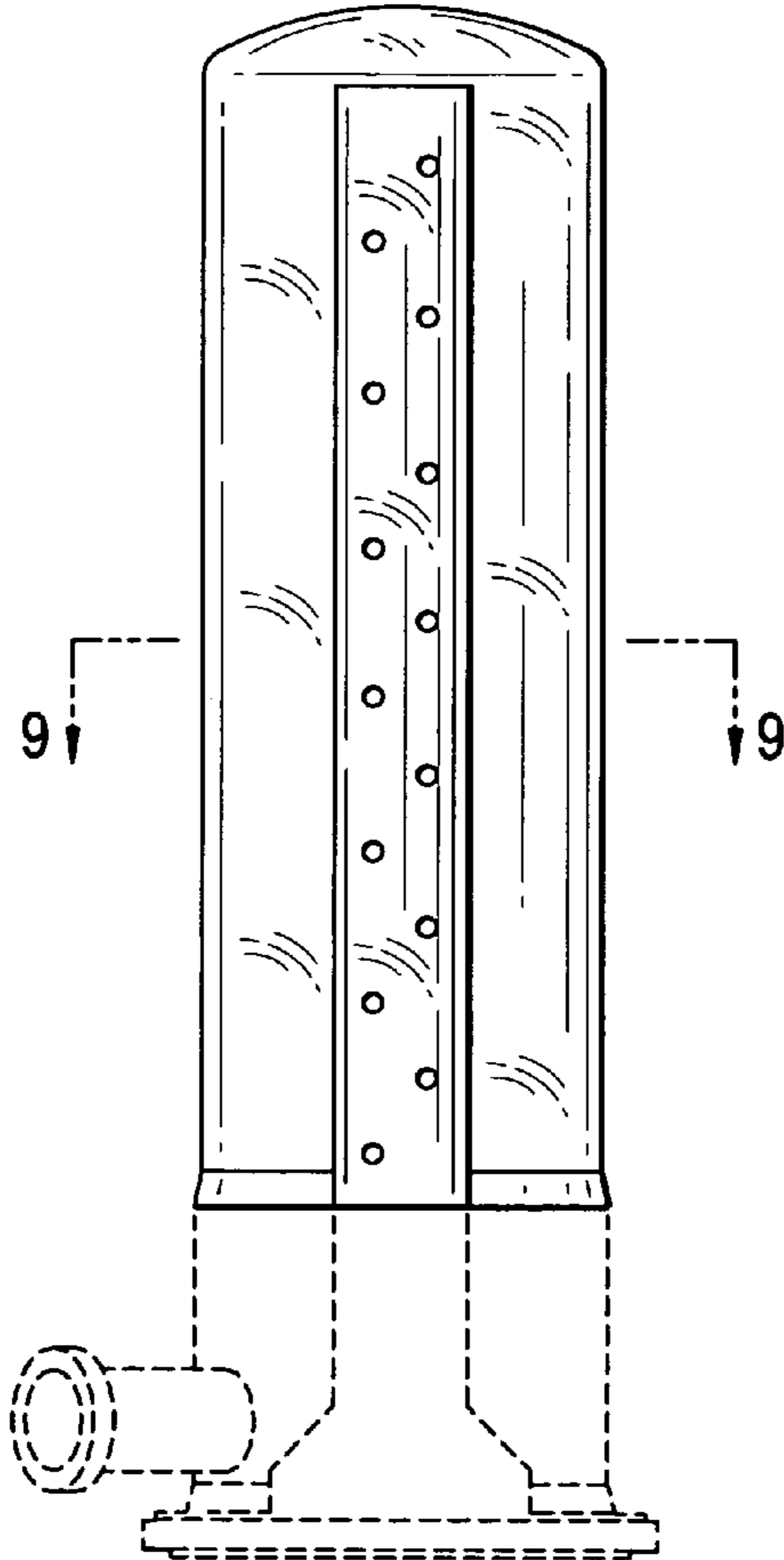


FIG. 2

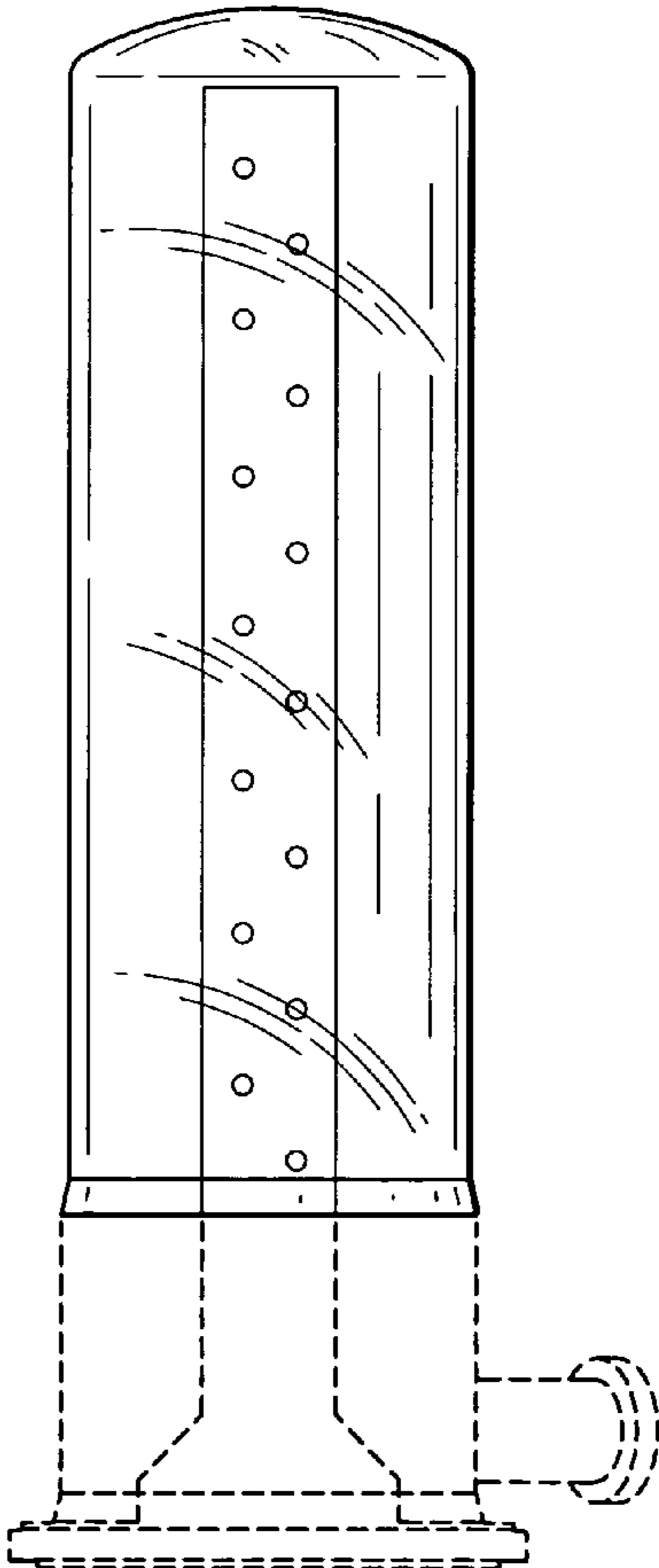


FIG. 3

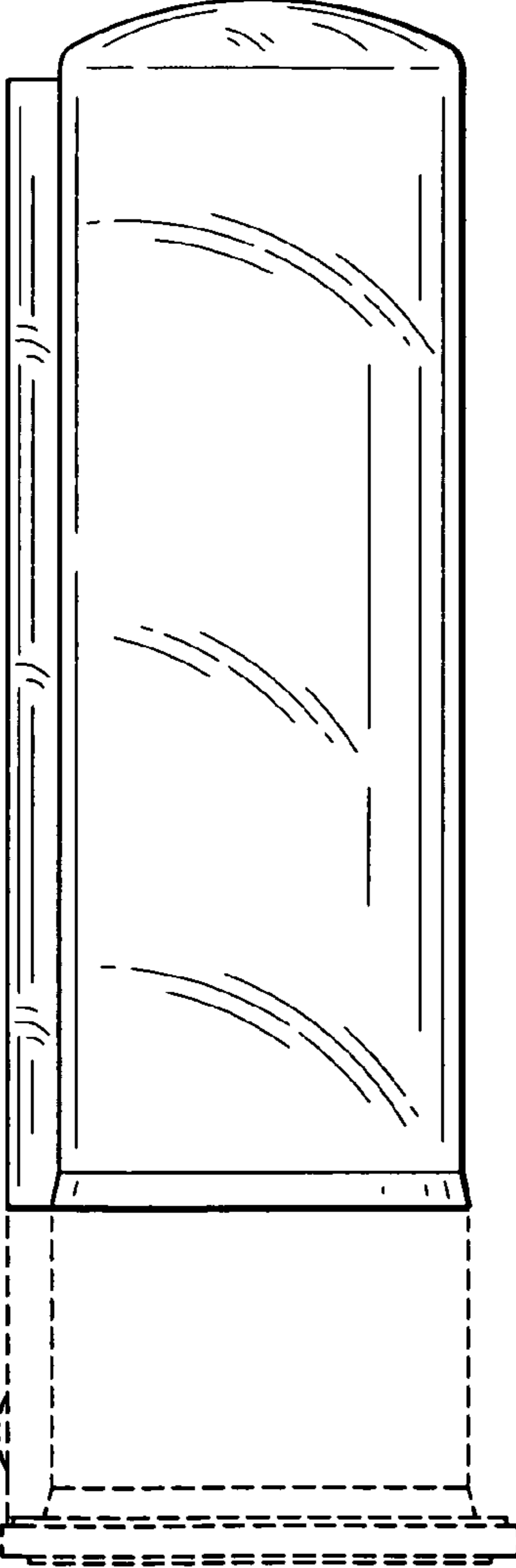


FIG. 4



FIG. 5

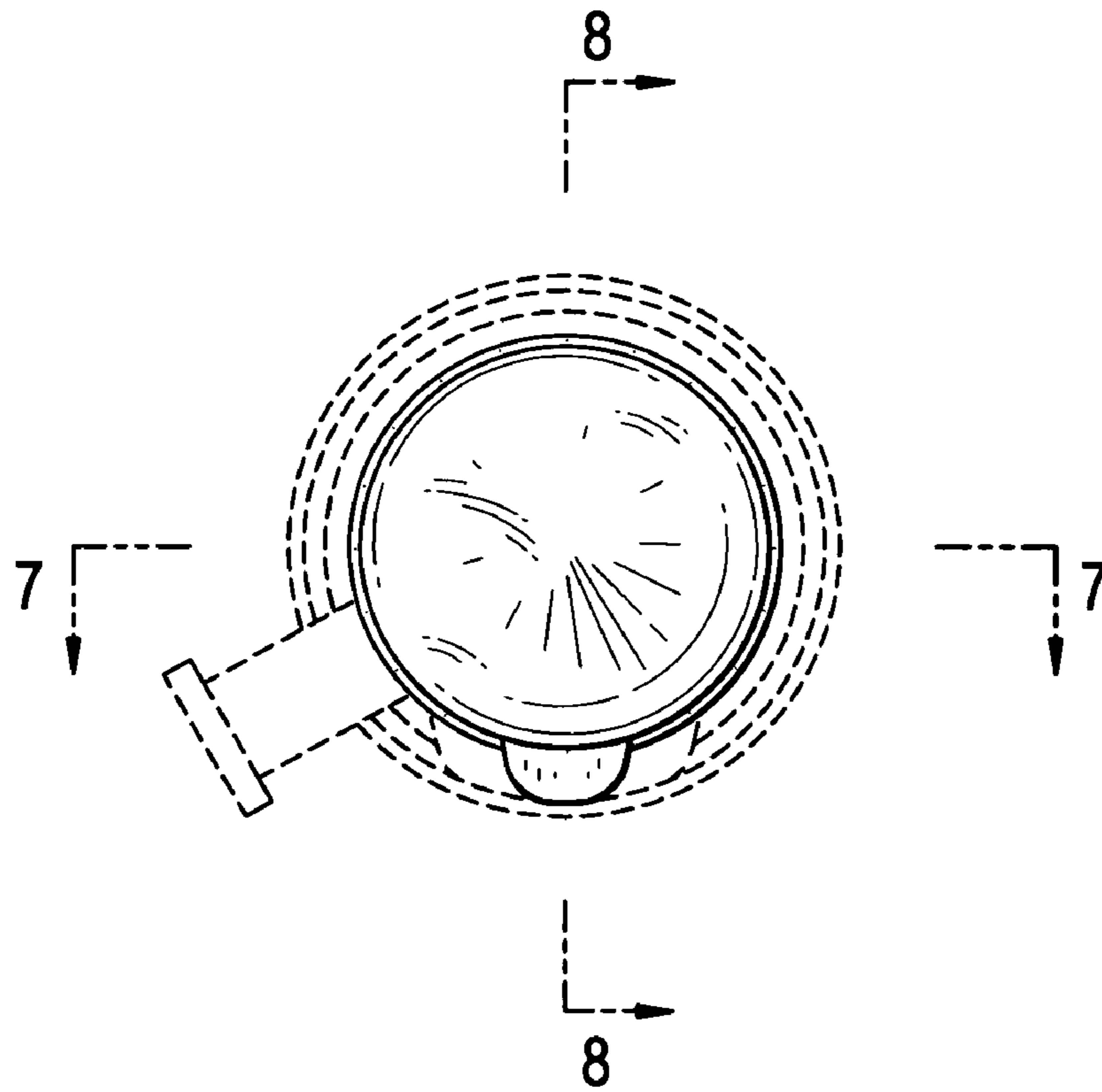


FIG. 6

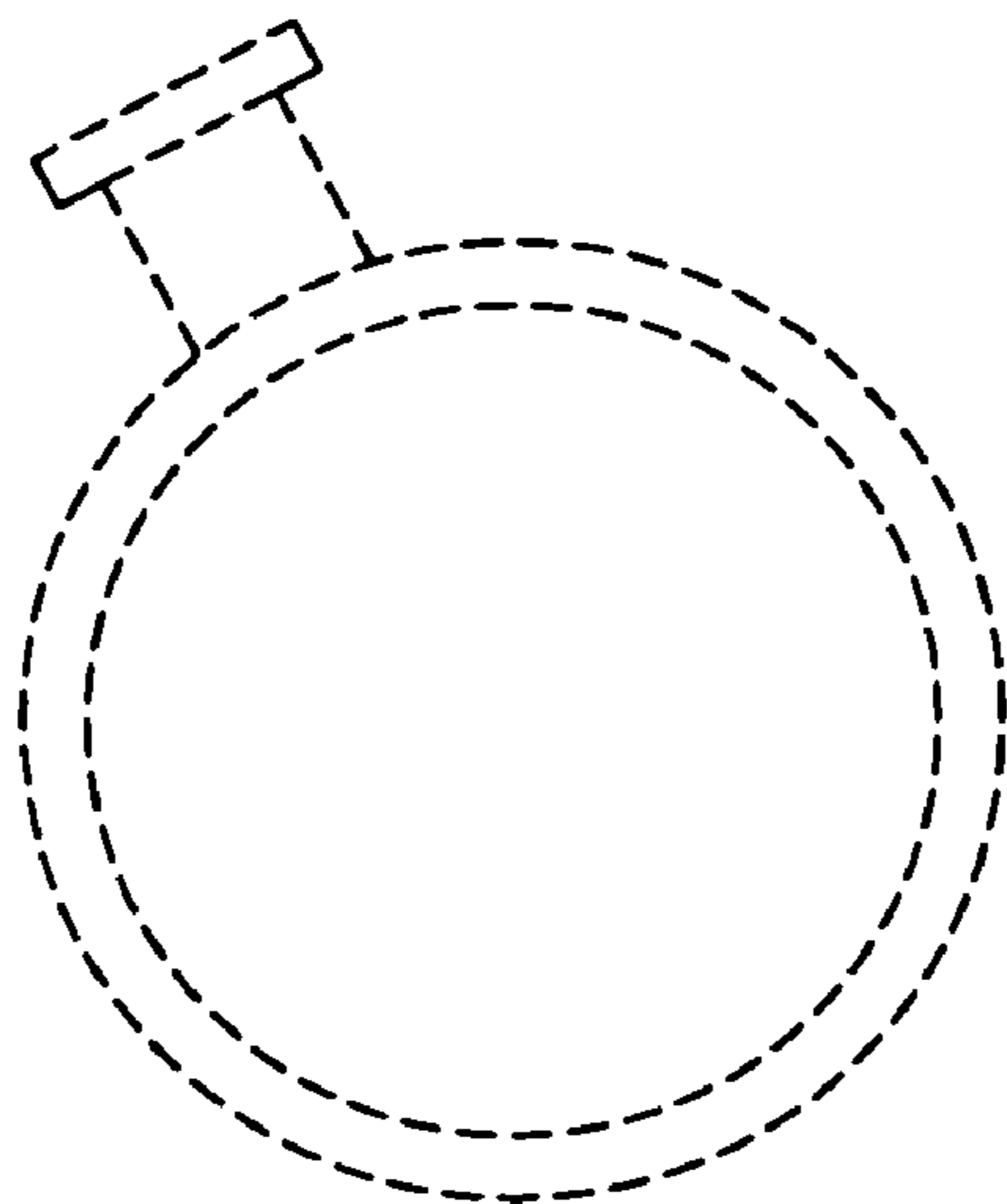


FIG. 7

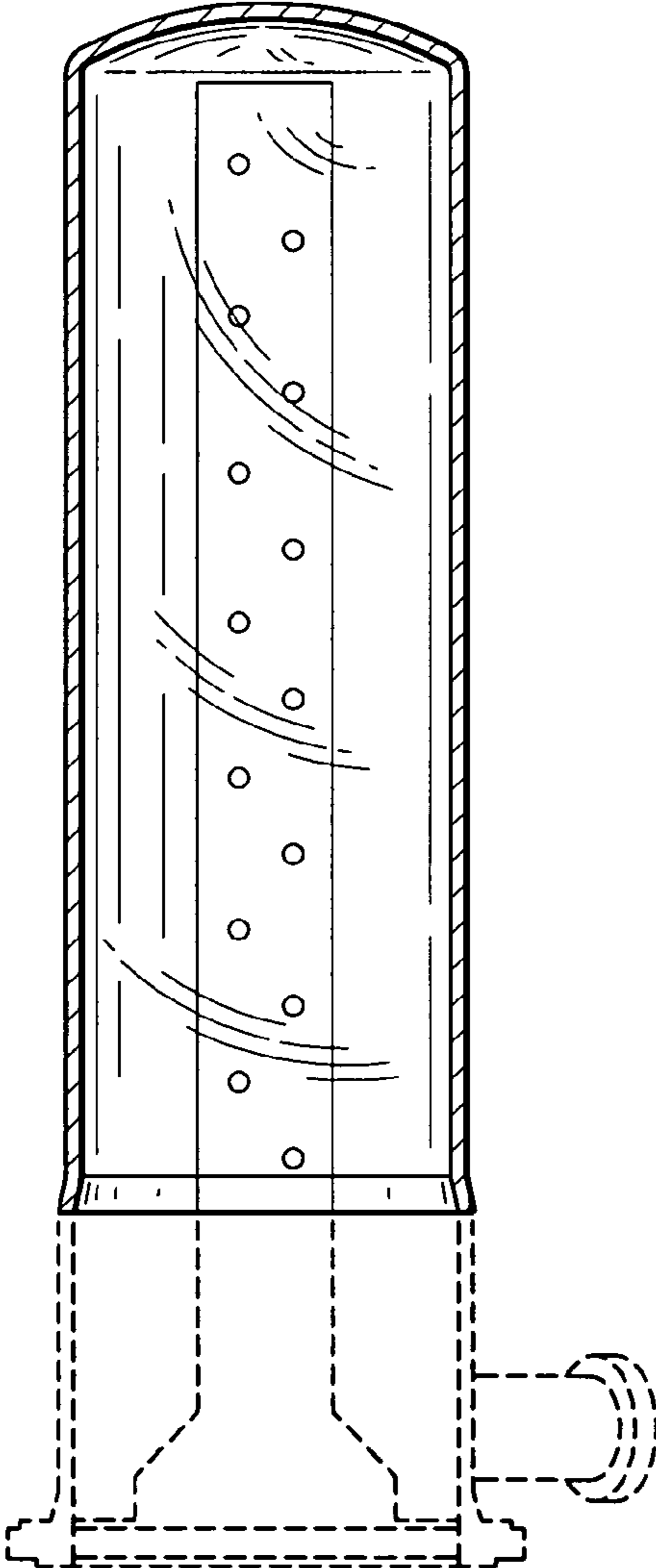


FIG. 8

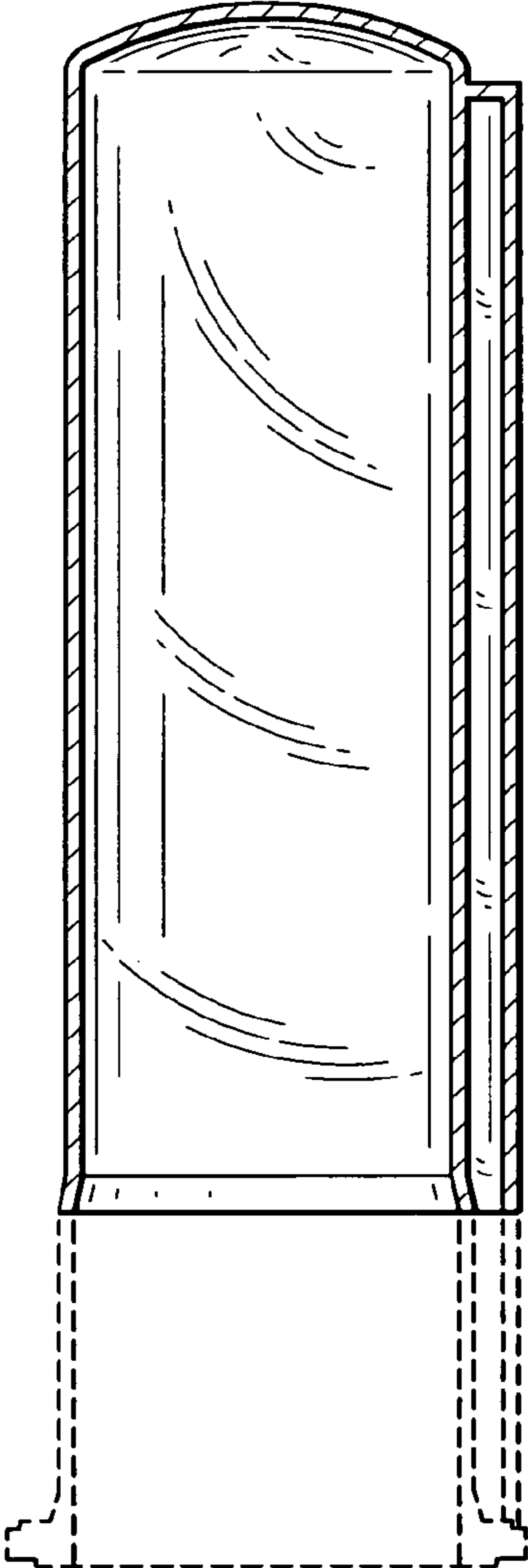


FIG. 9

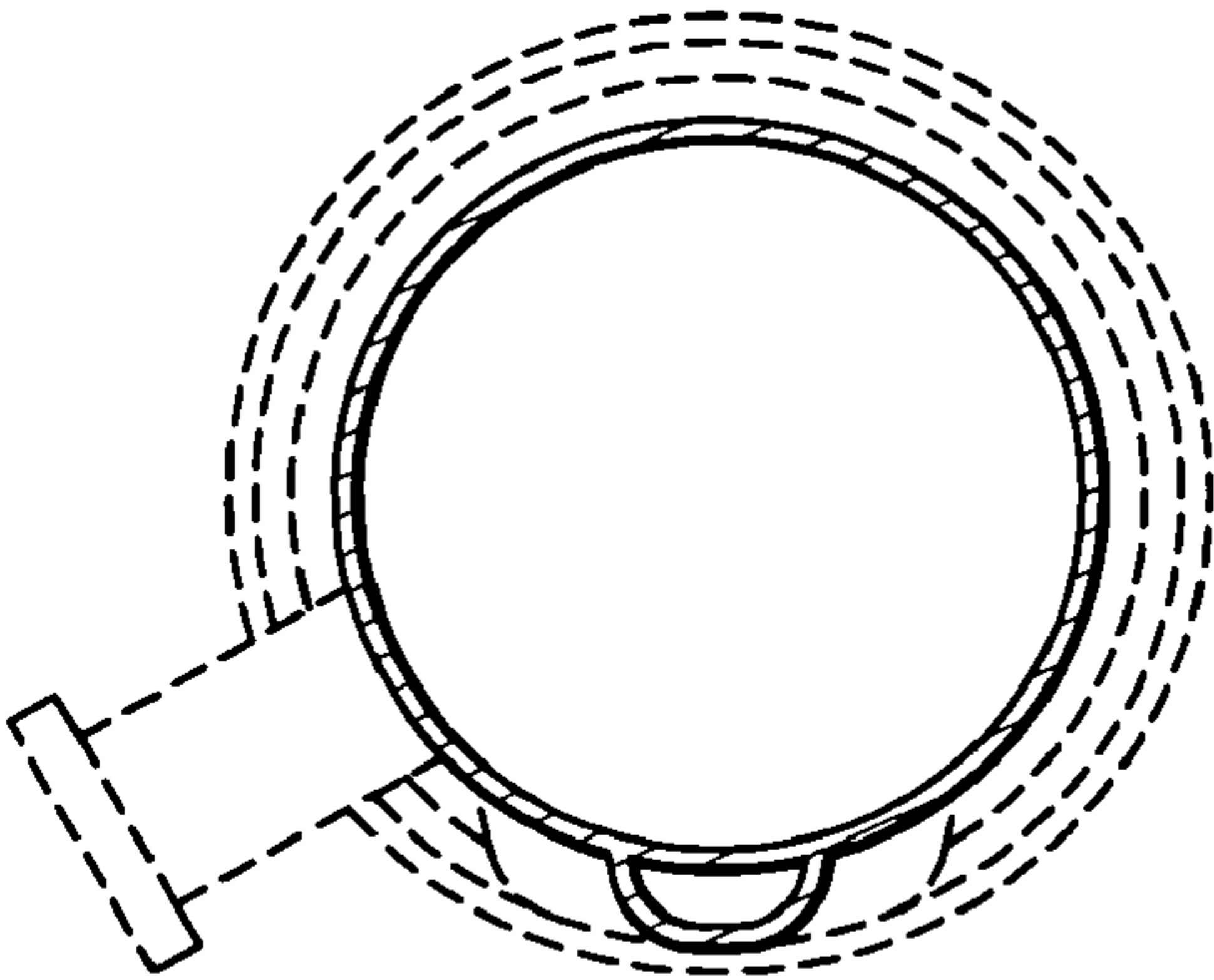


FIG. 10

