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(12) **United States Design Patent**  
**Tani et al.**

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(54) **GROOVES FORMED AROUND A SEMICONDUCTOR DEVICE ON A CIRCUIT BOARD**

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(\*\*) Term: **14 Years**

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**Related U.S. Application Data**

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(30) **Foreign Application Priority Data**

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May 1, 2006 (JP) ..... 2006-011446

(51) **LOC (9) Cl.** ..... **13-03**

(52) **U.S. Cl.** ..... **D13/182**

(58) **Field of Classification Search** ..... D13/182;  
174/250, 251, 253, 254, 255, 256, 265, 260,  
174/261; 361/760, 748, 720; 336/200  
See application file for complete search history.

(56) **References Cited**

**U.S. PATENT DOCUMENTS**

D319,629 S \* 9/1991 Hasegawa et al. .... D13/182  
5,420,558 A \* 5/1995 Ito et al. .... 336/200  
5,467,252 A \* 11/1995 Nomi et al. .... 361/760  
5,777,277 A \* 7/1998 Inagawa ..... 174/265

5,969,590 A \* 10/1999 Gutierrez ..... 336/200  
6,114,937 A \* 9/2000 Burghartz et al. .... 336/200  
6,121,552 A \* 9/2000 Brosnihan et al. .... 174/253  
6,486,412 B2 \* 11/2002 Kato ..... 174/260  
7,126,452 B2 \* 10/2006 Teshima et al. .... 336/200  
D566,060 S \* 4/2008 Ohsawa et al. .... D13/182  
D567,774 S \* 4/2008 Tani et al. .... D13/182  
D568,836 S \* 5/2008 Ohsawa et al. .... D13/182  
D568,838 S \* 5/2008 Terada et al. .... D13/182  
2006/0266545 A1 \* 11/2006 Takeuchi et al. .... 174/251  
2007/0188287 A1 \* 8/2007 Lien et al. .... 336/200  
2007/0205856 A1 \* 9/2007 Matsunaga et al. .... 336/200

\* cited by examiner

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(57) **CLAIM**

The ornamental design for grooves formed around a semiconductor device on a circuit board, as shown and described.

**DESCRIPTION**

FIG. 1 shows a plan view of the grooves formed around a semiconductor device on a circuit board showing the design according to the invention.

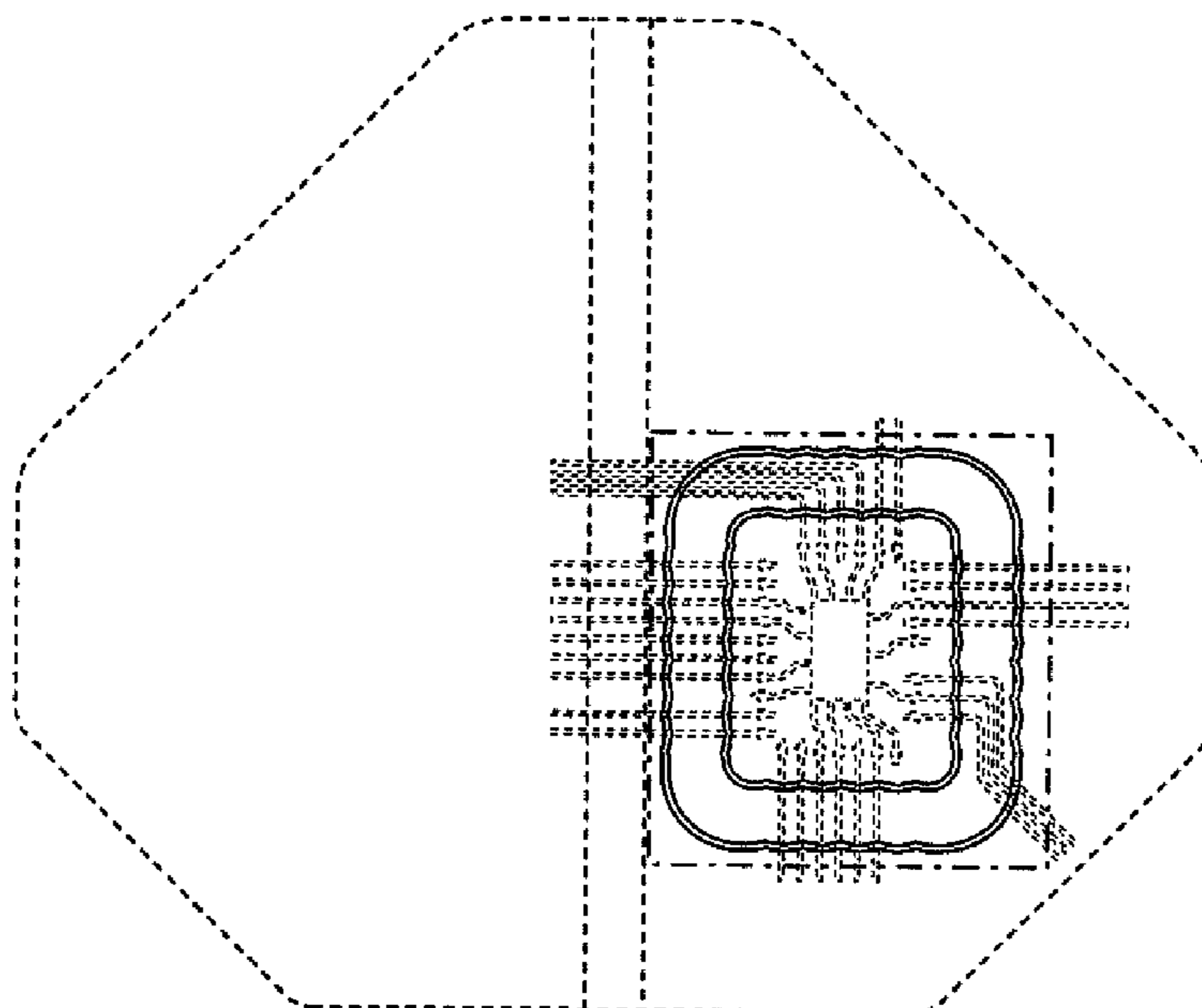
FIG. 2 shows an enlarged view of a claimed portion as identified by the area boxed by the dash-dot-dash line in FIG. 1.

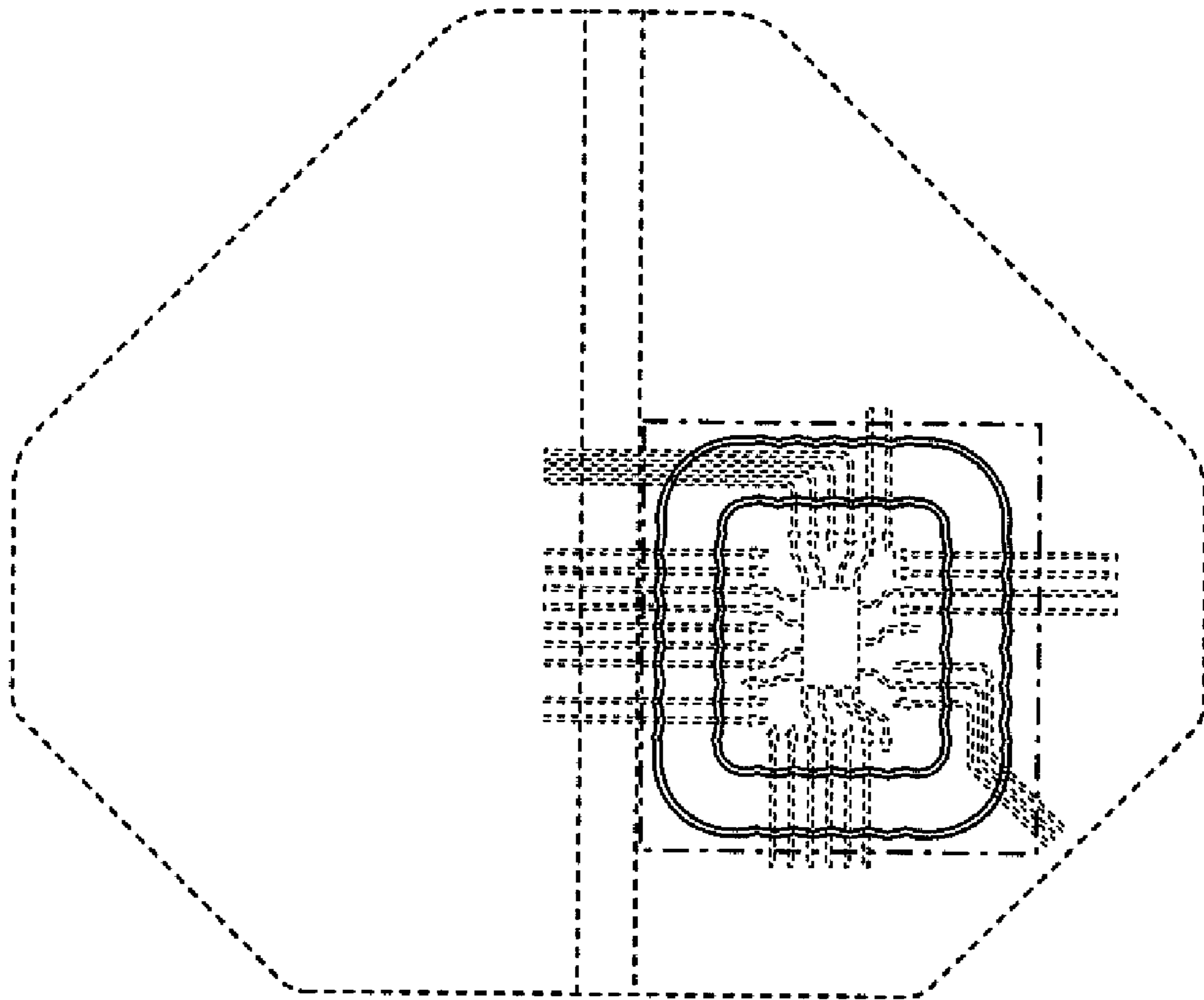
FIG. 3 shows an enlarged sectional view along the line 3—3 in FIG. 2; and,

FIG. 4 shows an enlarged sectional view along the line 4—4 in FIG. 2.

The elements shown in broken lines and dash-dot-dash lines are for illustrative purposes only and form no part of the claimed invention.

**1 Claim, 2 Drawing Sheets**





**FIG. 1**

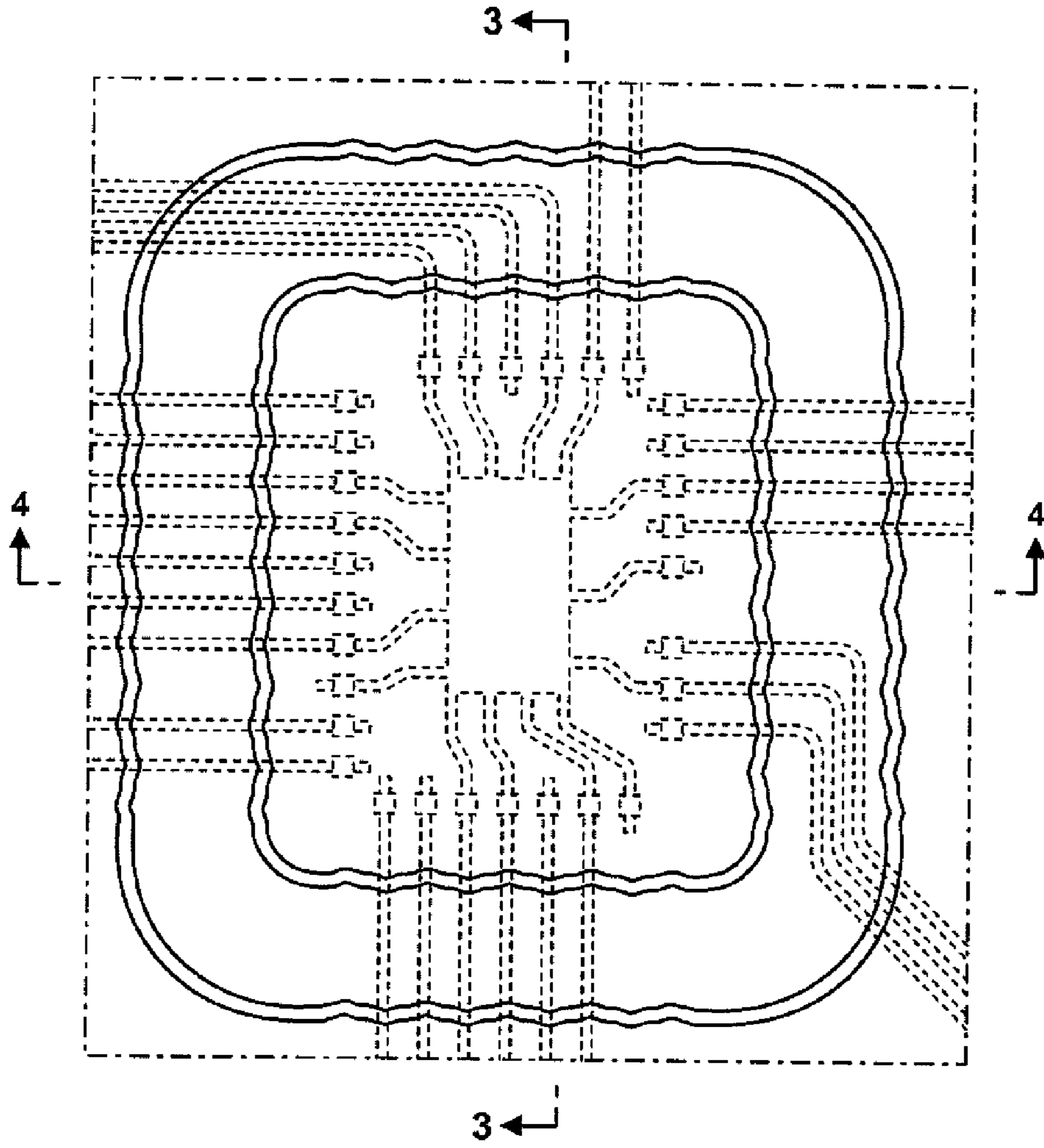


FIG. 2



FIG. 3

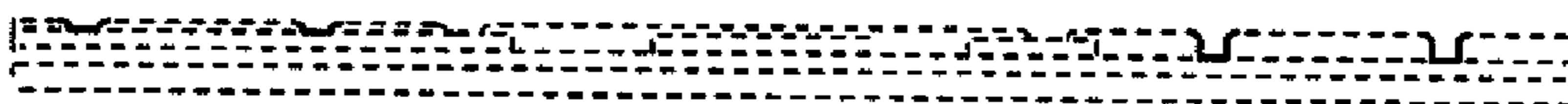


FIG. 4