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Terada et al.

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(54) GROOVES FORMED AROUND A SEMICONDUCTOR DEVICE ON A CIRCUIT BOARD

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(**) Term: **14 Years**

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Related U.S. Application Data

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(30) **Foreign Application Priority Data**

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May 1, 2006	(JP)	2006-011442

(51) **LOC (8) Cl.** **13-03**
(52) **U.S. Cl.** **D13/182**
(58) **Field of Classification Search** D13/182; 174/250, 251, 253, 254, 255, 256, 265, 260, 174/261; 361/760, 748, 720; 336/200
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

D319,629 S	*	9/1991	Hasegawa et al.	D13/182
5,420,558 A	*	5/1995	Ito et al.	336/200
5,467,252 A	*	11/1995	Nomi et al.	361/760

(Continued)

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(57) CLAIM

The ornamental design for grooves formed around a semiconductor device on a circuit board, as shown and described.

DESCRIPTION

FIG. **1** shows a plan view of the design according to a first embodiment of the invention.

FIG. **2** shows a bottom view of the design according to the invention. A claimed portion is not seen from the bottom.

FIG. **3** shows an enlarged view of a claimed portion as identified by the area boxed by the dash-dot-dash line in FIG. **1**.

FIG. **4** shows an enlarged sectional view along the line **4**—**4** in FIG. **3**.

FIG. **5** shows an enlarged sectional view along the line **5**—**5** in FIG. **3**.

FIG. **6** shows a perspective view of the design in FIG. **1**, on which an semiconductor device (not claimed) is disposed.

FIG. **7** shows an enlarged sectional view along the line **5**—**5** in FIG. **3**, on which a semiconductor device (not claimed) is disposed.

FIG. **8** shows a plan view of the design according to a second embodiment of the invention.

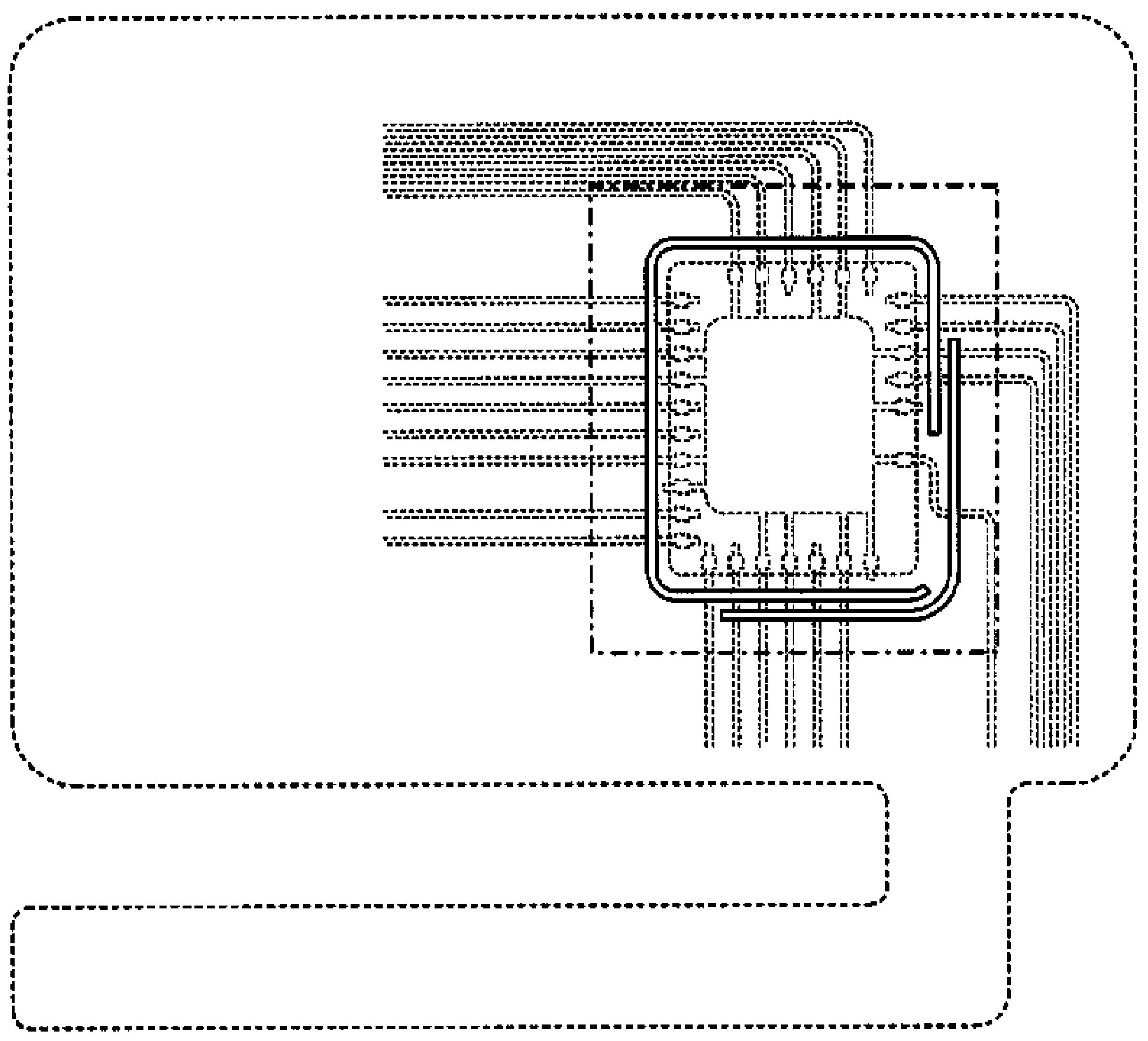
FIG. **9** shows an enlarged view of a claimed portion as identified by the area boxed by the dash-dot-dash line in FIG. **8**.

FIG. **10** shows an enlarged sectional view along the line **10**—**10** in FIG. **9**; and,

FIG. **11** shows an enlarged sectional view along the line **11**—**11** in FIG. **9**.

The elements shown in broken lines are for illustrative purpose only and form no part of the claimed invention.

1 Claim, 6 Drawing Sheets



U.S. PATENT DOCUMENTS

5,777,277	A *	7/1998	Inagawa	174/265
5,969,590	A *	10/1999	Gutierrez	336/200
6,114,937	A *	9/2000	Burghartz et al.	336/200
6,121,552	A *	9/2000	Brosnihan et al.	174/253
6,486,412	B2 *	11/2002	Kato	174/260
6,798,326	B2 *	9/2004	Iida	336/200
6,922,128	B2 *	7/2005	Vilander et al.	336/200
7,068,138	B2 *	6/2006	Edelstein et al.	336/200
7,126,452	B2 *	10/2006	Teshima et al.	336/200
D567,774	S *	4/2008	Tani et al.	D13/182
D568,836	S *	5/2008	Ohsawa et al.	D13/182
D568,838	S *	5/2008	Terada et al.	D13/182
2006/0266545	A1 *	11/2006	Takeuchi et al.	174/251
2007/0188287	A1 *	8/2007	Lien et al.	336/200
2007/0205856	A1 *	9/2007	Matsunaga et al.	336/200

* cited by examiner

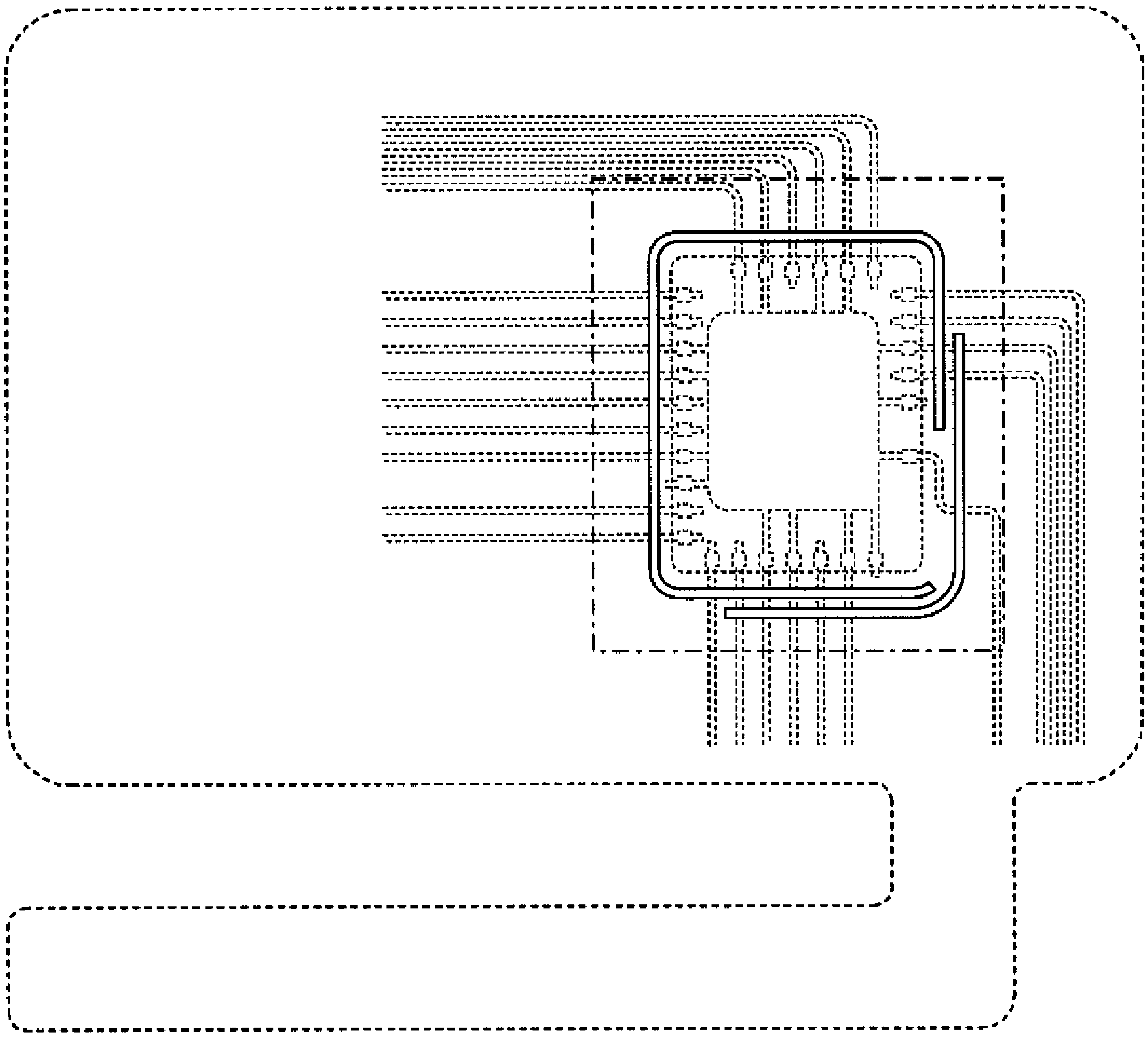


FIG. 1

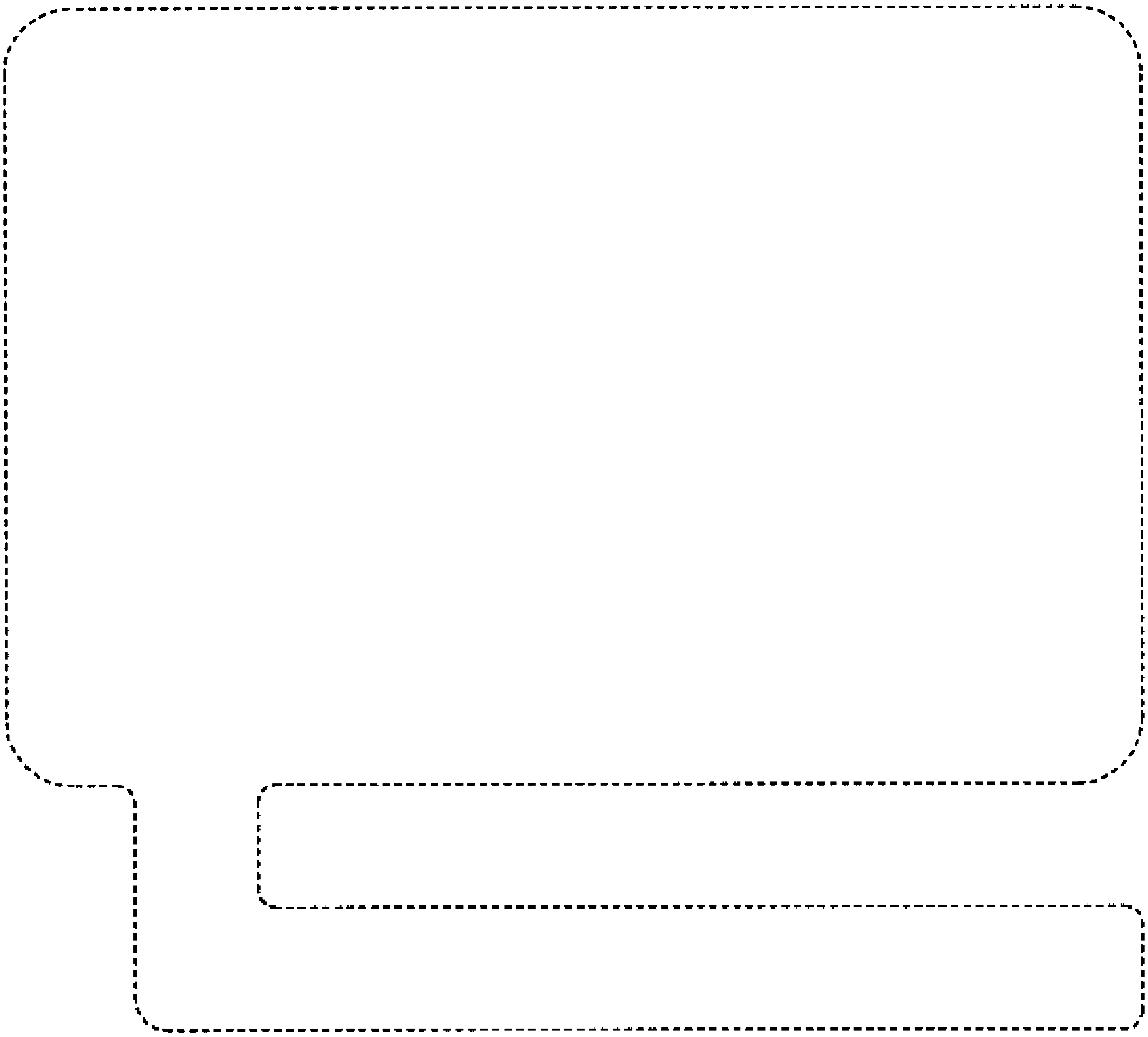


FIG. 2

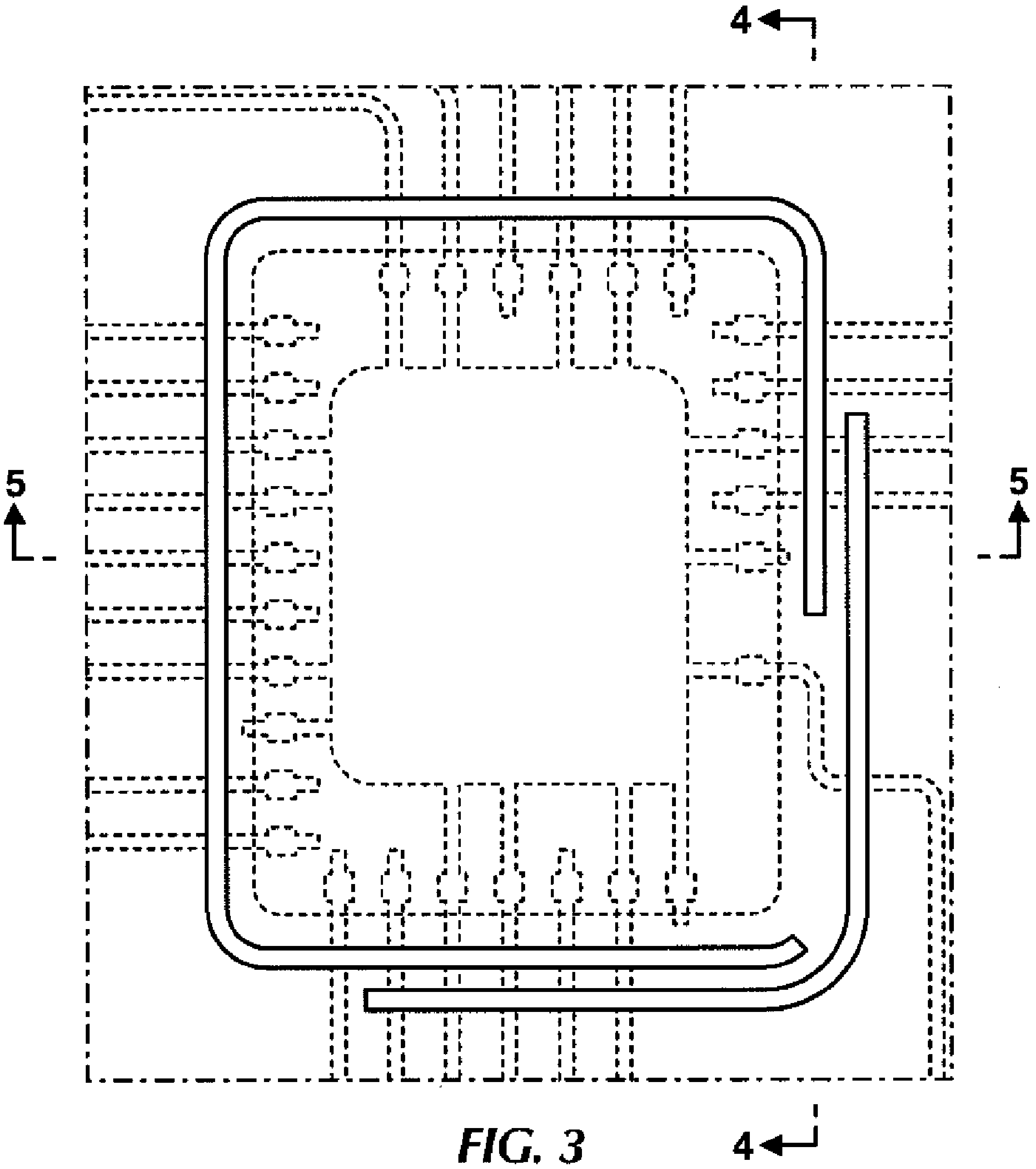


FIG. 3

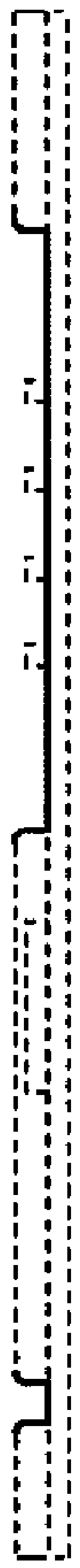


FIG. 4

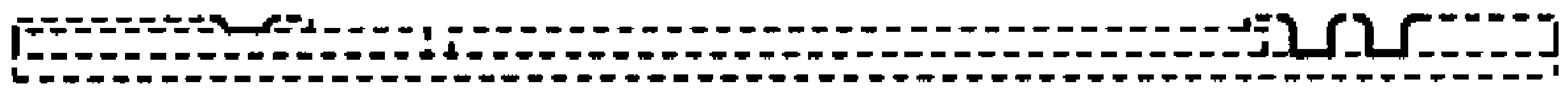


FIG. 5

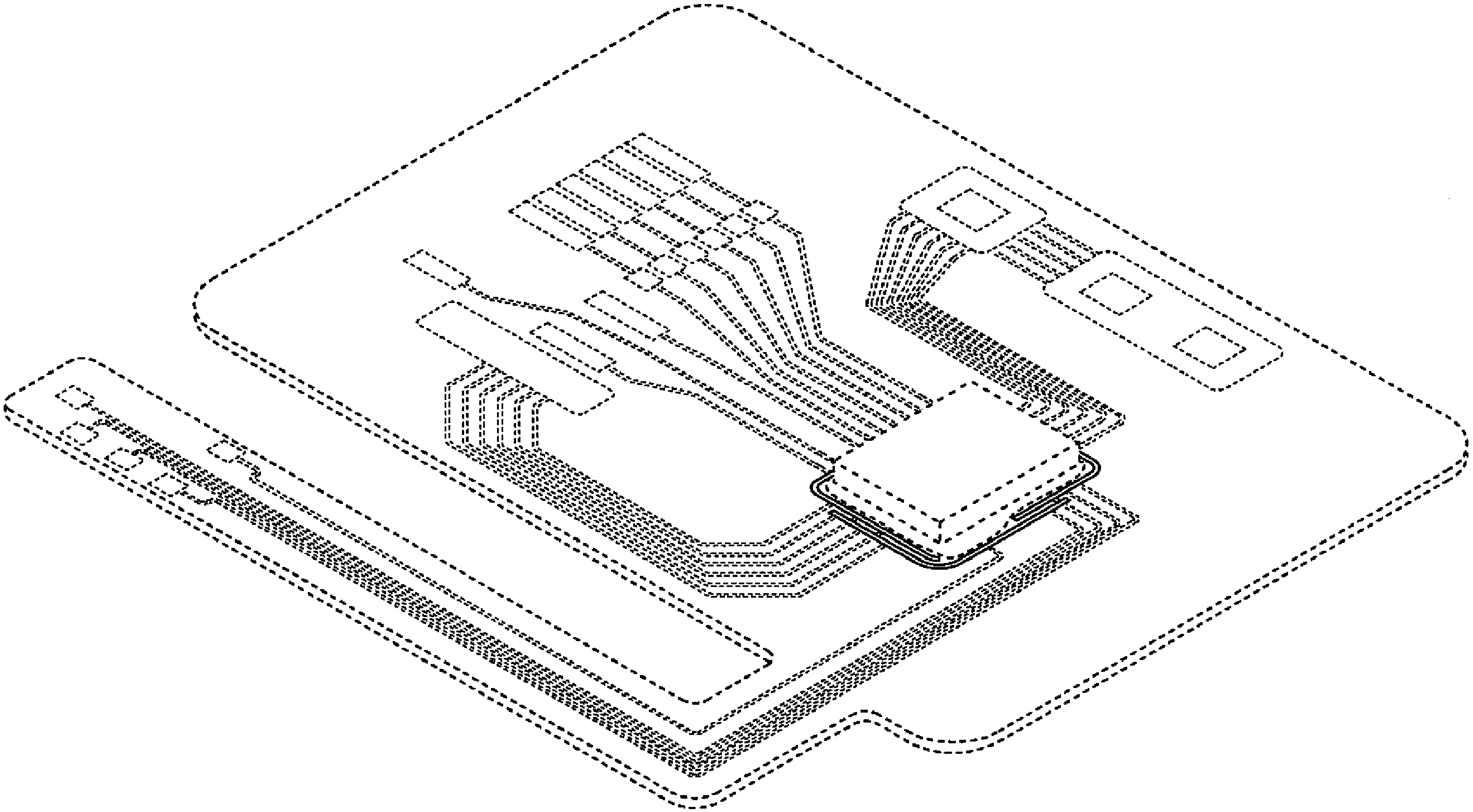


FIG. 6

FIG. 7

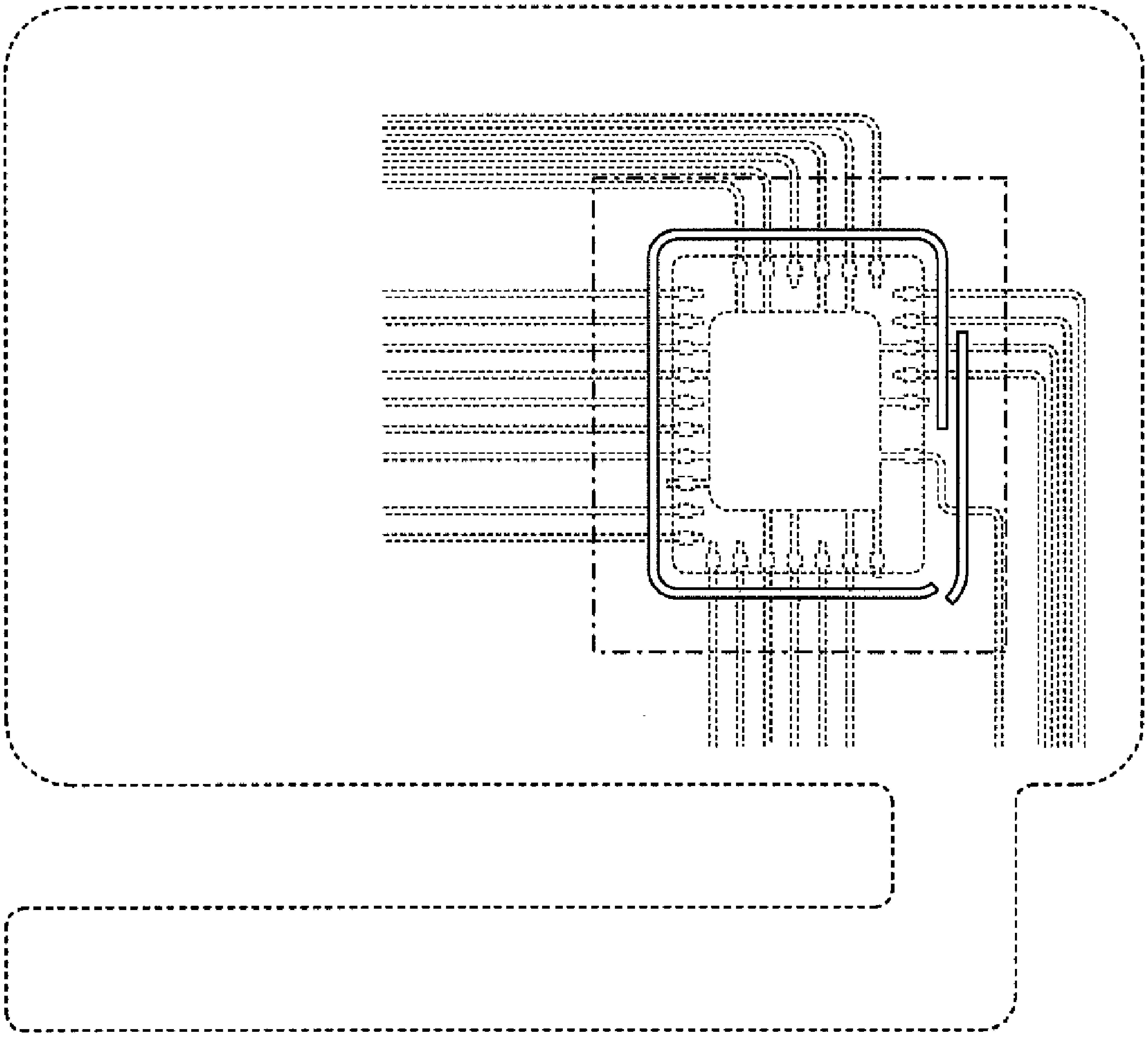


FIG. 8

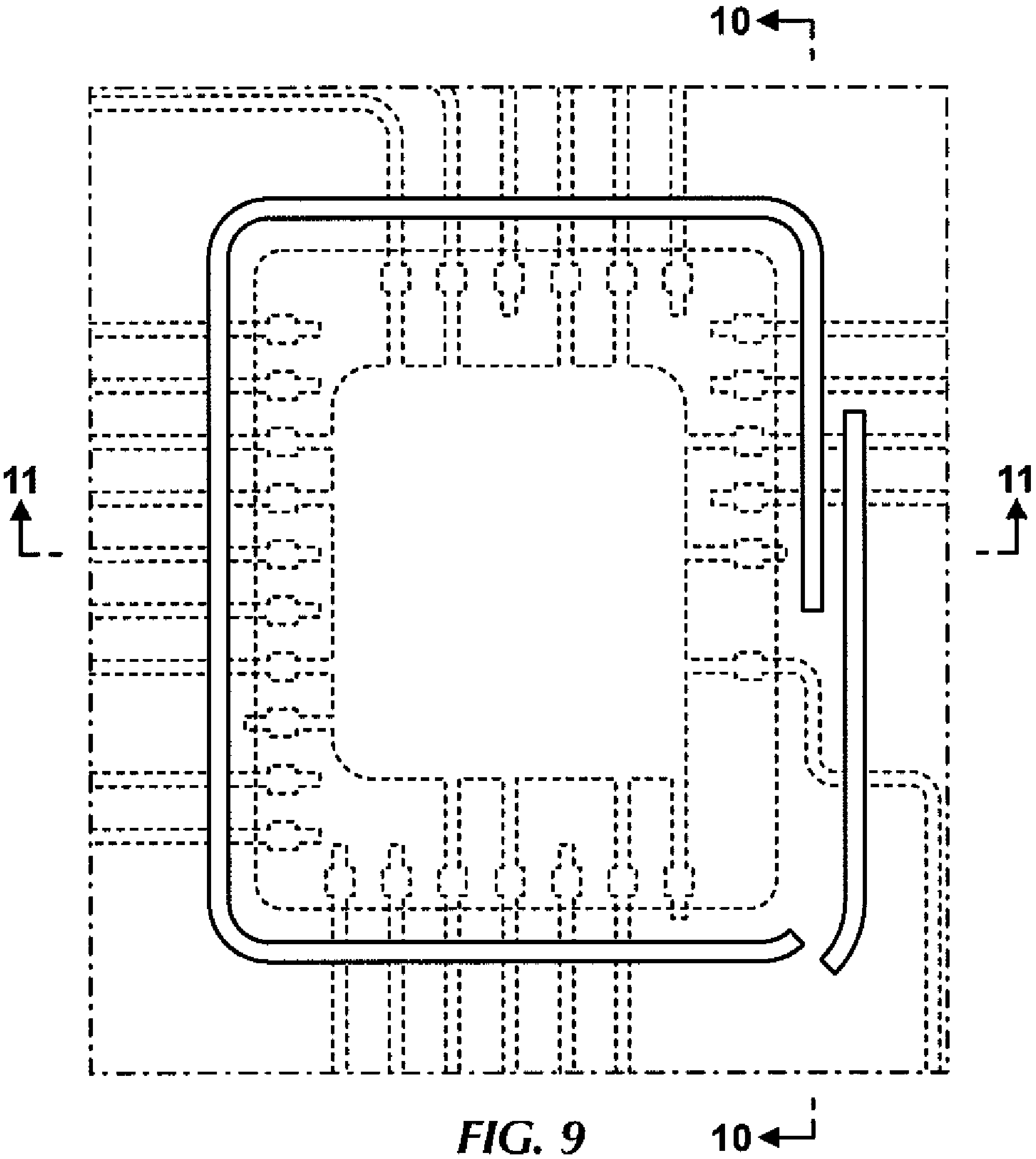


FIG. 9

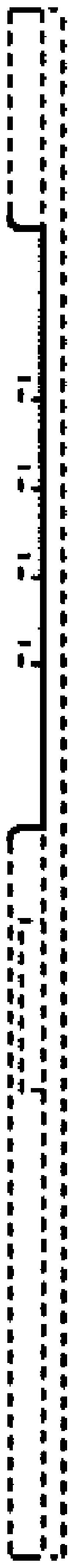


FIG. 10

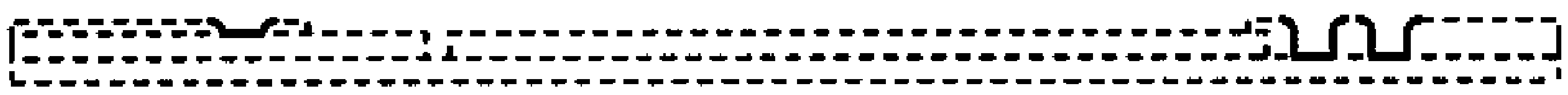


FIG. 11