



US00D580894S

(12) **United States Design Patent**
Sato

(10) **Patent No.:** **US D580,894 S**

(45) **Date of Patent:** **** Nov. 18, 2008**

(54) **WAFER BOAT**

(75) Inventor: **Izumi Sato**, Tokyo (JP)

(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)

(**) Term: **14 Years**

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(22) Filed: **Nov. 1, 2006**

(30) **Foreign Application Priority Data**

May 1, 2006 (JP) 2006-011365

(51) **LOC (8) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
118/715, 724, 728; 206/711; 211/41.18
See application file for complete search history.

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Primary Examiner—Selina Sikder
(74) *Attorney, Agent, or Firm*—Smith, Gambrell & Russell, LLP

(57) **CLAIM**

The ornamental design for a wafer boat, as shown and described.

DESCRIPTION

FIG. 1 is a side sectional view of the wafer boat as viewed along line 1—1 in FIG. 6.

FIG. 2 is a cross sectional view of the wafer boat as viewed along line 2—2 in FIG. 9.

FIG. 3 is another side sectional view of the wafer boat.

FIG. 4 is another side sectional view of the wafer boat.

FIG. 5 is perspective view of the wafer boat.

FIG. 6 is a bottom view of the wafer boat.

FIG. 7 is an enlarged, side, isolated view of a portion of the wafer boat within the area 7—7 in FIG. 9.

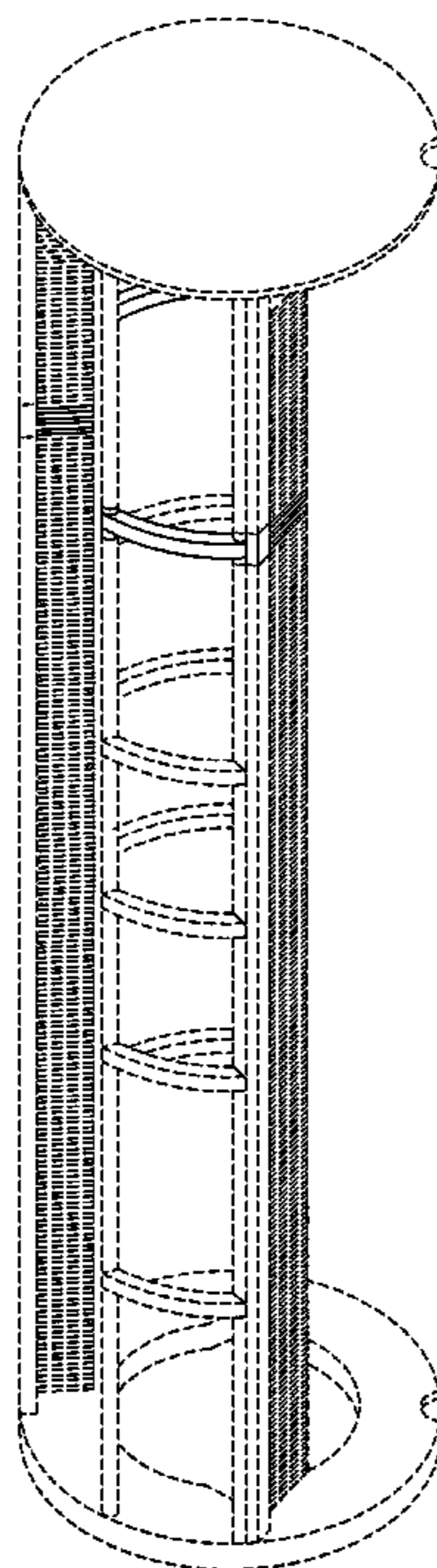
FIG. 8 is a top view of the wafer boat; and,

FIG. 9 is another side view of the wafer boat with focus on the portion shown in FIG. 7.

The rear elevation appears symmetrical with an elevational view.

Broken lines are used throughout the drawings to disclose the environment related to the claimed design. Dash lines are used throughout the drawings to define the boundary of the claimed design.

1 Claim, 7 Drawing Sheets



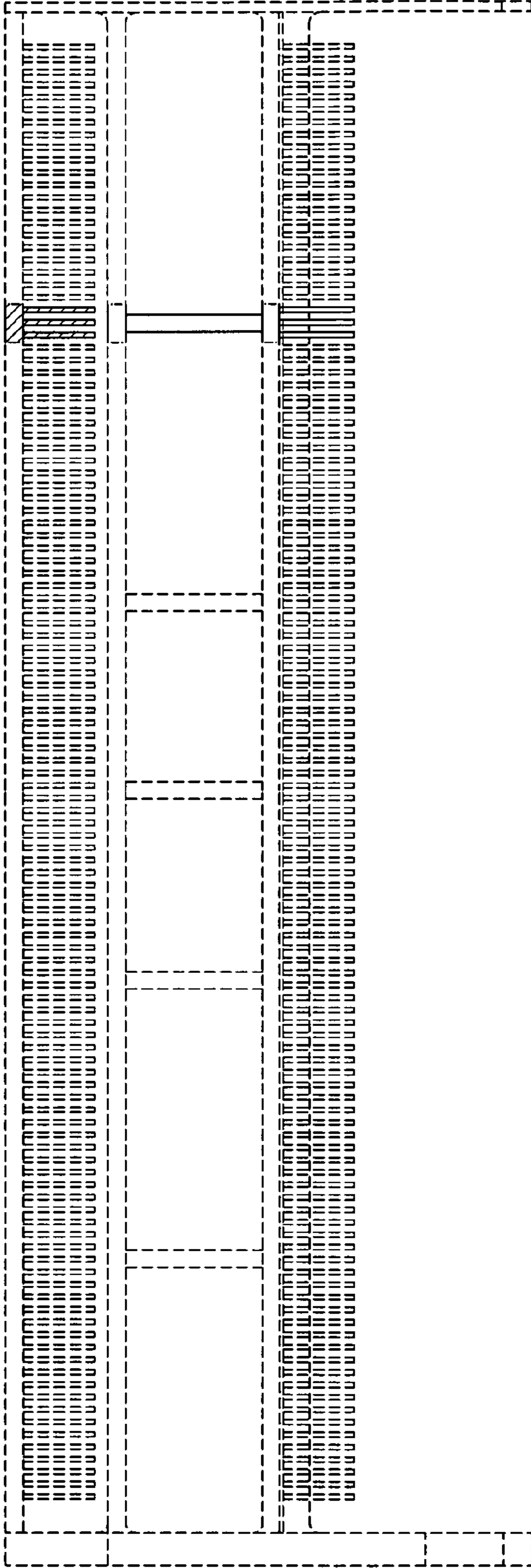


FIG. 1

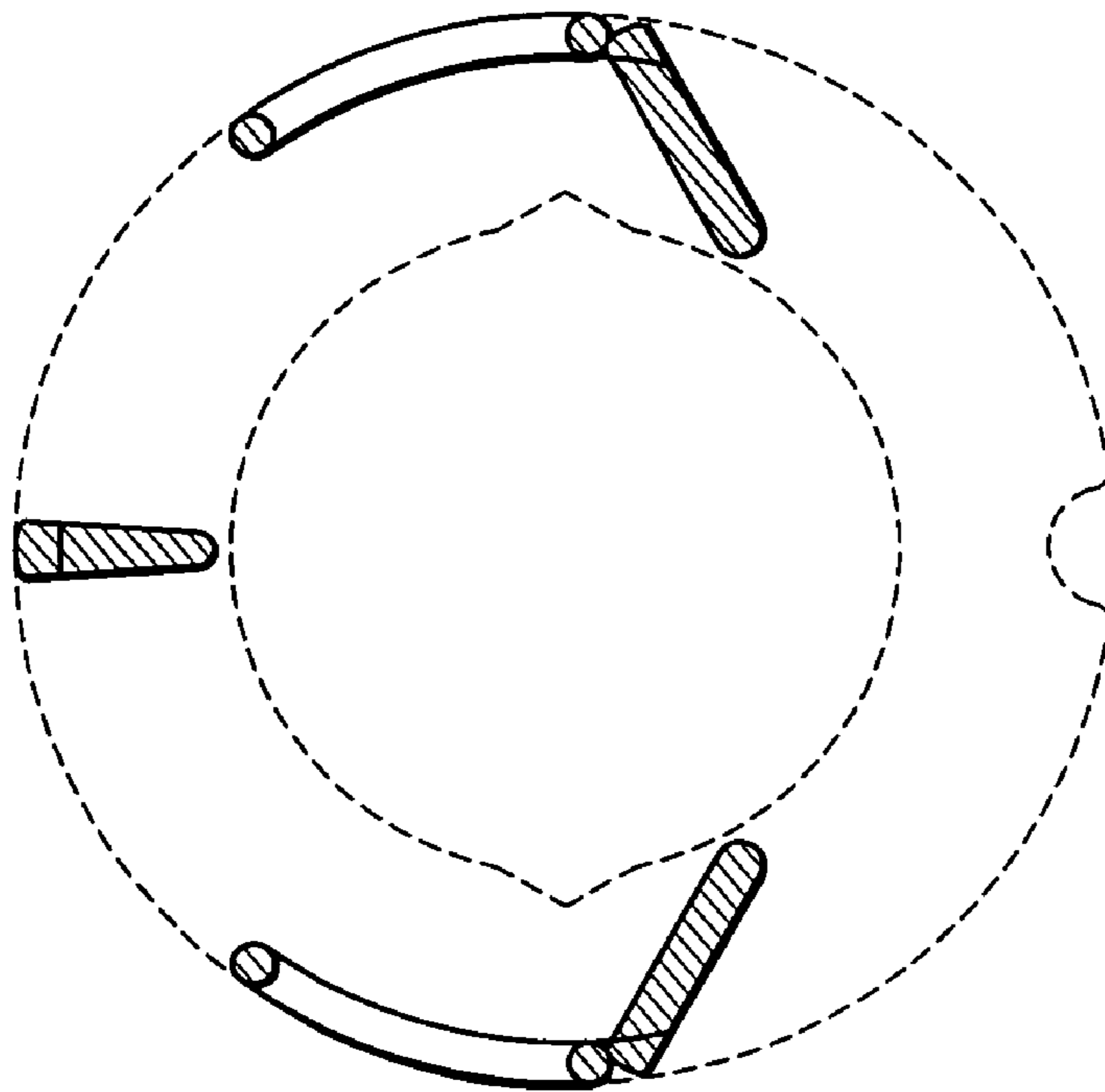


FIG. 2

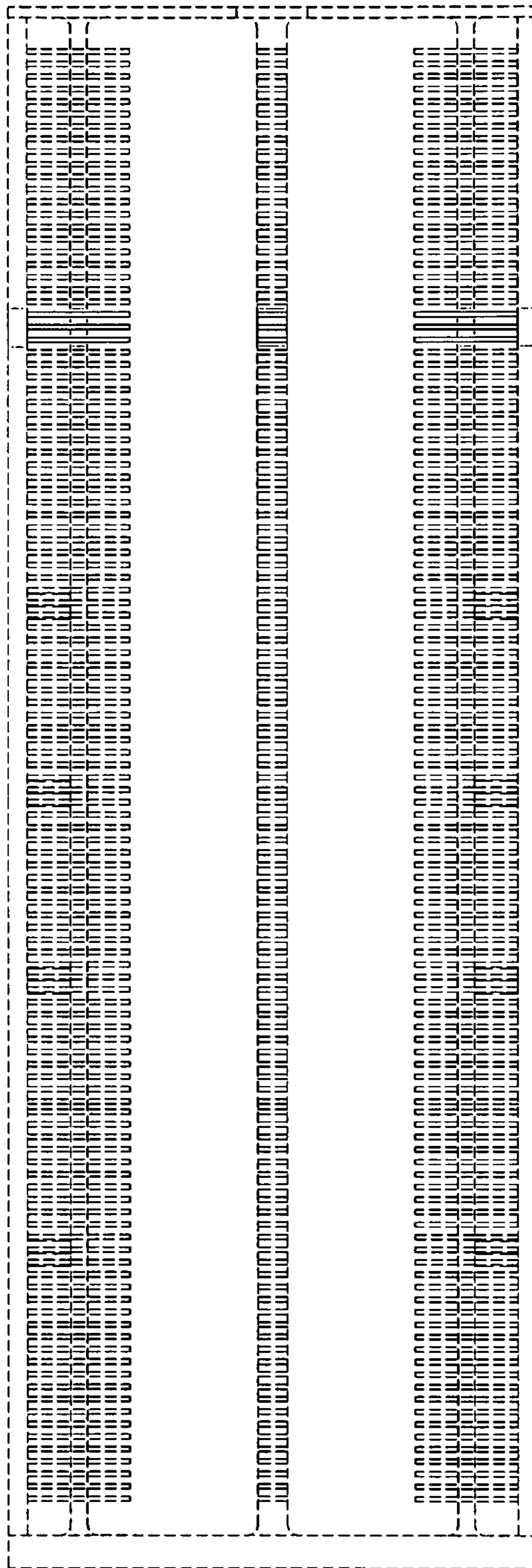


FIG. 3

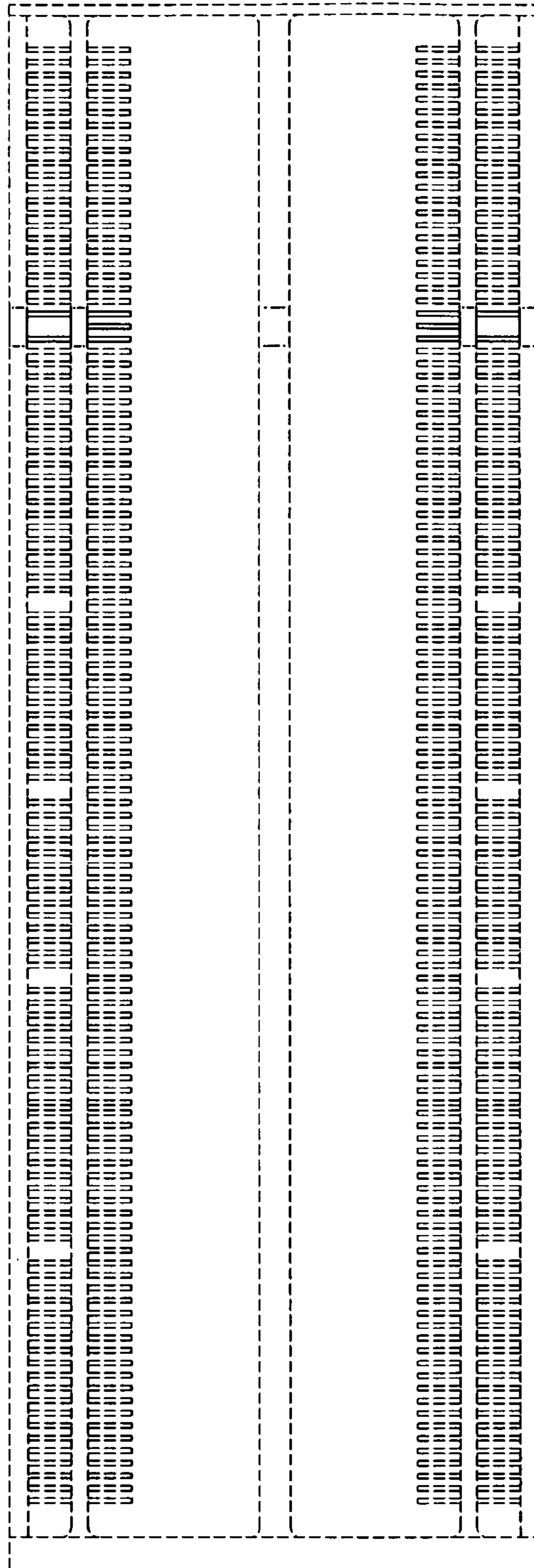


FIG. 4

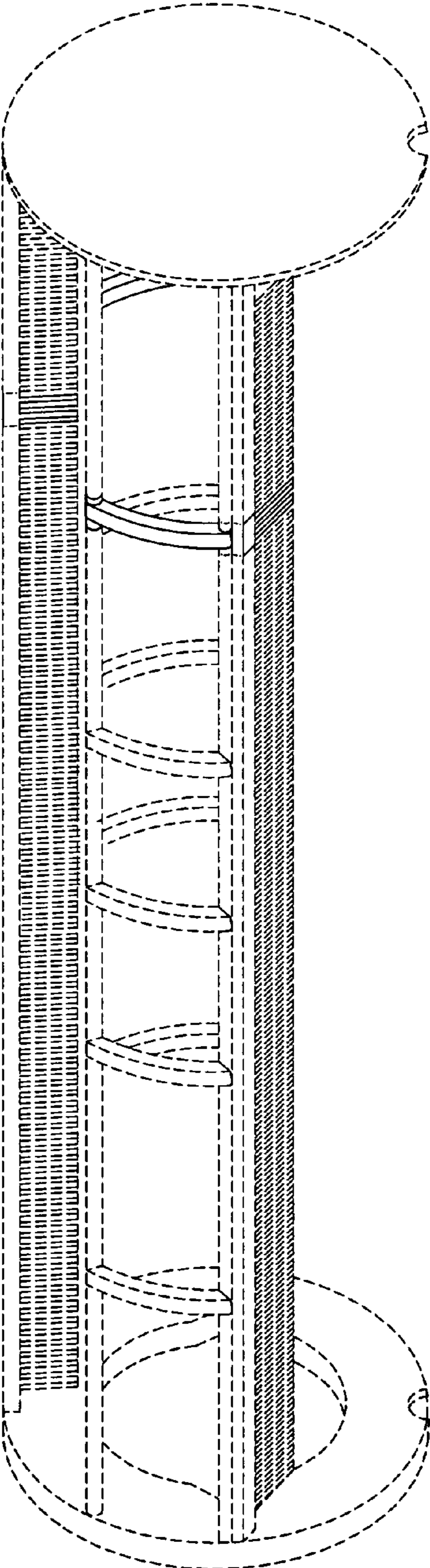


FIG. 5

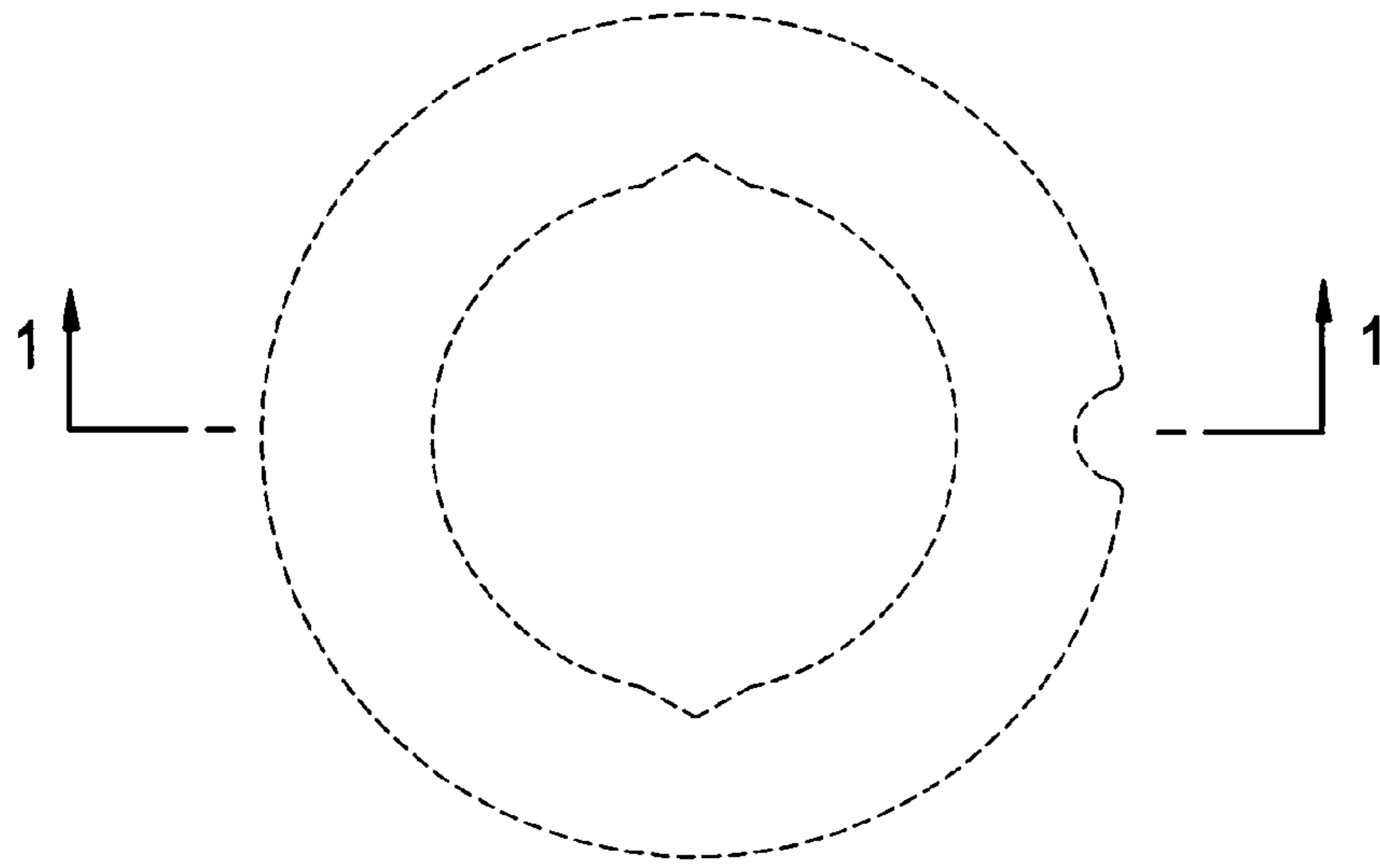


FIG. 6

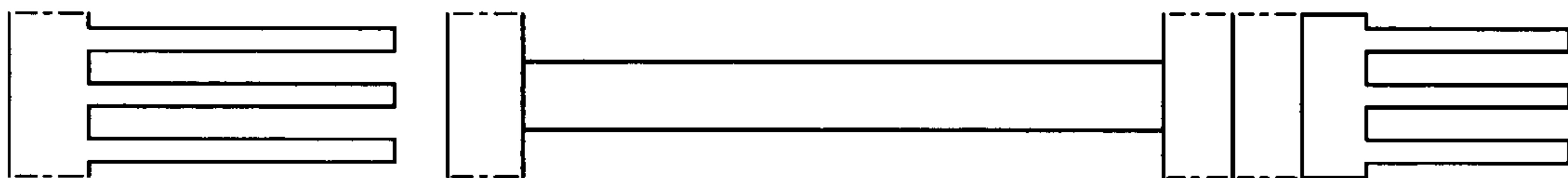


FIG. 7

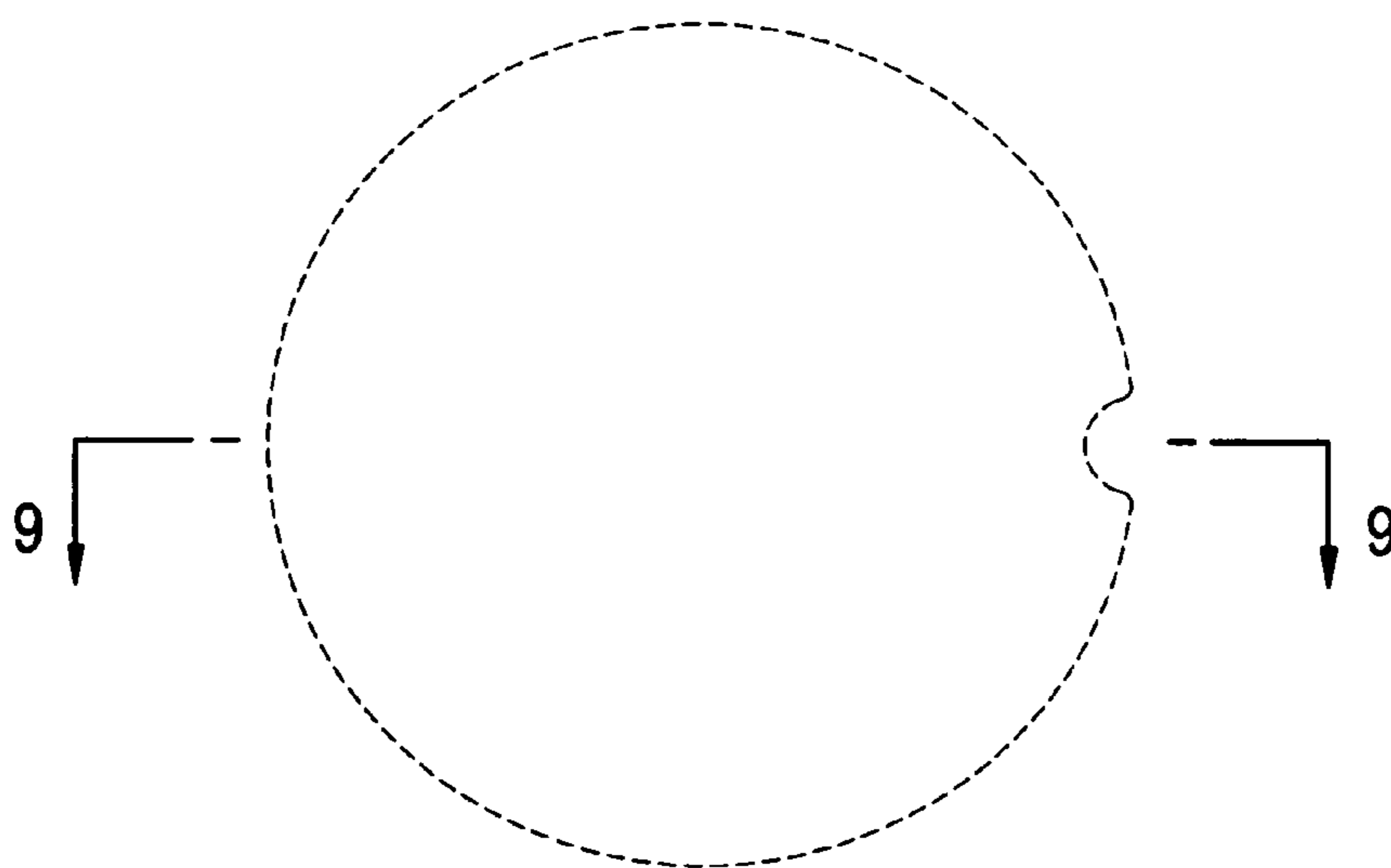


FIG. 8

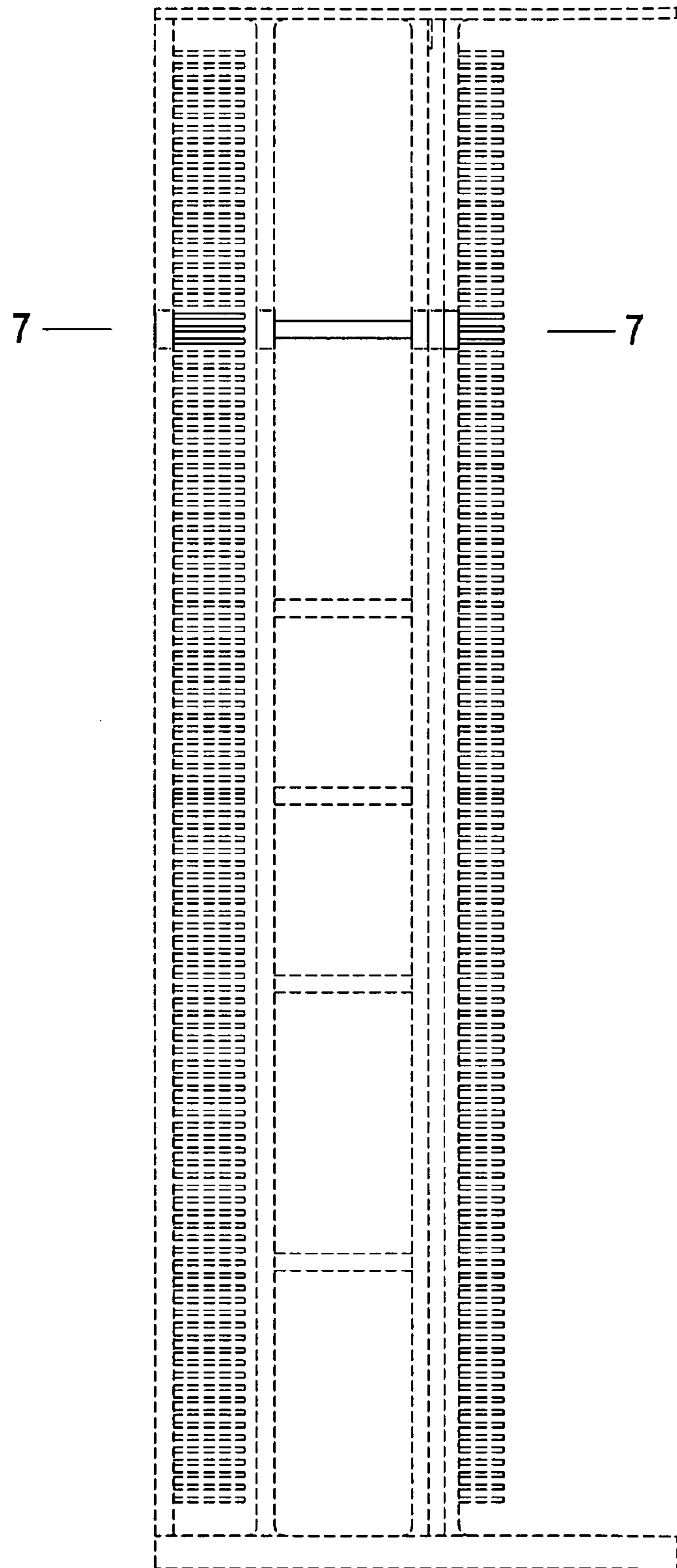


FIG. 9