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(12) **United States Design Patent**
Hosaka

(10) **Patent No.:** **US D571,740 S**
(45) **Date of Patent:** **** Jun. 24, 2008**

(54) **SEMICONDUCTOR WAFER DELIVERY APPARATUS**

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(73) Assignee: **Tokyo Electron Limited**, Tokyo (JP)

(**) Term: **14 Years**

(21) Appl. No.: **29/242,546**

(22) Filed: **Nov. 14, 2005**

(30) **Foreign Application Priority Data**

Aug. 12, 2005 (JP) 2005-023555

(51) **LOC (8) Cl.** **13-03**

(52) **U.S. Cl.** **D13/182**

(58) **Field of Classification Search** D13/182;
134/110; 396/611; 414/331.15, 411, 416.03;
700/213

See application file for complete search history.

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(57) **CLAIM**

The ornamental design for a semiconductor wafer delivery apparatus, as shown and described.

DESCRIPTION

FIG. 1 is a front elevational view of a semiconductor wafer delivery apparatus, showing my design;

FIG. 2 is a rear elevational view thereof;

FIG. 3 is a left side elevational view thereof;

FIG. 4 is a right side elevational view thereof;

FIG. 5 is a top plan view thereof;

FIG. 6 is a bottom plan view thereof;

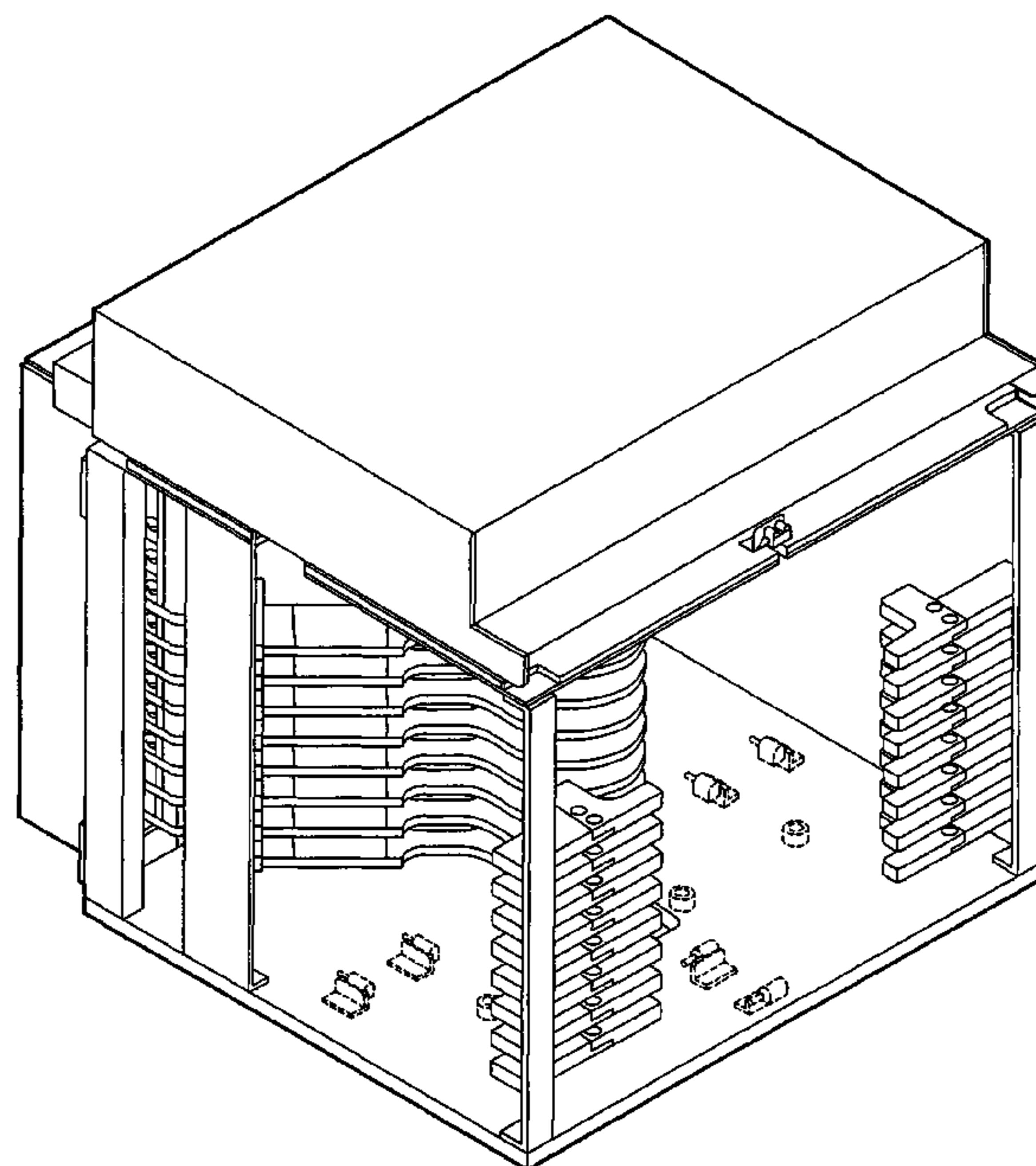
FIG. 7 is a cross-sectional view taken along line 7—7 in FIG. 1;

FIG. 8 is a top and right front perspective view thereof; and,

FIG. 9 is a top and right rear perspective view thereof.

The broken line showing and the indicia shown in the Figures are shown for illustrative purposes only and form no part of the claimed design.

1 Claim, 9 Drawing Sheets



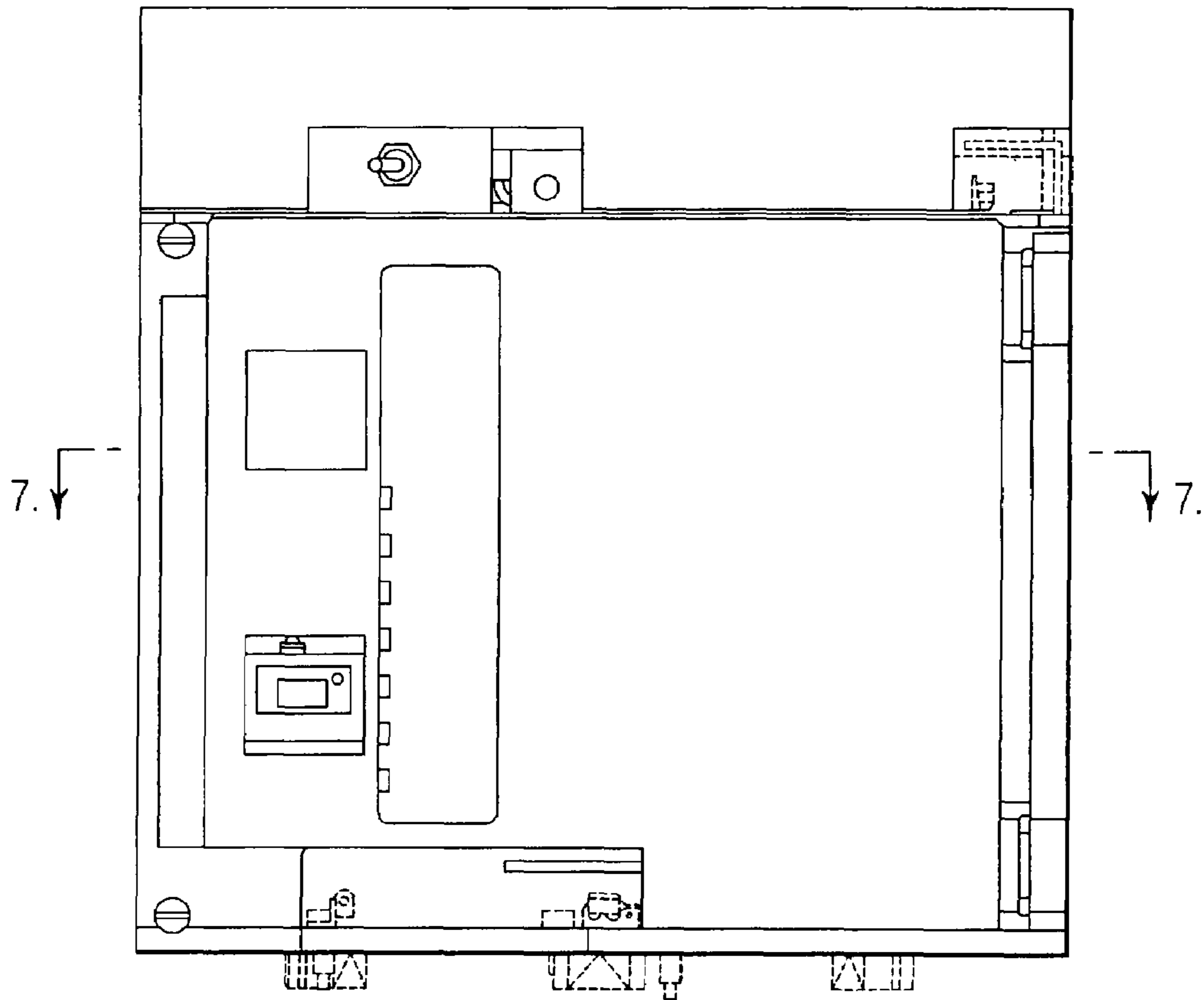


Fig. 1

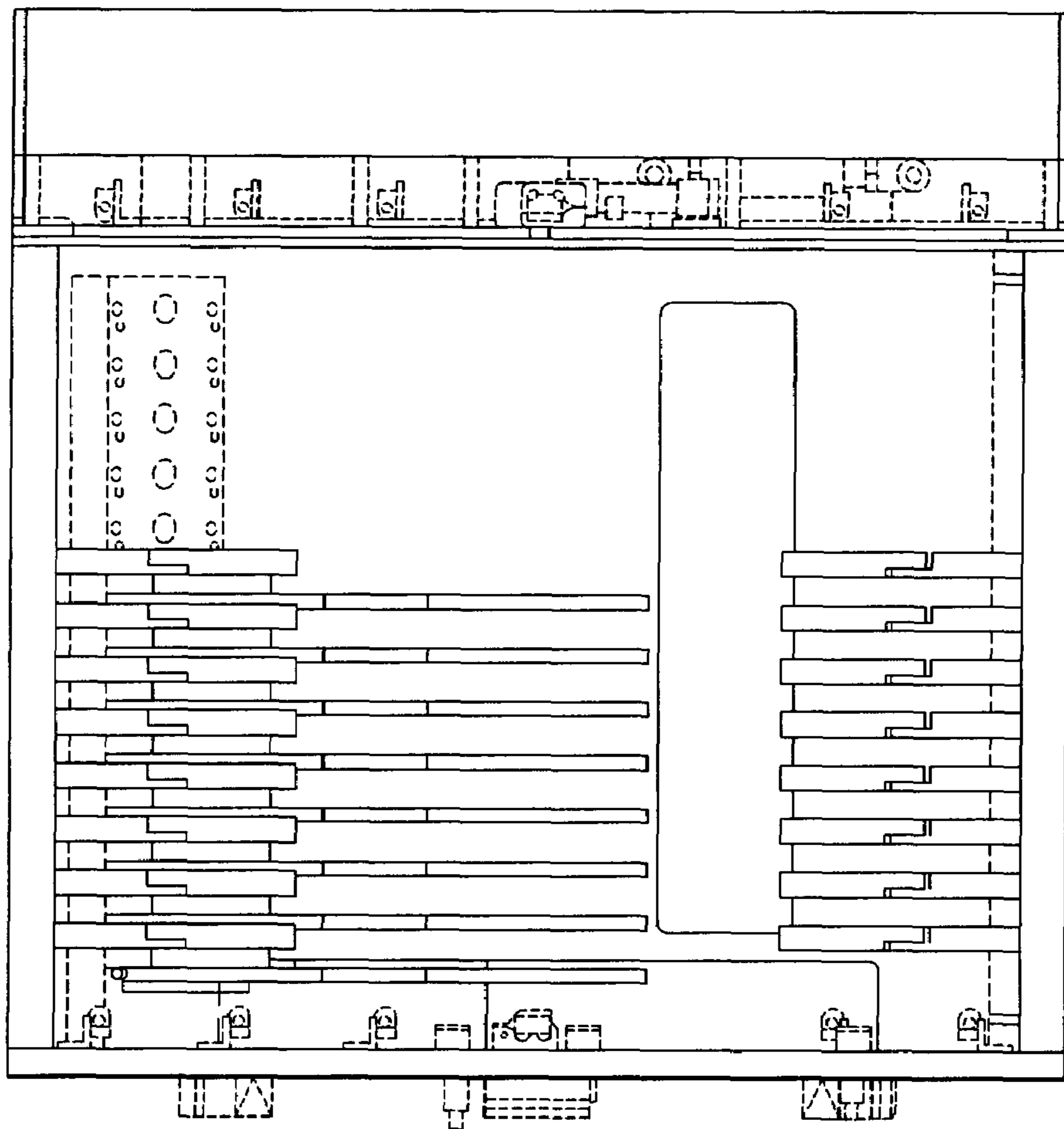


Fig. 2

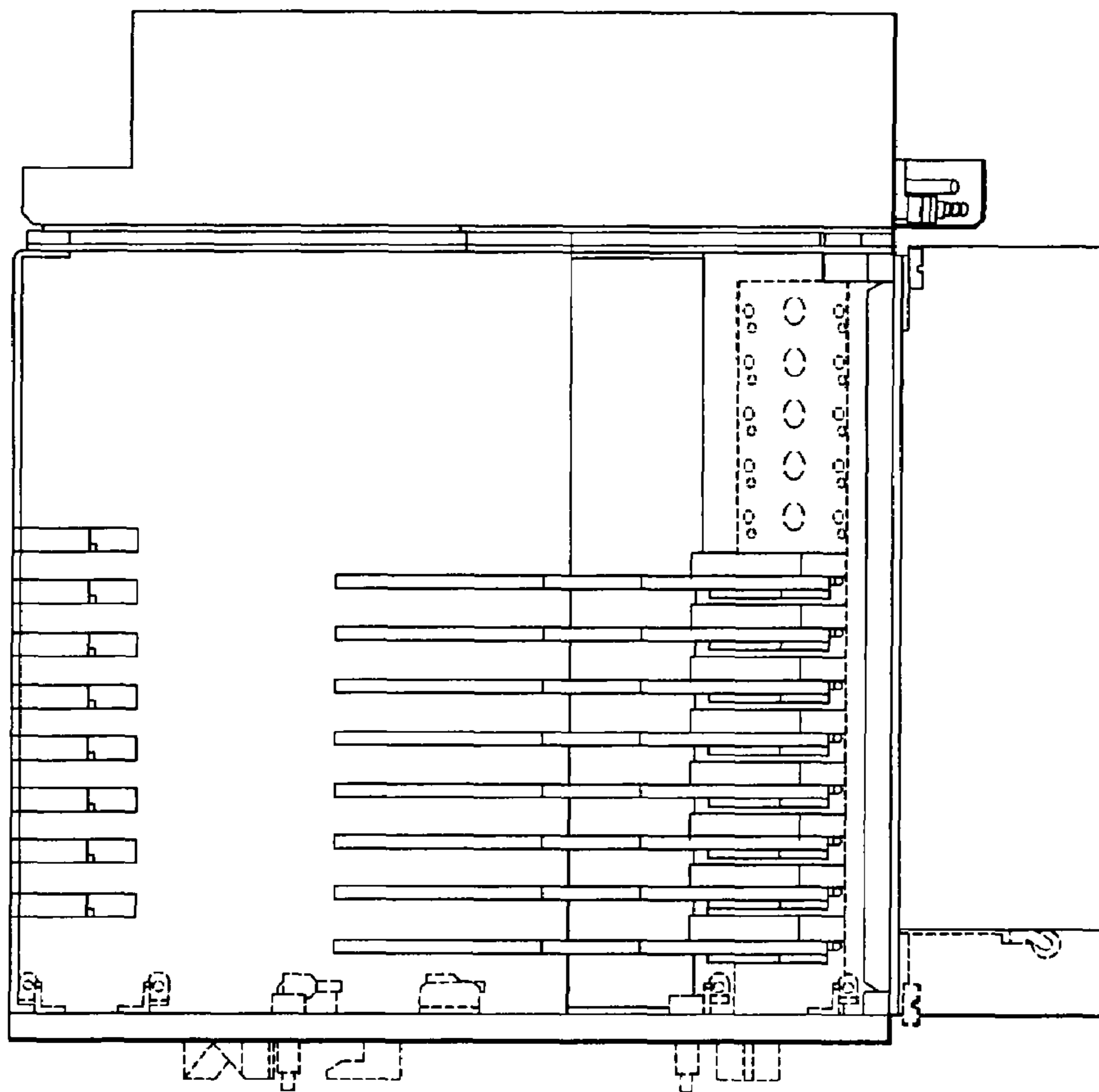


Fig. 3

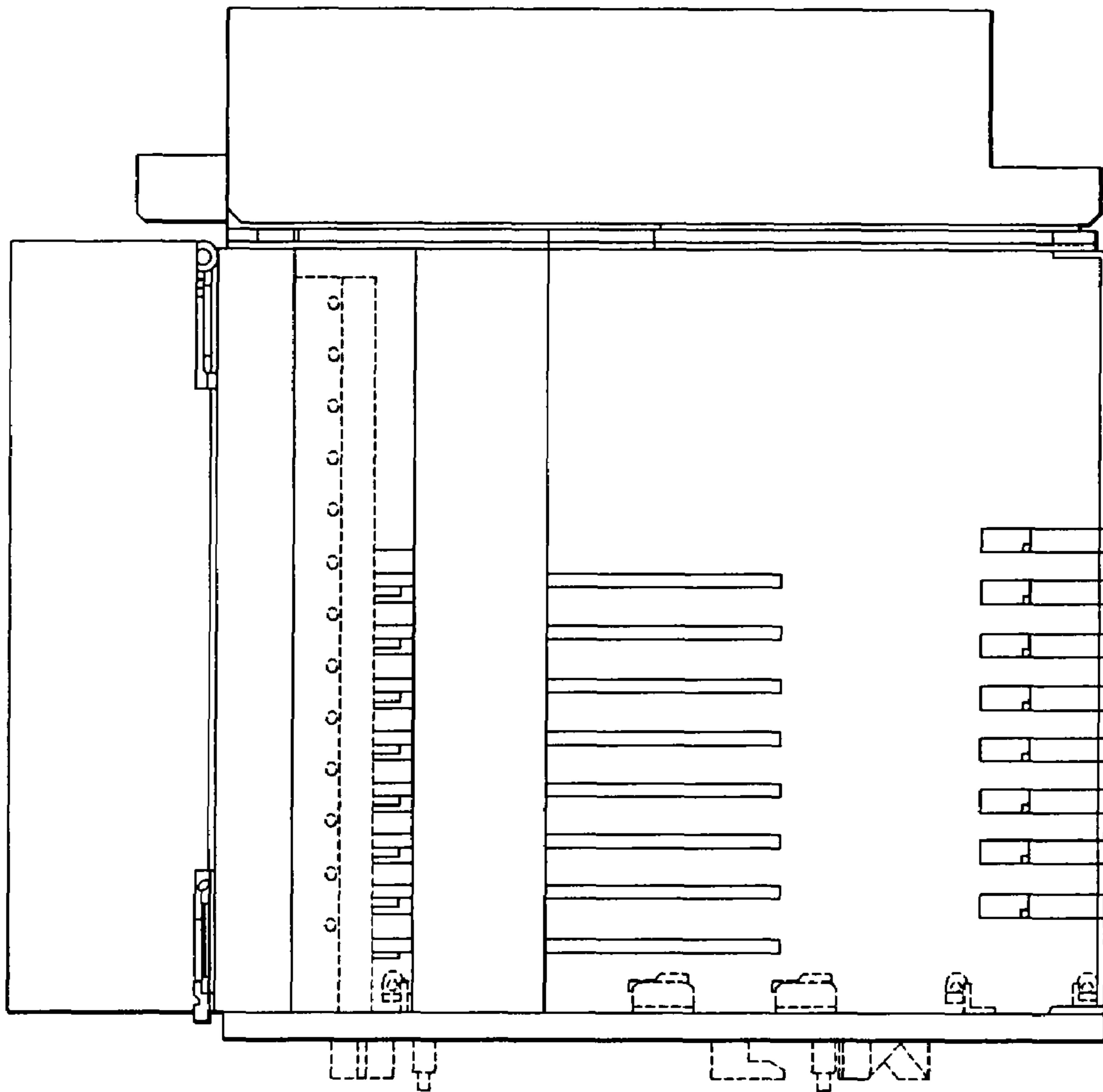


Fig. 4

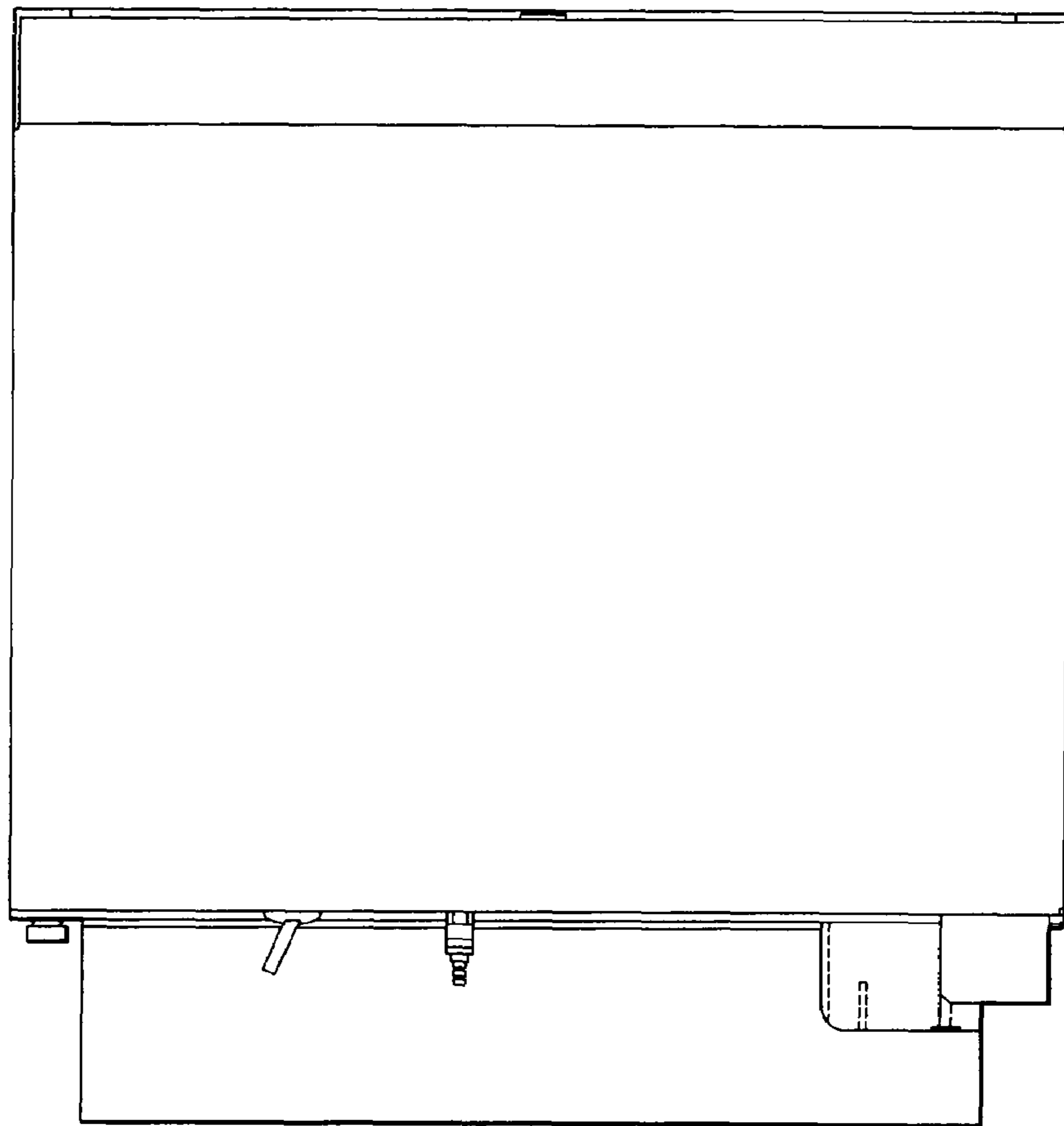


Fig. 5

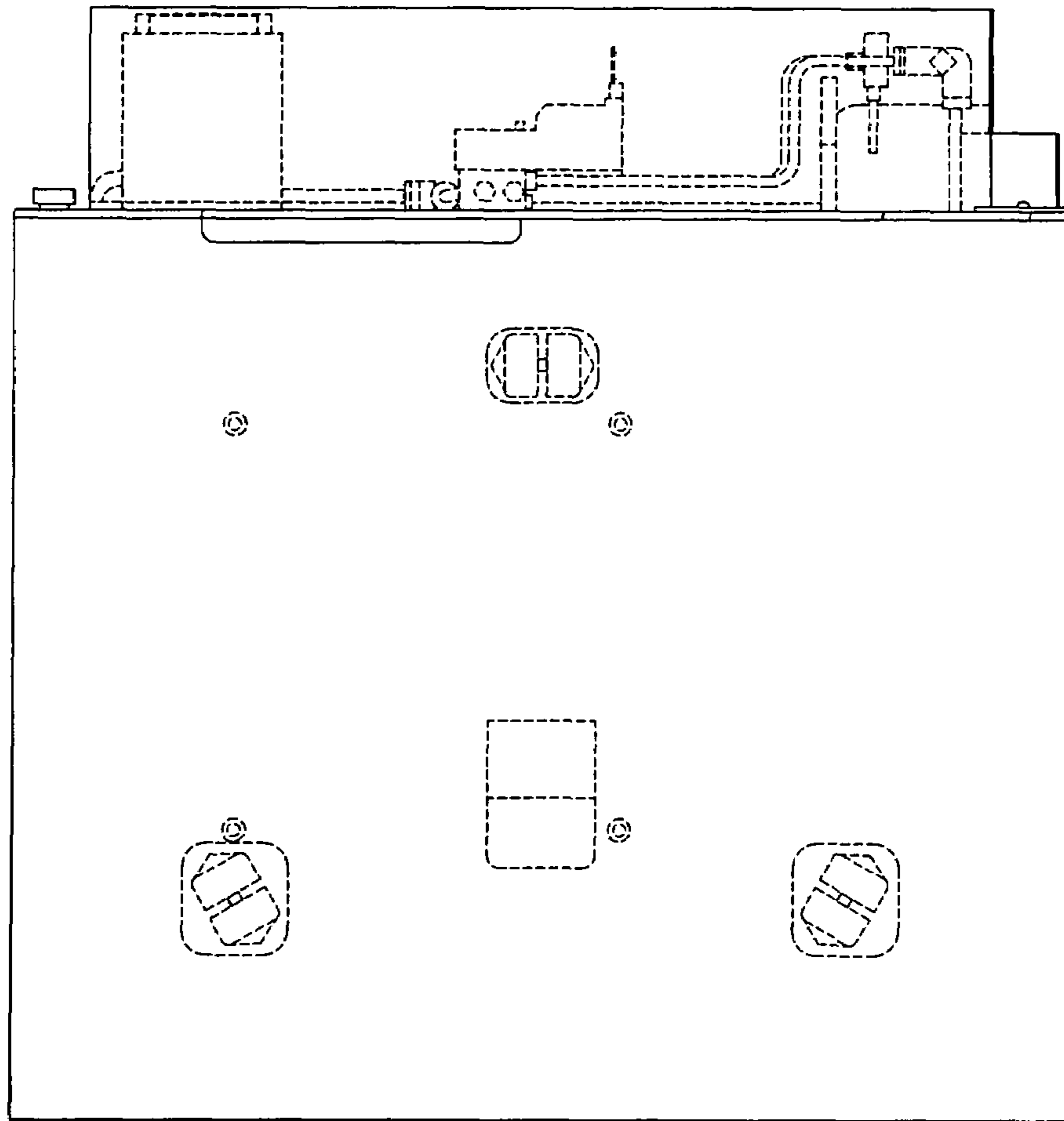


Fig. 6

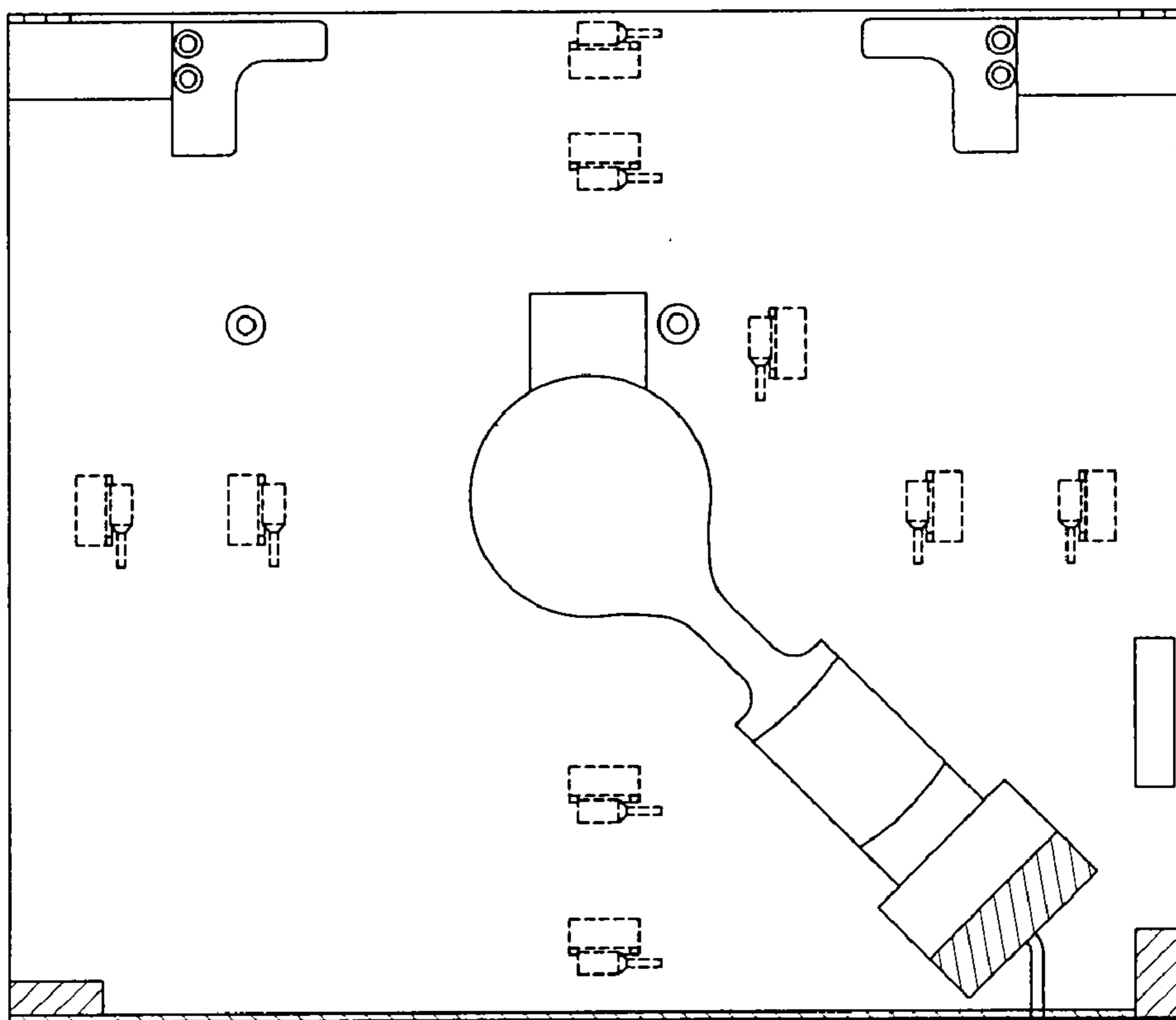


Fig. 7

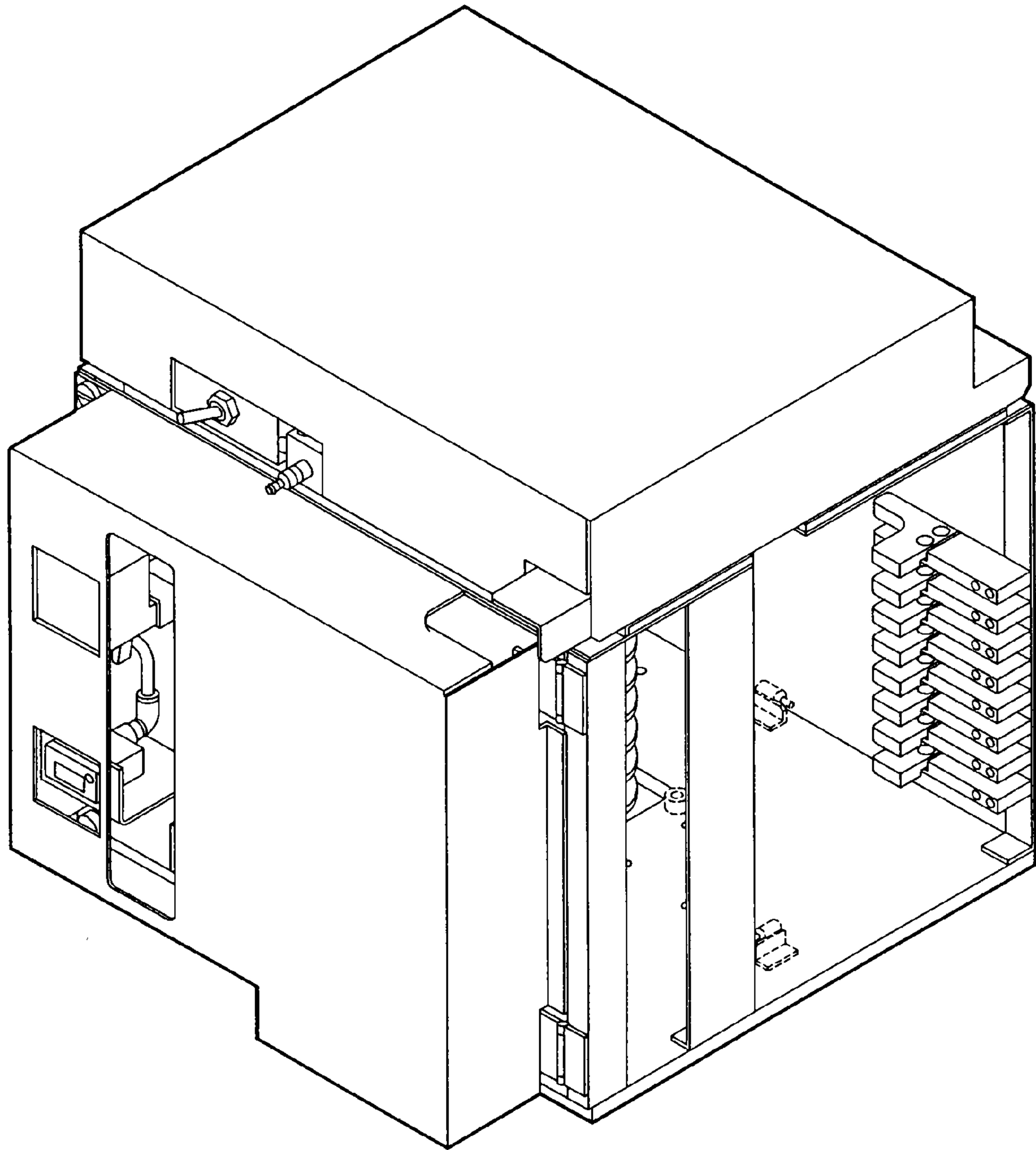


Fig. 8

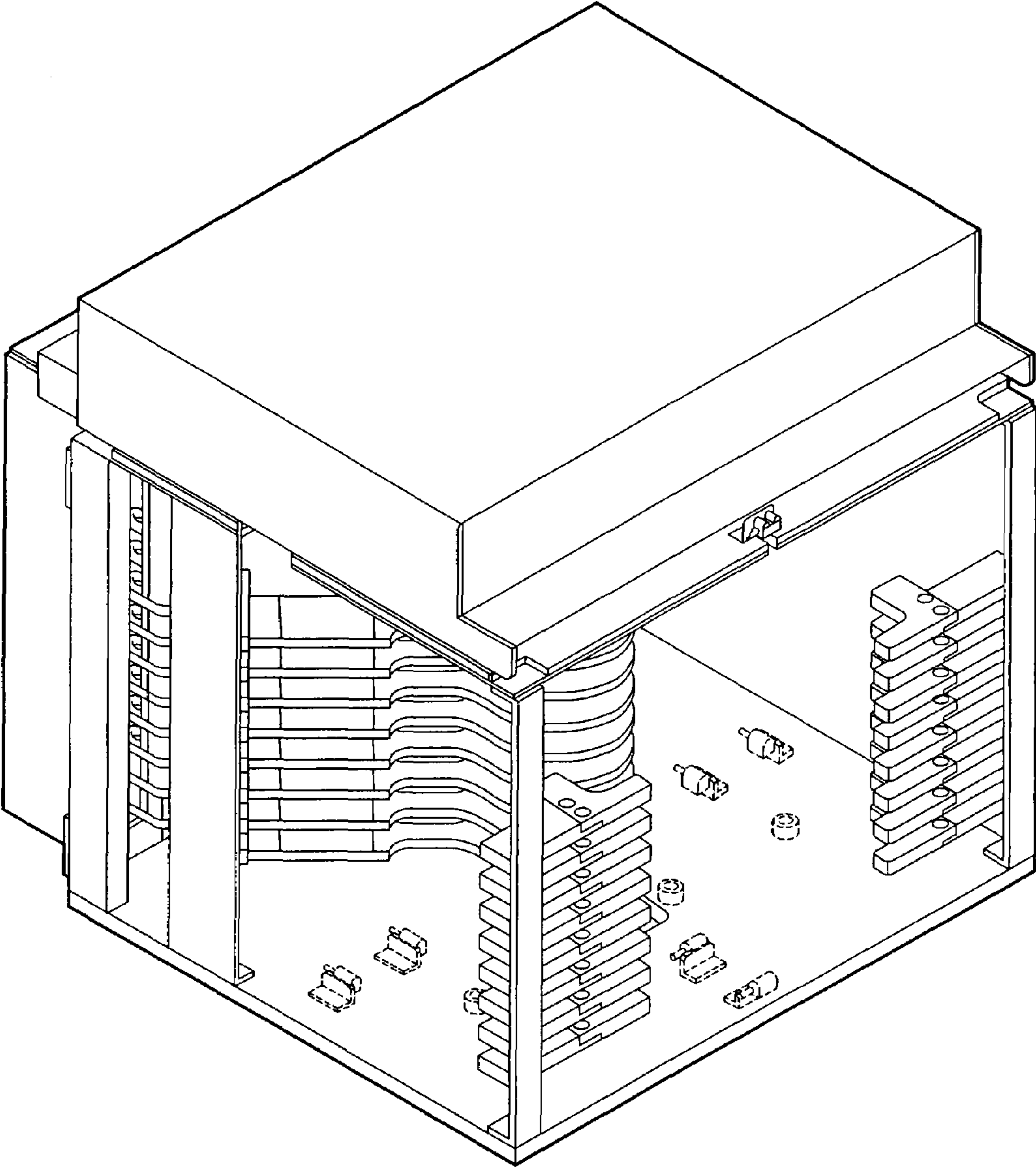


Fig. 9